



HAL
open science

NUMERICAL MODELING OF GATE TURN-OFF THYRISTOR USING SICOS

D. G. Ni, Gérard Rojat, Guy Clerc, Jean-Pierre Chante

► **To cite this version:**

D. G. Ni, Gérard Rojat, Guy Clerc, Jean-Pierre Chante. NUMERICAL MODELING OF GATE TURN-OFF THYRISTOR USING SICOS. IEEE Transactions on Industrial Electronics, 1993, 40 (3), pp.326-333. hal-00140576

HAL Id: hal-00140576

<https://hal.science/hal-00140576>

Submitted on 25 Apr 2007

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Numerical Modeling of Gate Turn-off Thyristor Using SICOS

Da-Guang Ni, Gerard Rojat, Guy Clerc, and Jean-Pierre Chante

Abstract—This paper presents a numerical model of gate turn-off thyristors (GTO's). The new concept of a controlled-switch realized by a controlled-current source is first introduced. Using this basic model, an equivalent circuit of the GTO is given. According to the characteristics of GTO given by manufacturers, the equations connected with all the parameters of the equivalent circuit are deduced. All of the parameters of the equivalent circuit are determined. A sample study is presented at the end of the paper. We have simulated this numerical model with the SICOS program and the results are in concordance with the experiment.

V_T = on-state voltage
 I_H = holding current
 V_{DRM} = repetitive peak off-state voltage
 I_{TRMS} = maximum rms on-state current
 t_d = delay time
 t_r = rise time
 t_s = storage time
 t_f = minimum off-time
 t_l = tail time
 I_{GQM} = peak turn-off gate current
 di_{GQ}/dt = maximum rate of rise of reverse gate current

I. INTRODUCTION

GATE turn-off thyristors (GTO's) of rated high voltage and high current are becoming increasingly used in power electronic applications and are replacing Static Converter Simulation (SCR's). Many models of GTO's have been proposed for the simulation of power circuits. These models can usually be divided into two groups: the first one is the ideal controlled switch. This type of switch model has only two states (ON and OFF) without considering the transition area of turn-on and turn-off. It is obvious that they are not suitable for simulating high-power converters. The second type of switch is based on semiconductor physics. As a model of GTO, they are very effective. However, this type of model is very difficult to use in simulation of power converters because the internal physics parameters are not given by manufacturers.

In this paper, we propose a new model of GTO. It is entirely based on the characteristics of GTO's, which are very easy to find in data sheets or obtained by experimental methods. The equivalent circuit obtained from this model can be realized easily in a good number of simulation programs. It represents the dynamic and static behaviors of a GTO.

II. CHARACTERISTICS OF A GTO

dI/dt = maximum rate of rise of on-state current
 I_{TAVM} = maximum average on-state current
 I_{TGQM} = maximum controllable turn-off current

Manuscript received July 12, 1992.
 The authors are with URA 829, Centre de Génie Electrique de Lyon, 69131, Ecully Cedex, France.
 IEEE Log Number 9207940.

Fig. 1 shows the typical current and voltage waveforms of GTO's. From these, we will try to produce an equivalent circuit that contains such characteristics.

III. STRUCTURE OF AN EQUIVALENT CIRCUIT FOR A GTO

A. Model of a Controlled Switch

A controlled switch is the switch that can be turned on or turned off by another voltage across another component. This component is either an element in the same power circuit as the controlled switch or an another element in another independent circuit. It can also be a branch of a network in series or in parallel.

Based on this concept, an equivalent circuit of the controlled switch is presented in Fig. 2. It is composed of a controlled-current source with two diodes, one in series with it and the other in parallel. The behaviors of this switch are described as follows.

1) When the voltage V_C is negative, the current of the controlled-current source $I(t) = 0$. The impedance of the source is infinite. The switch is turned off.

2) When the voltage V_C is greater than zero, the current of the controlled-current source $I(t) = K*V_C$, making diode D_1 turn on. The controlled switch thus appears as a small impedance. It is equal to

$$R_{AB} = (R_{D1} + R_{D2}) - R_{D1} \frac{I}{I_A}$$

If V_{AB} is negative, diode D_1 turns off and it withstands the inverse voltage. It is clear that the current of this switch is unidirectional and its voltage is bidirectional.

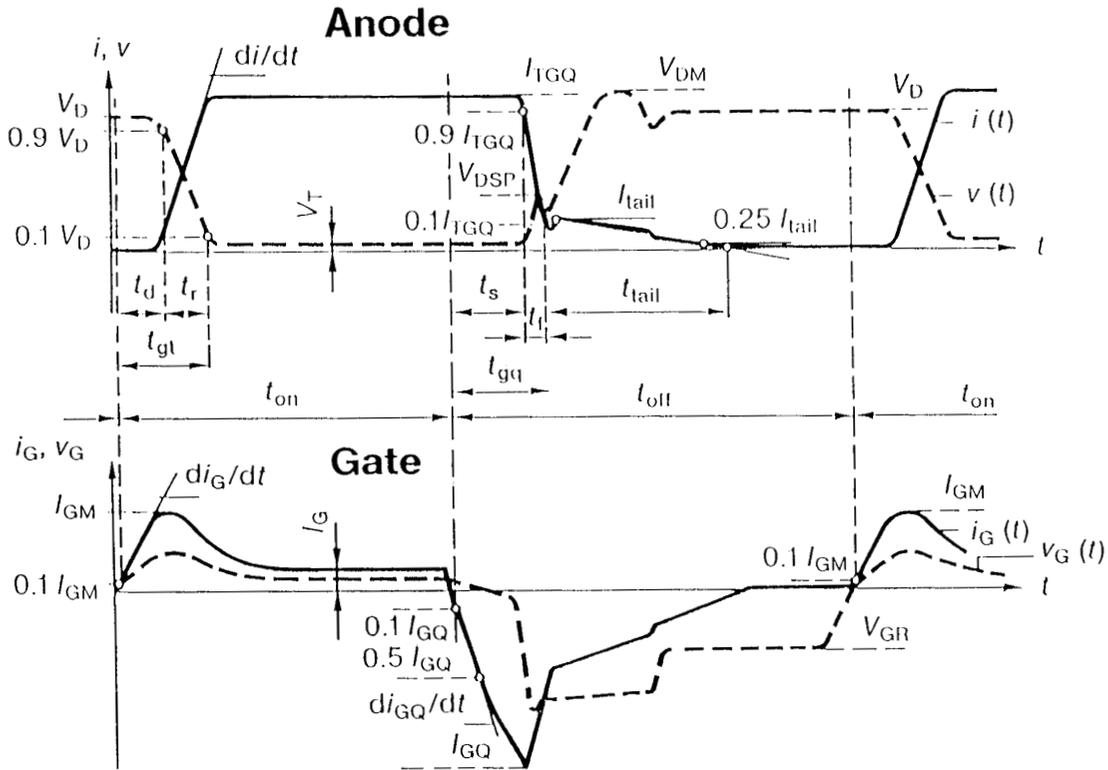


Fig. 1. General current and voltage waveforms with GTO-specific symbols.

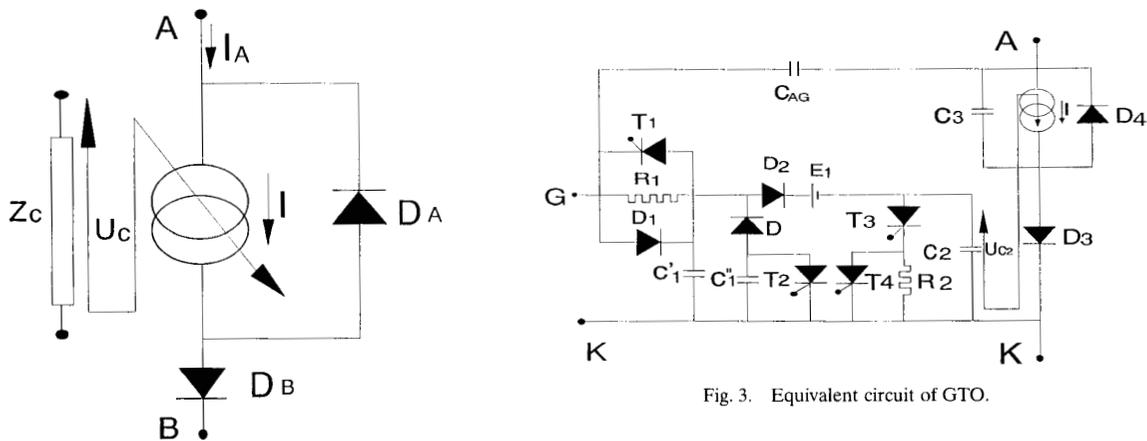


Fig. 2. Equivalent circuit of a controlled switch.

Fig. 3. Equivalent circuit of GTO.

B. Model of a GTO

Using the model of the controlled switch, we propose the equivalent circuit of the GTO as shown in Fig. 3. T_1 , T_2 , T_3 , and T_4 are ideal switches. Nodes A , K , and G represent, respectively, the anode, cathode, and gate of the GTO; D_1 , D_2 , D_3 , D_4 , and D_5 are ideal diodes; C_1 , C_2 , C_3 , and C_{AG} are ideal capacitors; and $I(t)$ is a controlled-current source. The GTO is controlled by

$U_{c2}(t)$, the voltage of capacitor C_2 . The equivalent circuit of a GTO also includes considerations of inverse voltage, holding current, and parasitic capacitance.

IV. BEHAVIORS OF EQUIVALENT CIRCUIT OF A GTO

At the instant $t = t_1$, a positive source is applied to the gate of the GTO (point G). C_1 is charged up to instant t_d . When $t = t_d$, $U_{c1}(t_d) = E_1$, the diode D_2 is conducting. Capacitor C_2 begins charging. At instant t_d , the controlled source $I(t)$ supplies the current and capacitor C_3 begins charging. This decreases the anode potential and increases the anode current. The GTO is conducting.

At $t = t_r$, the voltage $U_{c2}(t_r)$ reaches a value at which the current of the controlled source $I(t)$ is greater than the load current. Diode D_4 turns on and the part of the current that is superior to the load current passes through D_4 . After this moment, the GTO is entirely turned on.

At instant t_2 , the negative source is applied to the gate of GTO. Capacitor C'_1 begins charging inversely. When the voltage U_{c1} reaches the value zero, C'_1 and C''_1 are connected in parallel. From this time, C'_1 and C''_1 are charged in the inverse direction up to t_3 . This period (t_2-t_3) can be used as GTO storage time for simulation purposes. At $t = t_3$, $U_{c1}(t_3)$ reaches the value U_{cp} . Here, $C_1 = C'_1 + C''_1$. T_3 turns on, and C_2 discharges. This brings a decrease of the current i_{D3} . When the current of diode D_3 falls under the zero, T_1 is turned off. As a result of the insertion of R_1 , the gate current decreases. When the anode current is less by 10% anode current, T_4 turns off and the GTO enters the high-resistance state. During this time, there is still a small current (tail current). R_2 is inserted in the circuit T_3 , C_2 represents this phenomenon.

V. DETERMINATION OF THE PARAMETERS OF THE EQUIVALENT CIRCUIT

We have given an equivalent circuit for a GTO. It is certain that this equivalent circuit is based on the concept of black box, i.e., only external characteristics are considered. For example, it can also describe switch times t_d , t_r , t_s , t_f , etc.

According to the equivalent circuit (a three-terminals network), we are going to determine parameters R_1 , R_2 , and R_{T4} (the resistance of T_4 in the on-state), C'_1 , C''_1 , C_2 , C_3 , and the transconductance K of the controlled-current source $I(t)$. We consider that E_1 is smaller than E_{g1} and is strictly superior to zero. E_{g1} is a positive voltage source applied to the gate of the GTO and E_{g2} is negative.

$L_{g \max}$ is the inductance of the gate of the GTO. Manufacturers give the limiting rate of rise of the gate current. We can use this condition $di_{g \max}/dt$ to determine this parameter (for certain manufacturers it is specified).

$$L_{g \max} > \frac{E_{g2}}{\frac{di_{g \max}}{dt}}. \quad (1)$$

Here, E_{g2} is the reverse voltage of the dc source applied to the gate of the GTO, and $di_{g \max}/dt$ is the maximum rate of inverse gate current.

A. Determination of C'_1

When the positive dc voltage source is applied to the gate of the GTO, we have

$$U_{c1}(t) = E_{g1} \left(1 - \cos \left(\frac{t}{\sqrt{L_g C'_1}} \right) \right) \quad (2)$$

at $t = t_d$, $U_{c1}(t_d) = E_1$. Thus

$$C'_1 = \frac{1}{L_g} \left(\frac{t_d}{\arccos \left(\frac{E_{g1} - E_1}{E_{g1}} \right)} \right)^2 \quad (3)$$

with $E_{g1} - E_1 > 0$.

B. Determination of C_2

After t_d , C_2 begins charging, and the voltage $U_{c2}(t)$ is given by

$$U_{c2}(t) = (E_{g1} - E_1) \left(1 - \cos \left(\frac{t}{\sqrt{L_g(C'_1 + C_2)}} \right) \right) + I_0 \sqrt{\frac{L_g}{C'_1 + C_2}} * \sin \left(\frac{t}{\sqrt{L_g(C'_1 + C_2)}} \right) \quad (4)$$

for $t_d < t < t_r$.

Here,

$$I_0 = i_g(t_d) = E_{g1} \sqrt{\frac{C'_1}{L_g}} \sin \left(\frac{t_d}{\sqrt{L_g C'_1}} \right).$$

When $t = t_r$, let $U_{c2}(t_r) = E_{g1} - E_1$.

$$(E_{g1} - E_1) = (E_{g1} - E_1) \left[\sum \frac{(-1)^n}{(2n)!} \left(\frac{t_r}{L_g(C'_1 + C_2)} \right)^{2n} \right] + I_0 \sqrt{\frac{L_g}{C'_1 + C_2}} \left[\sum \frac{(-1)^{n-1}}{(2n-1)!} \left(\frac{t_r}{L_g(C'_1 + C_2)} \right)^{2n-1} \right].$$

We made a second degree approximation because t_r is very small. Thus we have

$$C_2 = \frac{1}{2} \left[\left(\frac{2I_0 t_r}{E_{g1} - E_1} + \frac{t_r^2}{L_g} \right) + \left(\left(\frac{2I_0 t_r}{E_{g1} - E_1} + \frac{t_r^2}{L_g} \right)^2 - \frac{1}{3} \left(\frac{t_r^4}{L_g^2} \right) \right)^{1/2} \right] - C'_1. \quad (5)$$

C. Determination of K

$I(t)$ represents the current of the controlled source, which is a function of K and U_{c2} :

$$I(t) = f(k, U_{c2}(t)).$$

This gives the relation between the gate circuit and the

anode-cathode circuit as follows:

$$I(t) = K \left[\left((E_g - E_1) \left(1 - \cos \left(\frac{t}{\sqrt{L_g(C'_1 + C_2)}} \right) \right) + I_0 \sqrt{\frac{L_g}{C'_1 + C_2}} \sin \left(\frac{t}{\sqrt{L_g(C'_1 + C_2)}} \right) \right) \right] \left(t < \sqrt{L_g(C'_1 + C_2)} \frac{\pi}{2} \right). \quad (6a)$$

When $t > \sqrt{L_g(C'_1 + C_2)} (\pi/2)$, $I(t)$ holds the maximum value because the state of diode 2 is turned off. That is,

$$I(t) = K \left[(E_{g1} - E_1) + I_0 \sqrt{\frac{L_g}{C'_1 + C_2}} \right] \left(\sqrt{L_g(C'_1 + C_2)} \frac{\pi}{2} < t < t_s \right) \quad (6b)$$

We take $I(t) > I_{TGM}$ for consideration of the extreminal case, thus we have

$$K > \frac{I_{TGM}}{(E_{g1} - E_1) + I_0 \sqrt{\frac{L_g}{C'_1 + C_2}}}. \quad (7)$$

D. Determination of C'_1

At $t = t_2$, the reverse voltage of the dc source E_{g2} is applied to the gate of the GTO. C'_1 discharges until t_0 .

$$U_{c1}(t) = (E_{g2} - U_0) \left(1 - \cos \left(\frac{t}{\sqrt{L_g C'_1}} \right) \right) + U_0 \quad (8)$$

with $E_{g2} < 0$.

Here, $U_0 = U_{c2}(t_2) + E_1$. After $U_{c1}(t) < 0$, D is in the on state. This instant is noted by t_0 . From (8) we have

$$t_0 = \sqrt{L_g C'_1} \arccos \left(\frac{-E_{g2}}{E_{g2} - U_0} \right). \quad (9)$$

C'_1 and C'_2 are connected in parallel. The initial current of the inductance L_g is determined by

$$I_{02} = (E_{g2} - U_0) \sqrt{\frac{C'_1}{L_g}} \sin \left(\frac{t_0}{\sqrt{L_g C'_1}} \right). \quad (10)$$

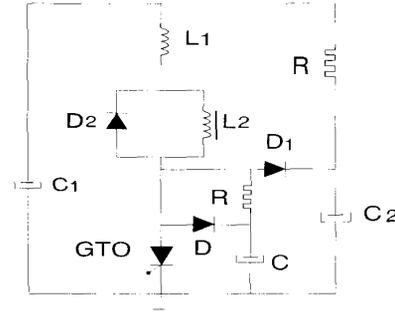


Fig. 4. Testing power circuit.

Using this initial condition, we can obtain the voltage of C_1 :

$$U_{c1}(t) = E_{g2} \left[1 - \cos \left(\frac{t}{\sqrt{L_g C'_1}} \right) \right] + I_{02} \sqrt{\frac{L_g}{C'_1}} \sin \left(\frac{t}{\sqrt{L_g C'_1}} \right) \quad (11)$$

with $t_0 < t < t_s$.

The reverse gate current is

$$i_g(t) = E_{g2} \sqrt{\frac{C'_1}{L_g}} \sin \left(\frac{t - t_0}{\sqrt{L_g C'_1}} \right) + I_{02} \cos \left(\frac{t - t_0}{\sqrt{L_g C'_1}} \right). \quad (12)$$

In fact, $I_{g \max} < I_{TAVM}/3$. The amplitude of the negative gate current is determined by the amplitude of the anode current I_T , the storage time t_s , and the gate negative turn-off gain G . The negative current of gate I_g can be generally represented by a sine function with a frequency $f = 1/(2\pi\sqrt{L_g C'_1})$. At the moment where $\omega t \leq \pi/2$, I_g reaches its maximum value $I_{g \max}$. Considering this physical characteristic, and from (12), we have

$$I_{g \max} = \frac{I_T}{G} = \frac{E_{g2}(t_s - t_0)}{L_g} + I_{02} - \frac{1}{2} I_{02} \left(\frac{t_s - t_0}{\sqrt{L_g C'_1}} \right)^2$$

$$C'_1 = \frac{I_{02}(t_s - t_0)^2}{2 \left[E_{g2}(t_s - t_0) + L_g I_{02} - \frac{I_T}{G} \right]} - C'_1. \quad (13)$$

Here, G is the negative turn-off gain that is equal to I_{TAVM}/I_{GQM} . When $t = t_s$, we have

$$U_{cp} = U_{c1}(t_s) \quad (14)$$

with $t_0 < t < t_s$.

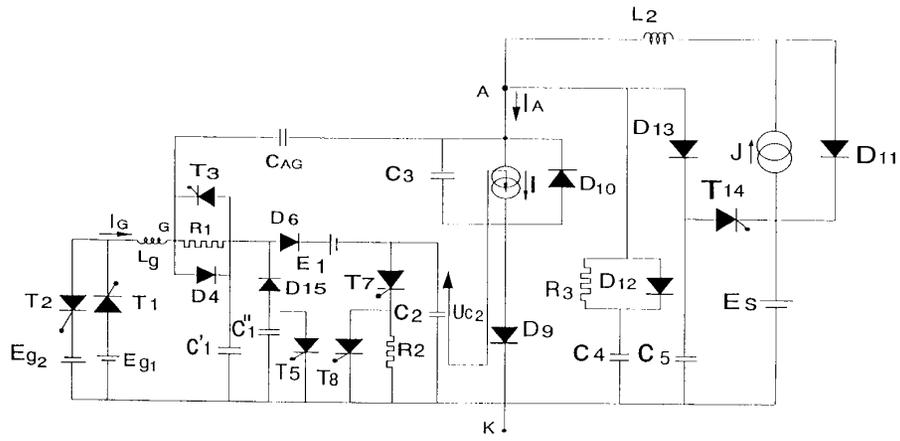


Fig. 5. Simulation circuit.

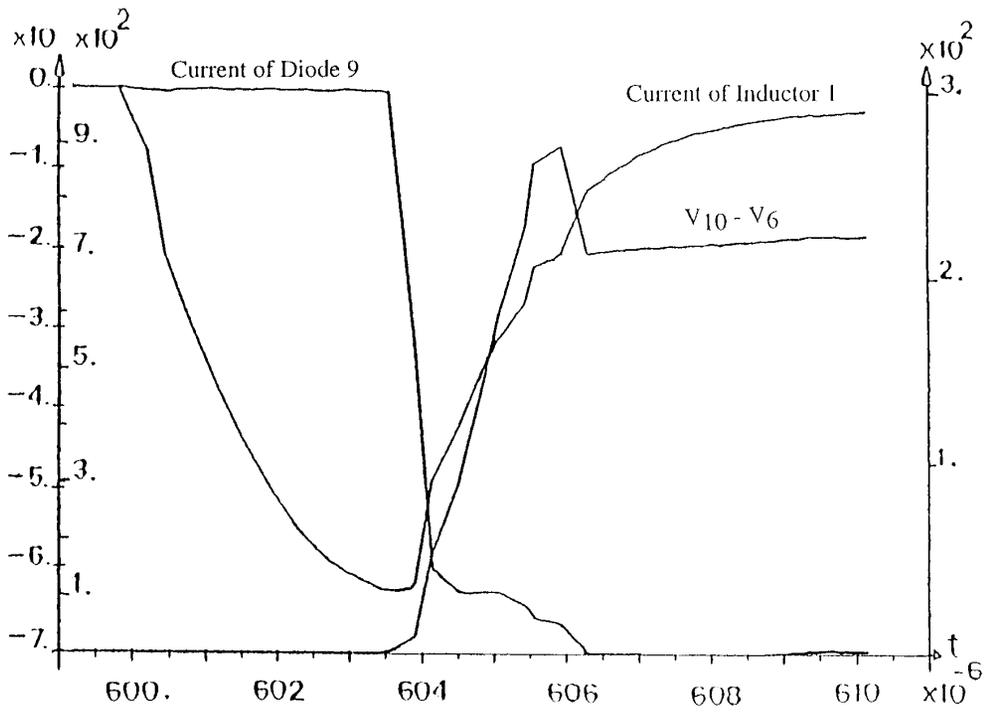


Fig. 6. Simulation results with SICOS.

E. Determination of R_{T3} , R_1 and R_2

After $t > t_s$, the voltage U_{c1} becomes over the voltage U_{cp} , which represents the stored charges in the base area. This means that the GTO goes out from its saturated state. The anode current begins to fall down. Thus T_3 turns on and at same time T_1 turns off. The GTO changes from a small-resistance to a high-resistance zone. From the equivalent circuit, we have

$$i_g(t_f) = \frac{E_{g2} - U_{c1}(t_s)}{L_g} t_f - I_g(t_s) \left(\frac{R_1}{L_g} t_f - 1 \right)$$

At $t = t_f$, $i_g(t_f) = g_1^* I_g(t_s)$, and $0.1 < g_1 < 0.8$. We take $g_1 = 0.4$.

$$R_1 = \left(0.6 I_g(t_s) - t_f \left(\frac{E_{g2} - U_{cp}}{L_g} \right) \right) \frac{L_g}{I_g(t_s) t_f} \quad (15)$$

$$R_{T4} = 0.43 \frac{t_f}{C_2}. \quad (16)$$

After $t = t_f$, the anode current of the GTO is less by of 10% $I_{T,AVM}$. The GTO turns off, and the internal resistance becomes very high. But for the edge zone it is still in the on state. T_4 turns off and the resistance R_2 is inserted. This can well simulate the period of tail time defined by $0.25 U_{c2}(t_f) = U_{c2}(t_i)$. Thus we have

$$R_2 = 0.72 \frac{t_i}{C_2}. \quad (17)$$

F. Determination of C_3

$$C_3 = \frac{K}{U_{DRM}} \left((E_{g1} - E_1) \left(t_r - \sqrt{L_g(C_1 + C_2)} \sin \left(\frac{t_r}{\sqrt{L_g(C_1 + C_2)}} \right) \right) + I_0 L_g \left(1 - \cos \left(\frac{t_r}{\sqrt{L_g(C_1 + C_2)}} \right) \right) \right) \quad (18)$$

with $t_d < t < t_r$.

C_{AG} is a parasitic capacitor given by the manufacturer. We consider that $C_{AG} = (\text{from } 0.01 \text{ up to } 0.005) * C_3$ if it is not given.

VI. EXAMPLE

For the GTO, type AEG G200 A 1200 V, 300 A, the properties are as follows:

$$\begin{aligned} t_{gt} &= 1.65 \mu\text{s} & t_r &= 1.4 \mu\text{s} & U_{DRM} &= 1200 \text{ V} \\ I_{TGM} &= 600 \text{ A} & t_s &= 3.6 \mu\text{s} & t_f &= 0.6 \mu\text{s} \\ t_i &= 6.5 \mu\text{s} & I_{TAVM} &= 300 \text{ A.} \end{aligned}$$

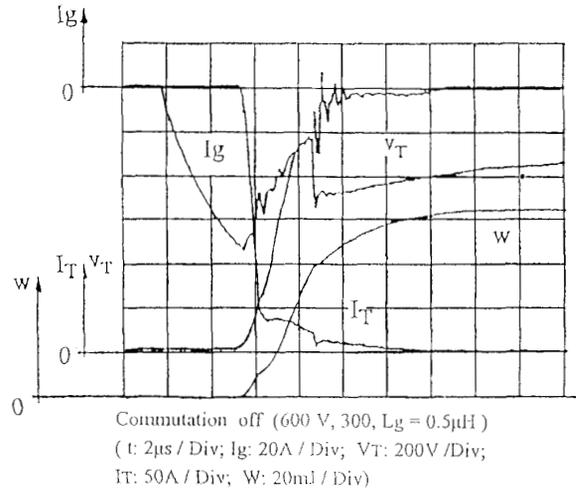


Fig. 7. Experimental results.

The power circuit used for testing the model of the GTO is given in Fig. 4 [6]. The parameters of the circuit are as follows:

$$L_1 = 25 \mu\text{H}, \quad L_2 = 2.5 \text{ mH}, \quad C_2 = 12.5 \mu\text{F}, \quad R = 9 \Omega$$

$$C = 0.5 \mu\text{F}, \quad C_1 = 2 \text{ mF}; \quad L_g = 0.5 \mu\text{H}.$$

The equivalent circuit of this power circuit is given in Fig. 5. Here, $E_{g1} = 15 \text{ V}$, $E_{g2} = -15 \text{ V}$. The parameters are determined from (1) to (18).

The parameters of the circuit are as follows:

$$L_g = 0.5 \mu\text{H} \quad C_1' = 0.224 \mu\text{F} \quad C_2 = 5.1 \mu\text{F};$$

$$C_1'' = 18 \mu\text{F} \quad R_1 = 0.4 \Omega \quad R_{T8} = 0.051 \Omega$$

$$K = 46.$$

The SICOS program (Simulation CONVERTISSEUR STATIQUE) has enabled us to simulate the equivalent circuit of the GTO. The results of the simulation are given in Fig. 6. The current of diode 9 and the current of the inductor 1 represent, respectively, the anode current and the gate current of the GTO. $V_{10} - V_6$ is the anode-cathode voltage of the GTO. Fig. 7 presents the experimental results [6]. A comparison of the two figures shows that the results of the simulation are similar to the experimental results. Fig. 8 is another case of a GTO in the on state, the signal of the gate of the GTO being zero. When the anode current becomes inferior to the maintain current, the GTO turns off. The step time is $0.08\text{E-}6 \text{ s}$.

VII. CONCLUSION

Gate turn-off thyristors, called GTO's, are fast switching power semiconductors that can sustain high currents

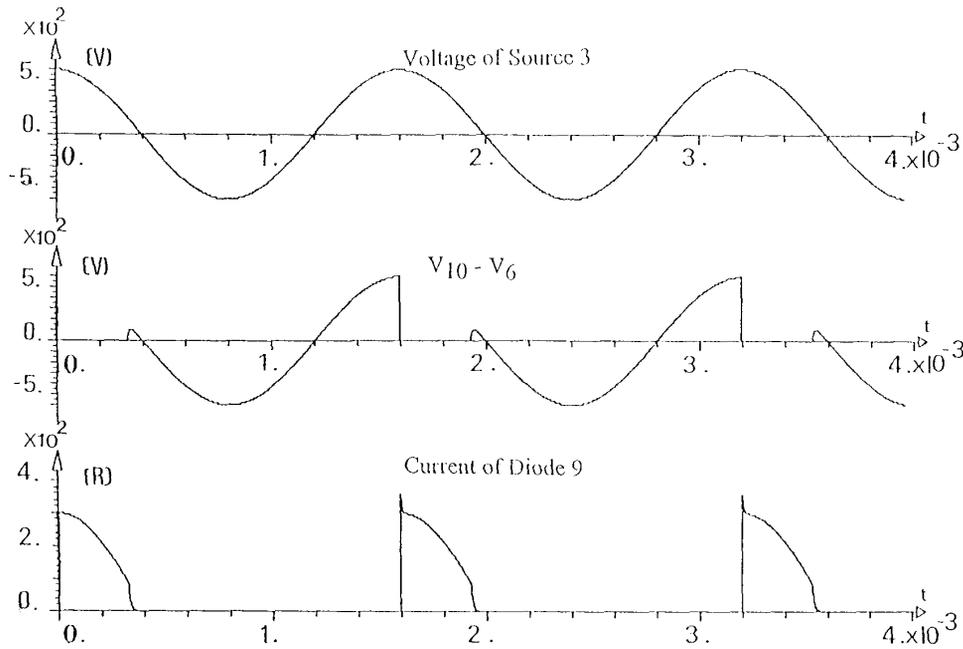


Fig. 8. Behaviors of holding current of GTO's numerical model.

and voltages. This property makes them readily applicable in forced-commutation inverter circuits. Models for such components are thus of primary importance in power circuit simulation. In this paper, we have given a new concept of the controlled switch. Using this model, a GTO equivalent circuit is developed. The simulation with SICOS or success [8], proves that this numerical model can be used to simulate dynamic and static characteristics. Since this model is completely based on the characteristics given by the manufacturers, it is very easy to use. Only one controlled-current source is employed so that the simulation time is very short. In the example given, the simulation time is only 6 min with the Hewlett Packard 9000/400 computer. Another advantage of this model is that it can be applied in almost all simulation programs for power circuits. Works are being made to minimize the number of components.

REFERENCES

- [1] R. L. Avant, F. C. Lee, and D. Y. Chen, "A practical SCR model for computer aided analysis of ac resonant charging circuits," in *IEEE Power Electronics Specialists Conf. Rec.* 1981, pp. 232-234.
- [2] M. Kurata, "A new CAD model of a gate turn-off thyristor," in *IEEE Power Electronics Specialists Conf. Rec.* 1974.
- [3] G. N. Revankar and P. K. Ivastava, "Turn-off model of an SCR," *IEEE Trans. Ind. Electron.*, IECI22, pp. 507-510, 1975.
- [4] C. W. Lee and S. B. Park, "Determination of thyristor reverse recovery current parameters," *IEEE Proc.*, vol. 135, pt. B, no. 2, Mar. 1988.
- [5] J. P. Pascal, "Etude de Circuits d'aide à la commutation de thyristor GTO montés en série pour des application à la traction ferroviaire," These de Doctorat d'Etat ès Sciences Physiques, l'Université Pierre et Marie Curie, 1986.
- [6] R. Lallemand, "Caractérisation des GTO," Rapport INRETS, no. 8, July 1986.
- [7] W. McMurray, "Simulation of switching transistor in GTOs using SPICE," in *Proc. Power Conv. Int.*, Oct. 1986.

- [8] C. Batard, H. Meynard, H. Foch, and Massol, "Circuit-oriented simulation of power semiconductor using successful application to diodes and bipolar transistors," *EPE-Firenze*, vol. 1, pp. 1068-1073, 1991.



Da-Guang Ni received the B.S. degree in electrical engineering from the Dalian Institute of Railway Technology, Dalian, China, and the M.S. degree in electrical engineering from North-East Heavy Machinery Institute, Qin Huang Dao, China, in 1982 and 1988, respectively. He is presently studying for the Ph.D degree in the department of electrical engineering, Ecole Centrale de Lyon, Lyon, France.

Since 1987 he has worked as a Lecturer in Electrical Engineering Department of the Dalian Institute of Railway Technology and in 1990, he did research in Direction des Etudes et Recherches de Electricité de France (EDF). His current research interests are modeling of power electronic devices, design and construction of semiconductor high-power switches and power converters, application of semiconductors in power networks, and analysis of power networks.



Gerard Rojat was born in Caraman, France, on May 6, 1946. He received the M.S. degree and the Doctor's degree in electrical engineering from Paul Sabatier University, Toulouse, France in 1974, and in 1980, the "Docteur d'Etat" from Claude Bernard University, Lyon, France.

Since 1974, he has been with Ecole Centrale de Lyon, Ecully, France as a professor, where he teaches power electronic and speed variation of electrical machines. His research interests are in the areas of power electronics and electromag-

netic compatibility.



Guy Clerc was born in Libourne, France, on November 30, 1960. He received the Engineer's degree and the Doctor's degree from the Ecole Centrale de Lyon, France, in 1984 and 1989, respectively, both in electrical engineering.

From 1989, he was a Lecturer in the Ecole Centrale de Lyon. He taught "numerical control of electrical machines" and electrical engineering. He carried out researches on static apparatus and control of induction machine. He has authored several papers on static apparatus (GTO cascade and IGBT switches), numerical drives of static circuit breakers and fault prediction.



Jean-Pierre Chante received the Professor doctorate in 1981 from Claude Bernard University of Lyon.

He managed a research team until 1986 in the field of power components. Since 1986, he has been managing the team "Composants de Puissance et Application" part of the CEGELY (URA CNRS no. 829) and "Centre Interuniversitaire de Microélectronique de Région de Lyon."