# SPECS : A serial protocol for experiment control system in LHCb

D. Breton, D. Charlet, P. Robbe, I. Videau

# SPECS : A SERIAL PROTOCOL FOR EXPERIMENT CONTROL SYSTEM IN LHCB.

D.Breton, [1]D.Charlet, P.Robbe, I.Videau
*LAL ,Orsay France*

## Abstract

This document describes the SPECS protocol and its implementation. The SPECS is a 10 Mbit/s serial bus, designed to be simple, cheap, reliable and to work in radiation sensitive environments. It is mainly used to download and read back the configuration of the electronics located on the detector. It is made of Master PCI boards and slave daughter boards, provides I2C, JTAG and parallel interfaces for the users, and is delivered with a software patch.

## General presentation

The LHCb sub-detector electronics is organized around the detector in crates or on individual boards which require a configuration access to load or read different types of information. These operations will be driven from a computer located in the control room, roughly 130 meter distant from the various front-end crates. Therefore, the experiment requires a configuration bus, able to communicate properly on over a 130 meter line, with a unique master, and up to 32 slaves.

In such a configuration, the master card would be located in the control room, which is not exposed to radiation, and the slave would be implemented close to or on the detector electronics boards.

A serial, synchronous and bi-directional bus has thus been developed. The fact of choosing to have two signals in each direction simplifies the receiver part which does not have to extract the clock from a unique mixed line and to encode it back for the return path. Moreover, the slave does not need any external clock to be operational for write operations, which makes the system mostly insensitive to its environment.

## [2]Radiation environment

For radiation zones, hardness to the single event latch-ups (SEL), single event upsets (SEU), and single event transients (SET) are required. This point has to be considered carefully, and the design of the slave chip ensures that the registers and state machines are protected by appropriate redundancy. The single event latch-up sensitivity however depends on the technology used. For this reason we have tested and chosen some specific ones. All the components have thus been tested either by us or by other laboratories up to 30kRads.

## Data rate

The SPECS transfer is performed at 10 Mbit/s. The effective data rate actually depends on the type of transfer, block or word transfer. For block transfers the rate can reach 984KB/s whereas it is of 285KB/s for 16-bit transfers.

## Safety of the information

Transfers of long frames are more prone to errors, while short frames will slow down the effective speed by introducing too many control bytes compared to the useful data. Therefore a maximal length for SPECS frames of 256 bytes was chosen as a reasonable compromise.

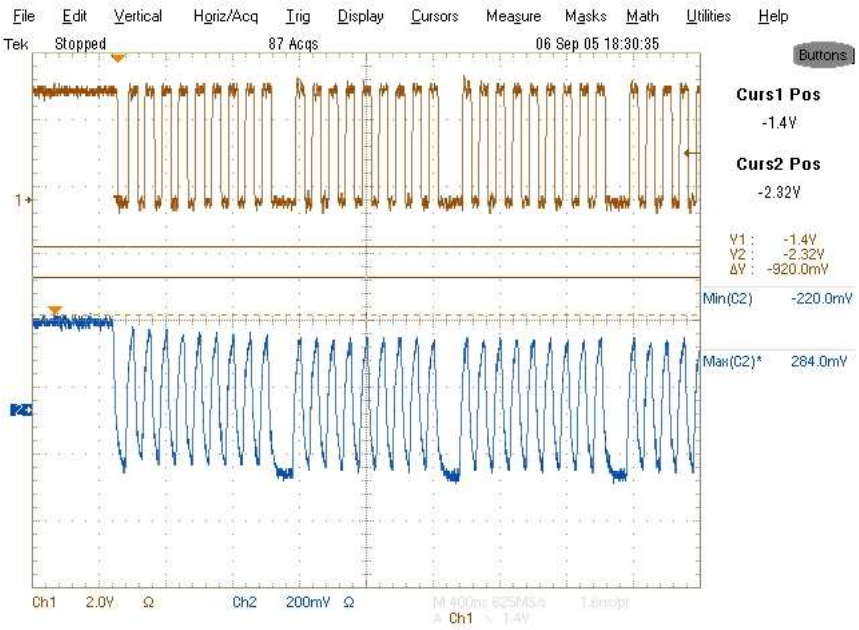
SPECS bus has no error correction, but 2 error detection systems:

- Four bits of redundancy follow the header of the frame, which contains the address of the slave and other parameters. If an error is detected, the slave ignores the whole message, and sends an error interrupt to the master straight away.
- One byte of redundancy is sent at the end of the frame, and allows detection of a data error. If an error occurs, data is loaded, but the concerned slave mentions it to the master, sending an error interrupt straight away.

[1]Corresponding author

### Physical link

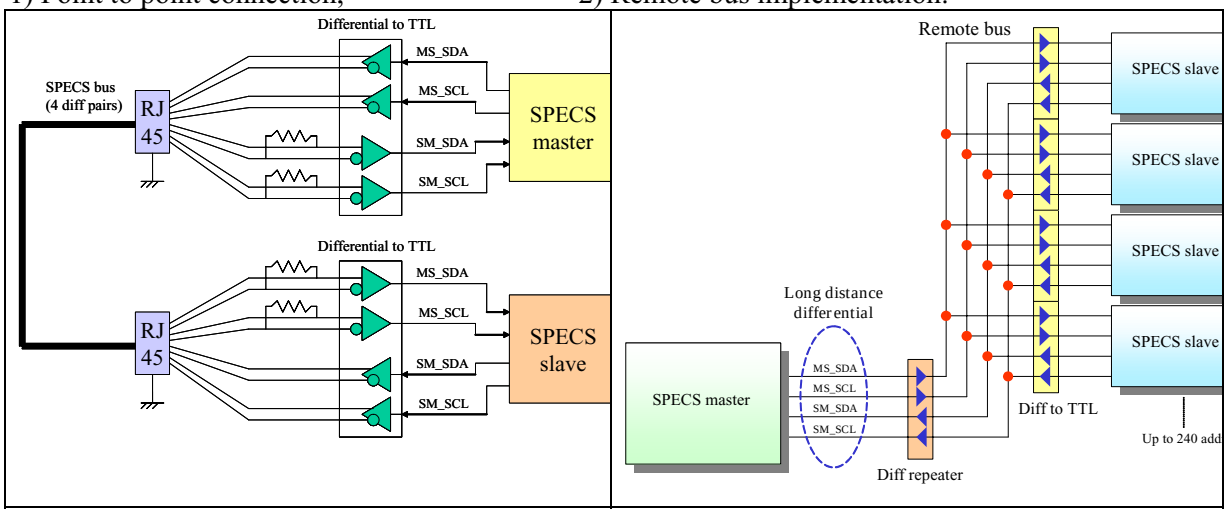
The protocol requires 8 copper links (4 pairs). The technology is the BLVDS. At a 10 Mbit/s rate and for 130m of CAT 6 cable, a pole-zero cancellation of the cable skin effect is mandatory. The BLVDS has excellent qualities for such an implementation. Sent on twisted pair cables, it can propagate fast signals (more than 150 MHz) along relatively long distances thanks to its 10 mA output current. Moreover, it can support a large number of slaves on the same line. The 8-pin RJ45 connector was chosen for the interconnections. It is a cheap and compact standard, which can be associated with Ethernet type cable. These associated cables are twisted pairs surrounded by a shield. All of these choices allow a very good respect of signal integrity as can be seen on the plot below at the extremities of a 130m link.




## THE SPECS PROTOCOL

### General description

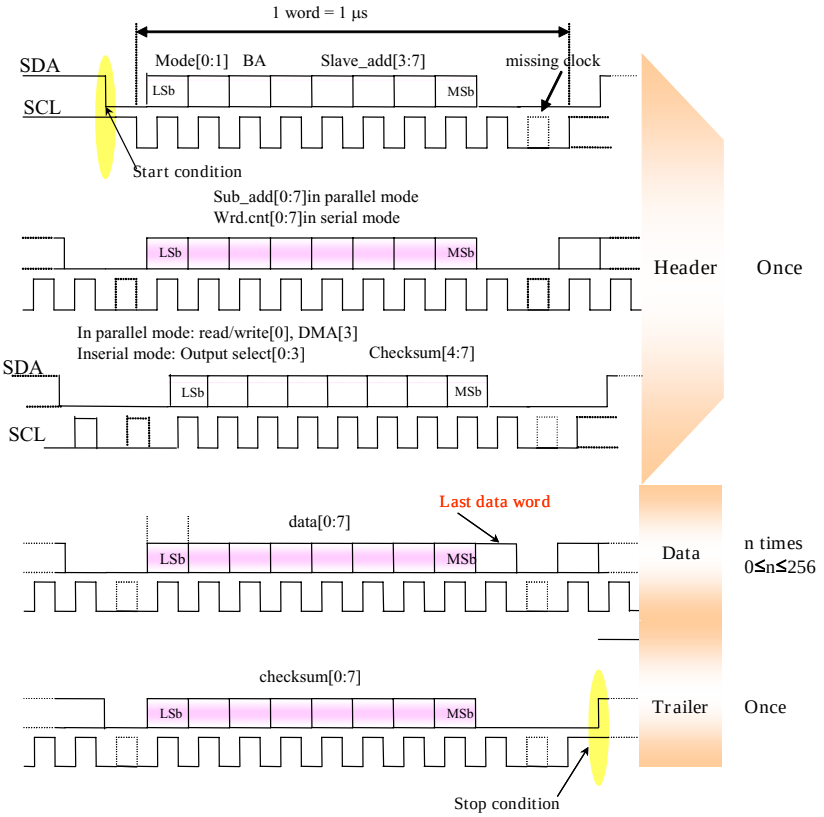
The SPECS is a single master, multi slave serial bus. It allows communication between a unique master and up to 32 slaves (limit fixed by the address range), at a 10 MHz rate, thanks to 4 different unidirectional lines. These lines called MS_SDA, MS_SCL, SM_SDA, SM_SCL are the data and clock lines, from master to slave, and from slave to master respectively;
The SPECS can be implemented in two different ways:
1) Point to point connection, 2) Remote bus implementation.



The first implementation allows the user to connect a master to a single slave over a long distance. If the number of slaves to access is important and the mean bandwidth small, it might be more appropriate to use the remote bus implementation. The latter offers the possibility to drive about 32 slaves at a long distance with a single master. It makes use of a remote differential repeater to ensure the signal integrity. This solution was chosen for the calorimeter electronics of LHCb, through distribution of the bus on the crate backplanes.

## SPECS Data Frame

The standard data transfer frame is shown below. Each word has a specific role in the protocol. The order of the bits transferred is always least to most significant bit (20 to 28). The 9th bit (bit 28) tags the last data word of the frame, and is set to zero otherwise. The 8 remaining bits are used to transfer different types of data.




The frame is composed of a fixed size header, a variable size data block, and a fixed size trailer.
The header consists of 3 8-bit words:
The first word contains 2 bits for the mode (I2C, JTAG, parallel bus, register), one bit for the broadcast address if appropriate, and 5 bits for the slave address.
The second word gives the slave sub-address in parallel mode transfers or the word- count (number of words to transfer) in serial mode, i.e. I2C and JTAG
The third word also has a different contents depending on the mode:
in parallel mode it contains a read/write bit[0], a DMA bit [3] and the 4-bit header checksum. Bits [1] and [2] are not used.
in serial mode the first four bits give the output select (internal/external I2C and JTAG addresses) and the 4 most significant bits the header checksum.
The data block contains a series of 0 to 256 words, according to the transfer to be performed. A more precise description follows in the next section.
Finally, the trailer contains the checksum of the data block. The calculation of the checksum is:

$$trailer\_checksum[7:0] = \sum_{i=0}^{number\_of\_data\_words-1} data[i][7:0]$$ where the sum operator is 'Xor'.

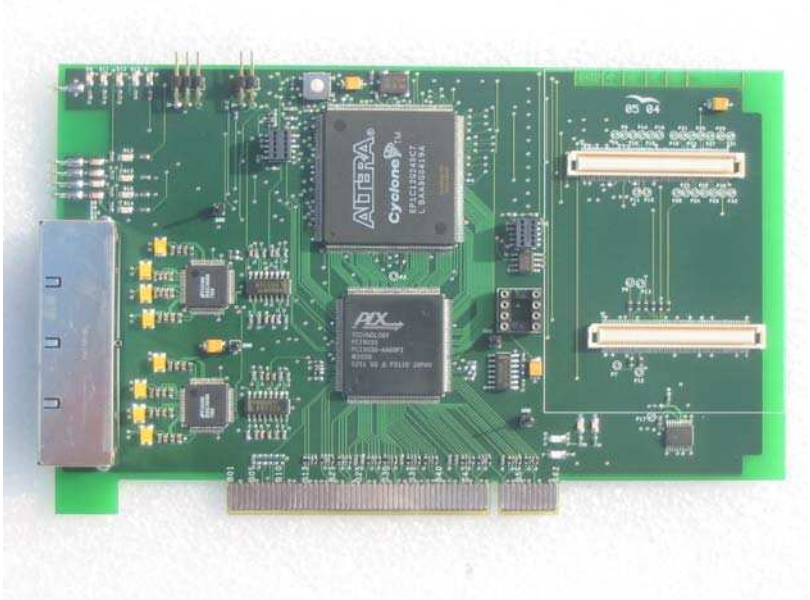
## SPECS Interrupt Frame

The interrupt frame has to be as short as possible in order to reduce the probability of conflict, while providing the minimum relevant information to the master. The interrupt frame consists of a single word frame including only the address of the sender. This way the master can distinguish the slave who has generate the interrupt and react in consequence.

## Communications

The master always takes control of the bus to perform the required operations. The two possible operations for the master are the write and read accesses.
A slave normally does not take control of the bus without being requested to do so by the master. After a write command, it executes the operation, but a priori does not reply anything. No answer means that the transfer was successful. After a read command, the slave takes control of the bus to provide the requested data.
In case of a suspicious transfer, the slave sends an interrupt message to the master, both in read and write mode. The interrupt is sent after a known delay following the master's command.
The slave can also take control of the bus without any occurrence of a command from the master. This is the case when a 'user interrupt' is requested from the slave's host board. Then, totally asynchronously, the slave takes control of the bus to send the user interrupt to the master.
In any case, before the master or a slave can take the control of the bus, they check that no transfer on the SM (slave to master) line is being performed. If any activity is detected, the action is delayed until the end of the current transfer. Then, when the SM bus becomes idle, the slaves wait for 1 or 2 clock cycles, and the master waits for 3 clock cycles before they can take control of the bus. This gives the right of way to the slaves, which may have to reply something before the master sends another command. Moreover, the wait time for the interrupt is shorter than for the other commands, which gives it higher priority.
Finally, to prevent any device on the bus from remaining in an abnormal state after a wrong transfer, the master has a timeout counter. Since no transfer can be longer than 3+256+1 words (header size + maximum data size + trailer size), which corresponds to 260 µs, any continuous activity lasting more than about 300 µs will reset the state machines of all devices.

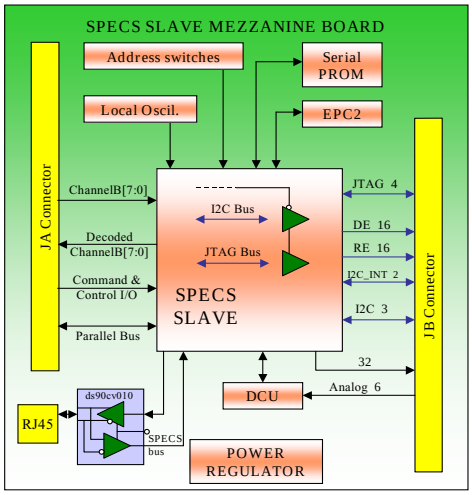
## SPECS multi-master board

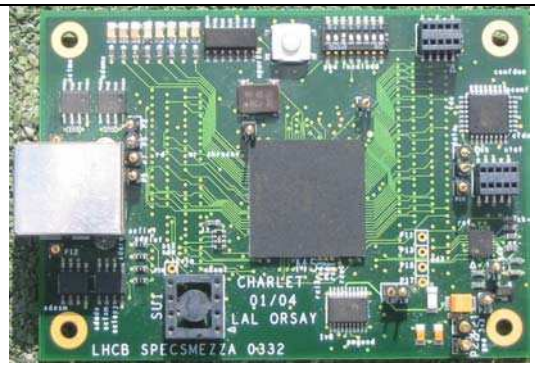


The SPECS master board hosts 4 SPECS masters. The SPECS master is implemented on a standard 32-bit 33 MHz PCI board, which can be plugged into a PC. In order to offer an easy setup for the test benches, the board also includes an internal SPECS slave, which allows the user to benefit from both JTAG and I2C local output capability. The heart of the system is integrated within an ALTERA CYCLONE FPGA and the PCI interface is performed by a PLX9030 chip, each of them having its own configuration EEPROM. For the driver part, we use the DS92LV090 driver with the voltage RC pole-zero cancellation. For the receiver part, due to the long distance link, we use receivers with high common mode input voltage range (-2 to 4.4V), and low differential input thresholds ( < 50mv).

## SPECS slave mezzanine general description

An mezzanine daughter-board has been developed to house the SPECS slave, and to provide all the described functionalities of the SPECS Slave chip through 2 SMC connectors. The mezzanine board also provides most of the necessary service functions for the sub-detector front-end electronics. The goal is to avoid putting unnecessary electronics in the radiation sensitive area.
The mezzanine can be configured in master mode or in slave mode. In master mode, the mezzanine can deal with 2 SPECS busses:
One point to point long distance bus. This bus is implemented with RJ45 connectors on the mezzanine, which permits a direct connection, without any additional component, to the master through an Ethernet cable. In this configuration, called master mode, we can connect up to 31 other slaves, using the on-board bus located on the SMC connector. The connection can be either a long distance one making use of external drivers or a short distance one on the same PCB in respect of the signal integrity rules.
One multi-drop SPECS bus, located on the SMC connector. On this bus we can directly connect others mezzanine in slave mode, in respect of the signal integrities rules, or generate other long distance SPECS links by using additional drivers.
In slave mode, the mezzanine manages only the SPECS bus located on the SMC connector. As for the master mode, other mezzanines can be connected at long or short distance.
The two different modes of the mezzanine, master or slave, are selected digitally through a dedicated SMC pin.



## List of the main features of the mezzanine board:

One long distance point to point differential SPECS interface (coming from the SPECS master).

One unipolar SPECS local interface for multi-load bus applications.

Three serial bus: 1) local I2C 2) long distance I2C 3) JTAG bus.

16 JTAG or 15 I2C chip-select control bits and direction control bits for external drivers. .

One parallel bus offering 16 data bits and 8 address bits.

One decoder for the channel B of the TTCrx, decoding: A) L0 front-end reset, B) L1 front-end reset, C) L1 event ID reset, D) Calibration pulse type 0, which can be delayed with a programmable counter.

One 32-bit static register to control or read back the local environment. The bits [31..0] can be individually configured either in output or in input mode.

One reset signal. This output can be triggered without the need of any clock on the board.

One local 40MHz oscillator. It is also provided as an output of the mezzanine and can be enabled by the software.

One PROM which will allow the ECS system to obtain some information about the front-end element housing the mezzanine. It will be mounted on a socket.

One DCU chip with 6 ADC channels of 12-bit resolution.

### SPECS slave chip

The slave is designed as a portable VERILOG code and will be eventually physically integrated inside an ACTEL flash PGA. With this technology, the slave will be SEL immune, and will also be made SEU immune, provided the internal registers will appropriately be protected by triple voting techniques, and state machines will use one-hot state. Moreover, to ensure a high reliability of the decoding of the SPECS commands, there will be no state machine in the SPECS receiver part. In addition, all commands (and in particular all resets) will be generated without using any local clock but only the SPECS lines. This may for instance allow the user to reset the TTCrx through SPECS if necessary. The chip will also be reasonably radiation tolerant, up to 10 krad (with some safety margin, the ACTEL chip having been tested up to 40 krads) over the lifetime of the experiment. It can then be placed at most locations where we foresee to have electronics, except in or near the Vertex Locator tank. The chip is an ACTEL APA150.

### Software

All the tools needed to use the SPECS system have been developed both for the Windows and Linux operating systems. They consist in 3 different software levels:

1) A PCI driver, developed by the PLX Company, enables communication with the PLX9030 chip on the SPECS master board via the PCI bus.

2) A SpecsLib library computes the different frames for all kind of mezzanine access (Parallel, I2C, JTAG, ...), for write and read operations.

3) A SpecsUser library decodes the frames into useful data values, manages the status for the PCI accesses, and handles the more complex accesses like JTAG, I2C, DMA, and the communications with the on-board ADC (DCU).

All these components are also interfaced to the PVSS architecture.

## References

[2]LHCb note. LHCb 2002 - 021 et LHCb 2002 -072

.