HIGH QUALITY FACTOR COPPER INDUCTORS INTEGRATED IN DEEP DRY ETCHED QUARTZ SUBSTRATES

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ABSTRACT

This paper reports on an inductor fabrication method capable to deliver high quality factor (Q) and high self resonance frequency (SRF) devices using quartz insulating substrates and thick high-conductivity copper lines. Inductors are key devices in RF circuits that, when fabricated on traditional semiconductor substrates, suffer from poor RF performances due to thin metallization and substrate related losses. Many previous works revealed that RF performances are strongly dependent on the limited metallization thickness and on the conductivity of the substrate. In this paper we demonstrate a new fabrication process to improve the Q factor of spiral inductors by patterning thick high conductive metal layers directly in a dielectric substrate. Moreover, we develop and validate accurate equivalent circuit modeling and parameter extraction for the characterization of the fabricated devices.

1. INTRODUCTION

Modern applications using RF ICs demand higher working frequencies, low noise and low power consumption, which require high Q-factor and high SRF passive components.

Our study concerns integrated inductors for which low RF performances limit their application in RF ICs. Typical values are $Q_{MAX} < 10 - 15$, with a peak bellow 2 GHz and self-resonant frequencies below 3 – 5 GHz [1]. The origin of their limited performances is well known and reported: inductors mainly suffer from substrate related RF losses due to low-resistivity underneath substrate, low metal tracks conductivity due to thin layers resistive losses and capacitive parasitics due to spiral tracks / substrate coupling.

Many works have already been done and a lot of solutions have been investigated to increase these performances. For reducing substrate-related losses, high-resistivity silicon or SOI substrates have been used [2], insulating the inductor from the silicon substrate [3]. Etching a cavity underneath the inductor have also been investigated [4].

Even if inductors with reasonable Q factors and resonant frequencies can be manufactured on top of low-resistivity silicon wafers [5], covering most of the telecommunication applications, the nature of the substrate remains a recurrent limitation. In the early 2000, Yoon et al. [6] investigated the RF performances of the same inductor design fabricated on both silicon and glass substrates. On-glass inductor provided a significant increase in both quality factor (45%) and self resonant frequency (2.5 times higher) due to a relatively large decrease in the parasitic capacitance to the substrate.

We used new inductive coupled plasma (ICP) etcher dedicated to dielectrics anisotropic deep dry etching in order to explore a new technique based on patterning the inductor directly in a quartz substrate. The main advantage of this technique is the high resistivity of the quartz (2.10^{14} Ω cm @ 20 °C), which reduces dramatically the substrate-related RF losses.

2. FABRICATION PROCESS

Fig. 1 shows a schematic cross section view of the technology steps used to fabricate thick copper spiral inductors embedded in a quartz substrate. A 2 μm sputtered amorphous silicon film is used as hard mask for the etching of the quartz (fig. 1a). This a-Si hard mask is patterned by thin-resist photolithography followed by a SF_6 / C_4F_8 dry plasma etching step (fig. 1b). The quartz substrate is then patterned by C_4F_8 / CH_4 / Ar plasma etching step performed in a state-of-the-art Alcatel AMS 200 DSE ICP dry etcher (fig. 1c). After stripping off the amorphous silicon mask (fig. 1d), the quartz mould is cleaned in a piranha bath (H_2SO_4 / H_2O_2) and receives 0.1 μm sputtered chromium as adhesion layer and a 0.2 μm sputtered copper as seed layer (fig. 1e). The mould

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is filled out with 4.8 µm of high conductive electroplated copper (resistivity = 2.0 µΩ cm, fig. 1f). Copper lines are then defined by a damascene approach using a high-removal rate chemical-mechanical polishing receipt (CMP) [7] (fig. 1g). The CMP stops at the top chromium layer which is cleared in very selective chromium to copper wet etch bath (fig. 1h).

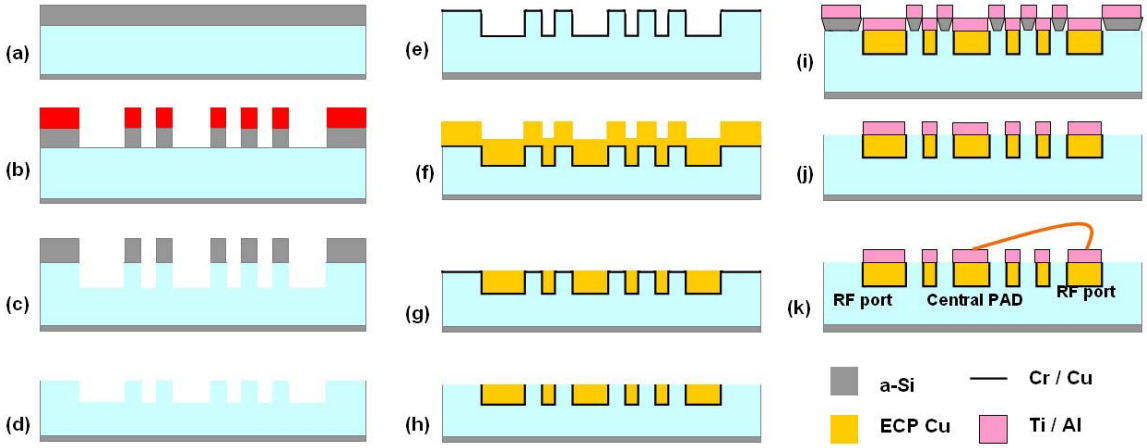

Fig. 1: Schematic cross section view of the coil fabrication process flow: (a) a-Si deposition (PVD), (b) a-Si dry etching, (c) Quartz dry etching, (d) a-Si mask strip, (e) Adhesion and seed layers deposition (Cr / Cu, PVD), (f) Cu electroplating, (g) Chemical mechanical polishing, (h) Top Cr wet etching, (i) Lithography and protection layer deposition (Ti / Al), (j) Lift-off, (k) Gold wire bonding.

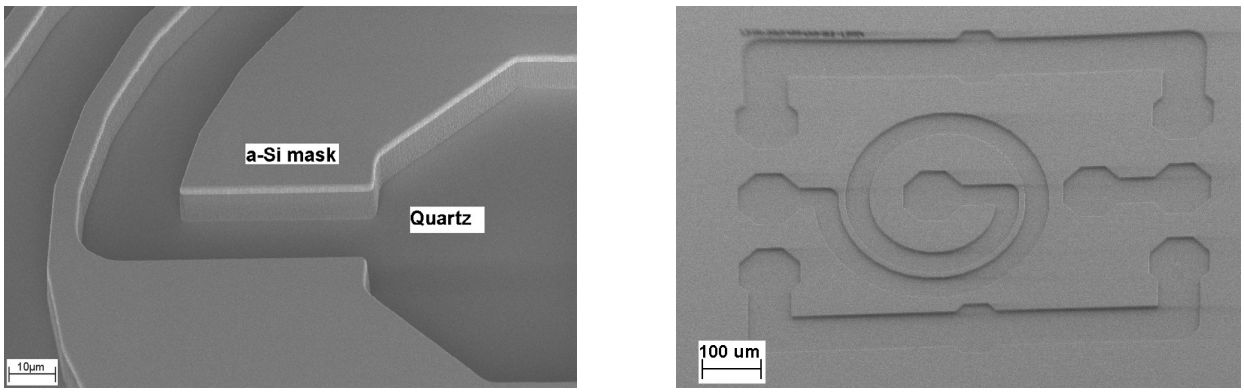

Fig. 2: SEM closed view of a 4 µm deep dry etched quartz inductor mould (40 µm track width and 8 µm track spacing).

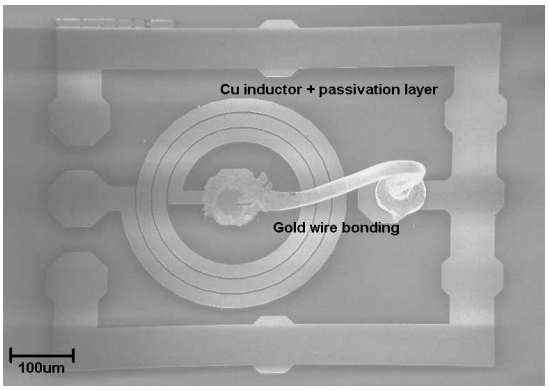

Fig. 3: View of a fabricated 3-turn circular spiral inductor (400 µm outer diameter, 40 µm track width, 8 µm track spacing).

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A protection layer is then defined in order to avoid copper oxidation and to have good electrical contacts to the devices. The protection is composed of 0.2 µm titanium and 0.6 µm of aluminum layers deposited successively in the same multi-target evaporator system, which avoids the first film to be exposed to air (fig. 1i). The protection layer is patterned by lift-off process, using reversal thin-resist (fig. 1j). Finally, connections are established by bonding a 25 µm diameter gold wire between the inductor central pad and the lateral RF port (fig. 1k).

Fig. 2 shows scanning electron microscopy (SEM) pictures of a quartz etched mould. C_4F_8 / CH_4 / Ar plasma etching is a very selective process (>20) that provides very vertical walls [8]. Quartz mould is also very well defined.

A SEM photo of a final fabricated device can be seen in fig. 3.

3. RESULTS

RF electrical characterization was performed using full 2-port S-parameter measurements in a microprober equipped with an HP 8719D vector network analyzer and Cascade Microtech RF ground-signal-ground probes (GSG). The RF setup is calibrated in the range of frequencies from 0.05 to 13.5 GHz using an *Impedance Standard Substrate* with SOLT references (short-circuit, open, load and thru). Measured S-parameter data are transformed into Y-parameters and inductance and quality factor of the devices are calculated from the equivalent 1-port impedance of the device as [1]:

$$L = \frac{imag\left(\frac{1}{y_{11}}\right)}{2\pi f} \qquad \text{(Eq.1), and}$$

$$Q = \frac{imag\left(\frac{1}{y_{11}}\right)}{real\left(\frac{1}{y_{11}}\right)} \qquad \text{(Eq.2),}$$

Where L is the inductance, Q is the quality factor, f is the measurement frequency and $1 / y_{11}$ is the equivalent complex impedance of port 1 when port 2 is connected to the ground [1]. These formulas are commonly used for isolated inductors working below the resonant frequency. The resonant frequency is defined when the expression for Q (eq. 2) goes to 0.

In this paper, we analyze 2 devices of 3.8 and 9.0 nH nominal inductances that have been fabricated and characterized in the 0.05 – 13.5 GHz frequency range. Dimensions and calculated inductance of each device are summarized in table 1. Expected inductance values are calculated following the current sheet method presented in [9]. The thicker layer used in this work with respect to [9] explains a reduction of a few percent in the inductance values with respect to the predicted ones (inductance decreases with both increasing track width and thickness, but must of practical formulae neglect the thickness dependency).

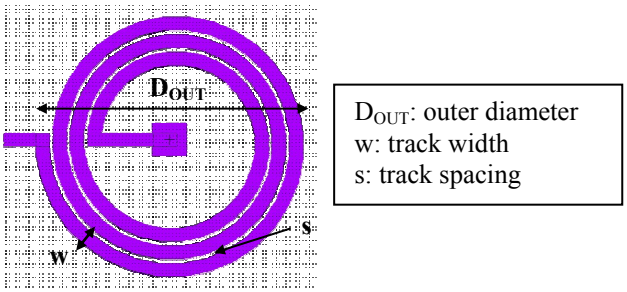

Fig. 4: Schematic view of a 3-turn circular inductor and its main geometrical parameters.

	L_1	L_2
D_{OUT} (µm)	800	800
w (µm)	20	40
s (µm)	12	12
form	octagonal	circular
# of turns	1.5	3
$L_{(PREDICTED)}$	4.3 nH	9.3 nH
$L_{(MEASURED)}$	3.8 nH	9.0 nH

Table 1: Dimensions and inductances of two analyzed inductors.

Figs. 5 and 6 show respectively the extracted L-values (eq. 1) and Q-factors (eq. 2) of these 2 inductors.

We have used a broadband RLC equivalent circuit of a spiral inductor in order to model the measured parameters. Fig. 7 shows the equivalent 1-port circuit [1] and the values of the parameters extracted from the measurements using a dedicated procedure (non-linear least squares fit on the S-parameter and on impedance data). The L-Q plots for this model are also shown in figs. 5 and 6.

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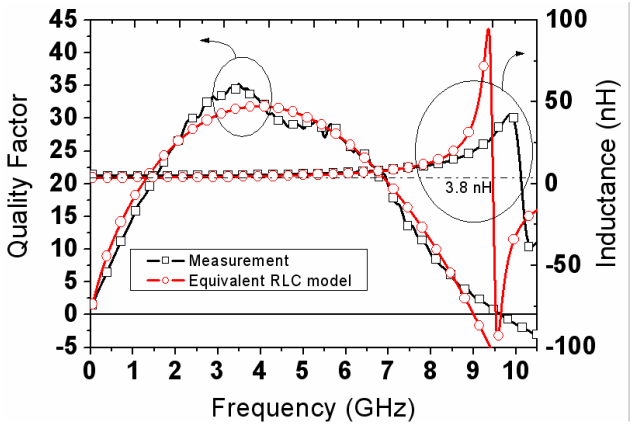


Fig. 5: Extracted inductance (eq. 1) and Q-factor (eq. 2) vs. frequency for the 3.8-nH device (L_1).

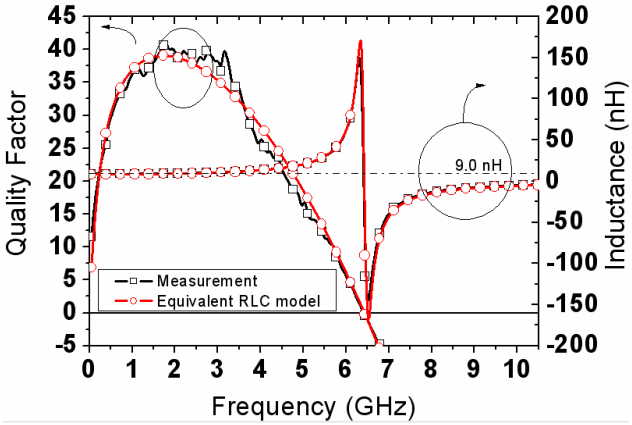
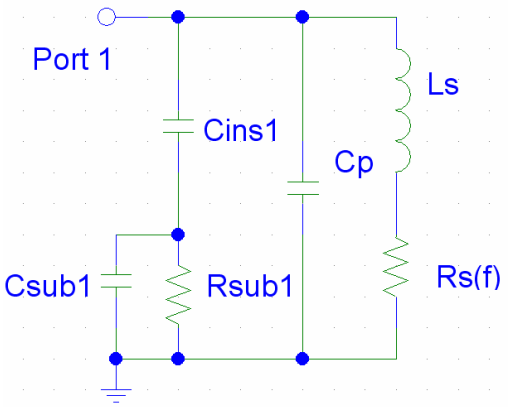


Fig. 6: Extracted inductance (eq.1) and Q- factor (eq.2) vs. frequency for the 9.0 nH circular inductor (L_2).

In the model of fig. 7, R_S accounts for the series resistance of the metal tracks and is dependent of the frequency in the form $R_S(f) = R_{DC} + a\sqrt{f} + bf$ where R_{DC} is the low frequency resistance and ***a*** and ***b*** are constants depending on the device geometry that accounts for the skin and proximity effects. These effects increase the resistance as function of the frequency [10]. C_P is the parasitic parallel capacitance that comes mainly from the capacitive coupling between adjacent inductor tracks. C_{INS1} and C_{SUB1} accounts for the parasitic capacitances between the measurement ports and between the spiral tracks and the backside ground of the wafers. R_{SUB1} accounts for the resistive losses in the substrate, due to the substrate conductivity as well as to eddy currents induced in the substrate by the magnetic field of the inductor. Its value ranges from typically some ohms to hundreds of ohms when the spiral is designed on top of low-resistivity substrates. This resistance decreases the peak quality factor as well as the self resonant frequency. For our devices, the contribution of the substrate is reduced to its minimum by the use of the insulating quartz substrate, and only the C_P value needs to be considered to produce an accurate equivalent circuit model.



Device	L_S	$R_{S(DC)}$	C_P
L_1	3.8 nH	0.62 Ω	83 fF
L_2	9.0 nH	0.48 Ω	67 fF

Fig. 7: Equivalent broadband RLC model of a spiral inductor [1] and extracted values for L_1 and L_2 devices (C_{INS1}, R_{SUB1} and C_{SUB1} substrate parameters are negligible).

Fig. 5 shows the electrical performance and RLC fit for the 3.8-nH inductor. We observed a peak quality factor of 35 at 3.5 GHz and a self resonance frequency of 9 GHz. Fig. 6 shows the electrical performances and RLC fit for the 9.3-nH inductor. Measured peak quality factor is 40 at 2.1 GHz and resonant frequency is 6.5 GHz.

It should be pointed that the fabricated devices exhibit a broadband Q-behavior, with Q exceeding 20 in the range of 1 to 5 GHz, enabling the use of such devices in multiband circuits, covering a significant number of telecommunication standards, including GSM, UMTS and WLAN. The achieved performances in terms of Q_{PEAK} and SRF are in the current state-of-the-art for integrated inductors [5, 11].

4. CONCLUSION

We developed an innovative fabrication process of passive devices directly embedded in an insulating substrate. This technique uses a state-of-the-art Alcatel AMS 200 DSE ICP dry etcher that enables to pattern deep trenches in quartz substrates and to fabricate devices using a reduced number of masks. The major advantage of this technique is to significantly decrease the RF losses due to parasitic capacitance by using a dielectric as substrate. We fabricated and characterized integrated spiral inductors with high RF performances (peak quality factor in excess of 30 around 2 GHz and self resonant frequency superior

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to 6 and 9 GHz) using a thick high conductivity copper / quartz fabrication process.

The broadband Q-behavior of the fabricated components enables the use of them in telecommunication applications, particularly in multi-standard circuits that can operate at different standards in the 1 – 6 GHz range (GSM, UMTS and WLAN).

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