Bonding Semiconductor Laser Chips : Substrate Material Figure of Merit and Die Attach Layer Influence

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Belgirate, Italy, 28-30 September 2005

BONDING SEMICONDUCTOR LASER CHIPS: SUBSTRATE MATERIAL FIGURE OF MERIT AND DIE ATTACH LAYER INFLUENCE

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ABSTRACT

The coefficient of thermal expansion (CTE) and the thermal conductivity are the two key parameters to consider when selecting a particular substrate material for a die bonding process. We will discuss here a model to determine the substrate material giving the best chip reliability expectations for GaAs and InP laser chips. In that respect, a comparison of the thermo-mechanical stresses induced during the soldering process of GaAs and InP semiconductor chips on different substrate materials used in optoelectronic packaging is presented. In parallel, the thermal resistances of the material stacks under consideration are evaluated. The comparison of the substrate materials is based on the evaluation of failure rates for two chip failures mechanisms. We will show that CuW is the best candidate for bonding GaAs lasers chips. In the case of InP chips, the AlN submount offers the best performances.

1. INTRODUCTION

While the manufacturing cost of semiconductor laser chips has been steadily reduced over the past few years, the major manufacturing cost factor of optoelectronic components today remains in the assembly and packaging steps. The latest trend in transceiver as well as pump laser assembly shows clearly that modules without thermo-electric cooler, so called uncooled modules, establish themselves as a cost-effective alternative [1]. This imposes stringent requirements on materials and package designs. In particular, the selection of the submount material is driven by the need of matching the coefficients of thermal expansion of both the optical components and the submount as well as by providing an efficient thermal pathway from the active layer to the heat sink in order to minimize the junction temperature [2][3]:

- During the heating step of the soldering process, the semiconductor laser die and the substrate are free to expand. However, the expansion of the substrate and the laser die usually differ owing to dissimilar CTE's. During the cooling phase of the soldering process, the motion between the die and the submount is prevented by the solder layer, and stresses are induced in the assembly.

- The performance of a laser diode is affected by the temperature distribution and temperature gradients in the active layer. In particular, a high junction temperature and local hot spots lead to a degradation of mechanical and electro-optical properties, which can result in a premature failure of the device. As the junction temperature increases with the thermal resistance of the material stack, the thermal resistance of the assembly should be minimized.

Generally, the preferred submount for soldering InP or GaAs chips is AlN or Si due to high thermal dissipation and good CTE matching properties. Silicon offers as well an extensive hybridization potential. Standard IC photolithography and structuring processes not only allow the fabrication of electrical interconnects but also open the way to the fabrication of high-precision alignment features needed to mount optical devices [4].

In this work, we have compared the performances of different materials (Si, Cu, CuW, Kovar, AlSiC, AlN, Al_2O_3, Diamond) to be used as the mounting platform of GaAs and InP semiconductor chips. The influence of the solder material composition and thickness will be evaluated. The selection of the best suited substrate material for a given laser chip geometry will be based on failure rates evaluation for two failure mechanisms. The impact of the laser geometry on the failure rates will be discussed.

ISBN 2-916187-01-4

2. CASE STUDY

The assembly under investigation is a 2.4 x 0.4 x 0.15mm^3 GaAs or InP semiconductor laser chip soldered on a 4.8 x 4 x 0.5 mm^3 thick submount (Figure 1). Such chip geometries can be found in 980 nm and 14xx nm pump lasers modules for erbium-doped fiber amplifiers.

The chip, substrate and die attach material properties involved in the calculations are summarized in Table 1.

Material	CTE (ppm/K)	Thermal conductivity (W/m.K)	Young modulus (GPa)	Shear modulus (GPa)
InP	4.6	80	61	23
GaAs	6.5	54	86	33
Si	4.2	150	130	52
Cu	17.8	400	110	46
CuW	7	180	260	710
Al	23.6	240	70	25
Kovar	5.8	15	138	52
AlN	4.5	170	350	140
Al_2O_3	6.7	21	390	125
AlSiC	8	200	188	76
Diamond	2	2000	800	
AuSn (80 % Au wt)	16	58	68	25
AgSn (96.5% Ag wt)	22	36	50	19
Epoxy	50	0.3	3	1.2

Table 1. Thermo-mechanical parameters of the assembly materials considered in this work.

A thin TiW/Ni/Au pad under the laser chip is provided for contact redistribution and as underbump metallization (UBM). The other metallic pads for the back facet monitoring photodiode and for the thermistor are not shown on this representation on the substrate as they do neither influence the magnitude of the thermal resistances nor the thermo-mechanical stresses. Unless otherwise stated, a 20 µm thick AuSn (80% wt Au) solder layer between the substrate and the laser has been assumed.

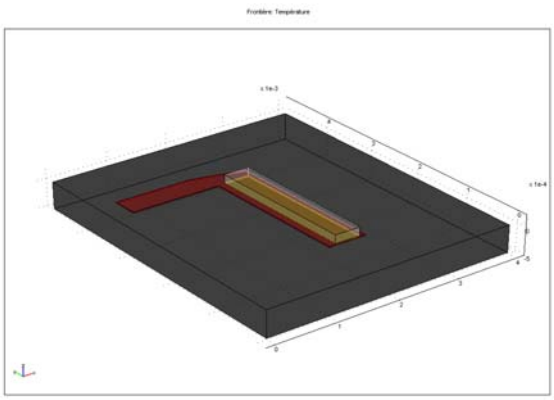

Figure 1 Chip on submount under investigation: the 2.4 mm long laser chip is soldered on a 4.8 mm x 4 mm. A metallic redistribution pad under the chip enables the electrical connection of the bottom laser electrode.

3. THERMAL RESISTANCES

The thermal resistance R_{th} is a key parameter that determines the junction temperature T_j according to

$$T_j = T_{hs} + R_{th} P_{heat} = T_{hs} + R_{th}\left(P_{el} - P_{opt}\right) \quad (1)$$

where T_{hs} is the heat-sink temperature, P_{heat} the generated heat power, P_{el} the electrical input power, and P_{opt} the generated optical output power of the laser diode. As the junction temperature increases with the thermal resistance of the material stack, the thermal resistance of the assembly should be minimized.

Heat conduction is described by a rate equation known as Fourier's law:

$$q = -k\Delta T \quad (2)$$

where q is the heat flux (W.m^2). The heat flux is proportional to the temperature gradient in the structure. k is the thermal conductivity (W/m.K).

In order to evaluate the thermal resistances between the laser channel and the base surface of the submount, we assume that a heat source of 1W is equally distributed along the channel. Under this assumption, the thermal resistance is equal to the temperature difference between the laser junction and the base of the submount.

In this work, the Fourier equation was numerically solved with Finite Element Modeling using Femlab. A non-uniform mesh has been used in the calculations with a minimum of 3 elements for the smallest dimension (Figure 2).

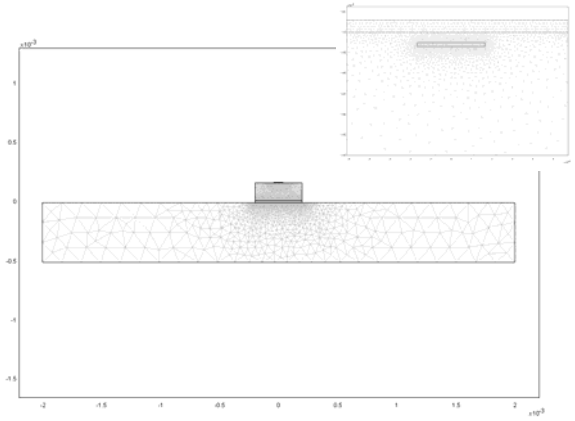

Figure 2 Non-uniform meshing used to calculate the temperature distribution in the structure. The elements are getting smaller as the structure dimensions decrease. Inset: close view of the active region.

The heat source (the active laser area) is considered to be 0.75 µm below the top surface of the chip. Its lateral dimensions are 3.5x 0.5 µm. A cross-section of the laser chip under investigation is shown in Figure 3. This simplified laser chip cross-section reproduces the thermal resistances of ridge structures within fractions of K/W, which is good enough for investigating differences in thermal performances of substrate materials.

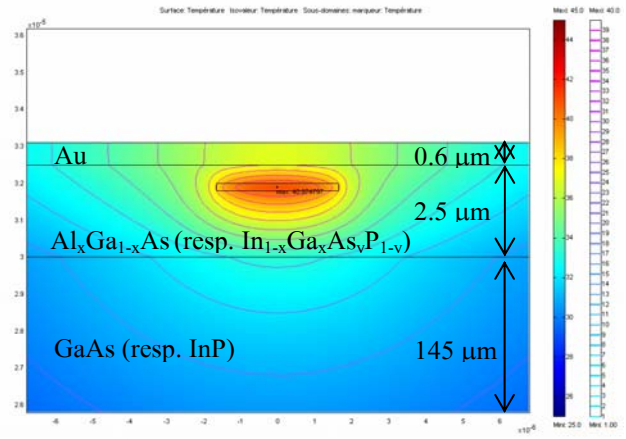

Figure 3 Cross-section of the simplified laser chip: the active layers are lattice-matched $Al_xGa_{1-x}As$ or $In_{1-x}Ga_xAs_yP_{1-y}$ materials on GaAs or InP. A 0.6 µm Gold layer has been deposited on the active layer for current injection.

4. THERMO-MECHANICAL STRESSES

Typical failure modes in chip-substrate assemblies are chip fracture (tensile/compressive stresses at the chip center or shear stresses at the corner) or failure of the attach material (cohesive or delamination).

The attach layer in a chip-substrate assembly is usually much thinner than the chip and the substrate, while Young's modulus of the attach material is smaller or similar to Young's moduli of the adherends' materials. Thus, the compliance of the attach layer is substantially larger than the compliance of the adherends and the attach material is subjected to shear only and its coefficient of thermal expansion does not affect the thermally induced stresses in the assembly. In this configuration and assuming that there is no bending, the CTE mismatch induced shear stress $\tau_{\alpha,s}$ at the substrate-solder and at the chip-solder interface is maximum at the edge of the chip. Its value is given by [5]:

$$\tau_{\alpha,s} = \Delta\alpha\Delta T G_d \frac{\tanh \beta L}{\beta t_d} \qquad (3)$$

where β is defined as:

$$\beta = \sqrt{\frac{G_d}{t_d}\left(\frac{1}{E_c t_c} + \frac{1}{E_s t_s}\right)} \qquad (4)$$

The subscripts c, s and d stand for chip, substrate and die attach materials, respectively, Δα is the CTE mismatch between the chip and the substrate, and ΔT is the temperature change. E and G are the elastic moduli in tension and shear, respectively, t represents the materials thickness, and 2L is the chip length.

Similarly, the maximum normal stress σ (at the center of the chip) is given by:

$$\sigma = \frac{\Delta\alpha\Delta T G_d}{\beta^2 t_d}\left(1 - \frac{1}{\cosh \beta L}\right) \qquad (5)$$

We are going to use this analytical approach to determine the magnitude of the interfacial shear stresses at the die-substrate corner as well as the stresses acting at the cross-sections of the die and substrate materials themselves. The normal stresses will influence the thermo-mechanical chip failure rate as discussed in section 6.

5. RESULTS

5.1. Thermal performance

In order to evaluate the influence of the substrate on the thermal resistance of the assembly stack of Figure 1, we have used 2D modeling. A comparison of the thermal resistivity of GaAs-based devices evaluated using 2D and 3D modeling shows that the difference of thermal resistances obtained with 2D and 3D modeling is below 5% in the worst case (Figure 4). A uniform heat load at

the top of the surface chip was considered here for this comparison.

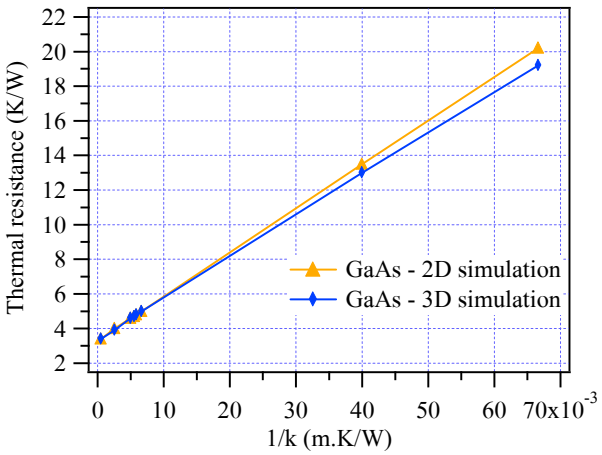

Figure 4 Thermal resistances as a function of the thermal resistivity of the different substrate materials under evaluation.

Based on the results of Figure 4, it is interesting to note that the thermal resistance of the whole stack can be modeled as a linear function of the thermal resistivity of the substrate:

$$R_{stack} = a_1 + \frac{a_2}{k} \qquad (6)$$

The system is equivalent to a 1D stack where 2 thermal resistances are put together in series:

- The thermal resistance a_1 for infinitely small 1/k corresponds to the thermal resistance of the GaAs chip (3.25 K/W).
- The slope a_2 gives an equivalent substrate thickness/surface factor identical for *all* substrate materials over this range of thermal conductivity. This slope is equal to approximately 254 m^{-1} in the 2D case and 239 m^{-1} in the 3D case, which gives an equivalent surface 2.1 larger than the chip surface if we consider that the submount thickness remains unchanged (0.5 mm).

The 2D thermal resistance of the stack are given in Table 2 for both GaAs and InP devices. A confined heat load in the laser waveguide is here being assumed.

Submount	Thermal resistance GaAs device (K/W)	Thermal resistance InP device (K/W)
Diamond	11.6	8.4
Cu	12.2	9
AlSiC	12.9	9.6
CuW	13	9.8
AlN	13.1	9.9
Si 100	13.3	10.1
Al_2O_3	21.9	18.6
Kovar	28.6	25.3

Table 2. 2D thermal resistivities of chip-substrate stacks with a 20 µm thick AuSn solder (80% wt Au).

Again, the linear dependence of the thermal resistance of the stack is confirmed here (Figure 5). Interestingly, the magnitude of the slope is similar to the one observed in the uniform loading case and is identical for both GaAs and InP devices, confirming that this slope is only a geometry parameter and not a material one.

The thermal resistances are larger here in the confined heat load than in the uniform heat load configuration. Indeed, there is a spreading resistance in the GaAs, resp. InP chip. This spreading resistance is in the range of 5.5 K/W (resp 4.1 K/W) for GaAs (resp. InP).

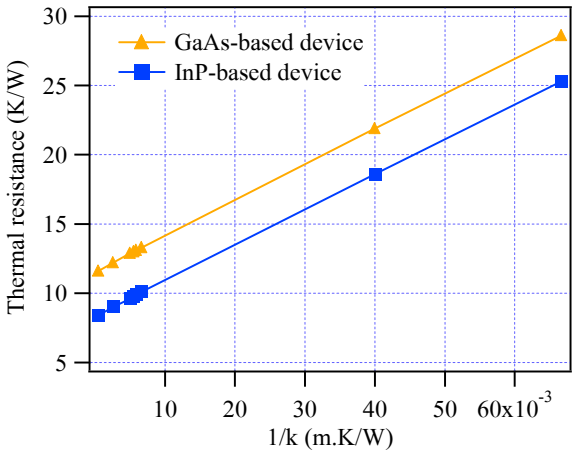

Figure 5 2D Thermal resistances of GaAs and InP devices as a function of the thermal resistivity of the different substrate materials under evaluation. Here, a confined heat load is assumed.

In a 2D simulation, the thermal resistance inversely scales with the chip length. Thus, in a GaAs on AlN configuration, the thermal resistances increases from

13.1 K/W for a 2.4 mm long laser chip to 52.4 K/W for a 0.6 mm long laser chip.

Figure 6 shows the influence of the solder thickness and composition on the thermal resistances. The calculations are given for a GaAs device soldered on a AlN and a Al_2O_3 substrate. The use of the AuSn solder (80% wt Au) instead of the AgSn (3.5% wt Ag) solder improves only slightly the thermal resistances of the stack. Similarly, the solder thickness has only limited influence (<5% variation) on the thermal resistances in the thickness range considered here.

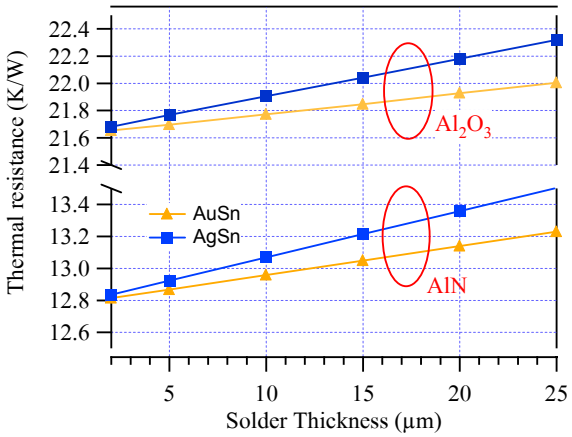

Figure 6 2D Thermal resistances as a function of the solder thickness and composition. The calculation are given for a GaAs device soldered on a AlN and a Al_2O_3 substrate.

It is clear that in a flip-chip configuration, i.e. when the laser is soldered p-down, the temperature of the laser junction is reduced as the junction is closer to the heat sink. Such a configuration is shown in Figure 7.

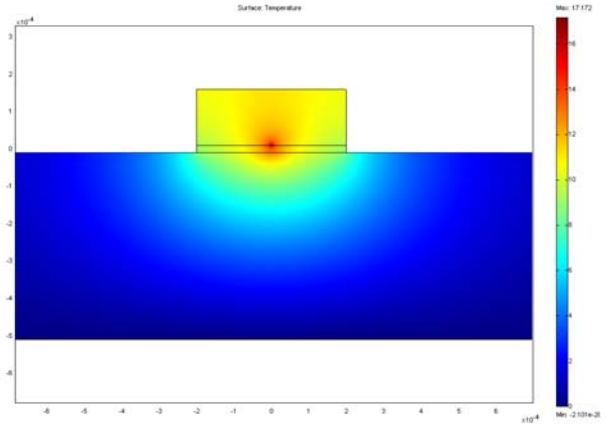

Figure 7 Flip-chip configuration: the laser is soldered face-down on the substrate: the laser junction is close to the heat sink.

The thermal resistances from a GaAs laser junction down to the base of the substrate in a flip-chip configuration are presented in Figure 8 together with the face-up mounting case. A decrease of the thermal resistances of 4 to 6 K/W can be expected in a flip-chip configuration.

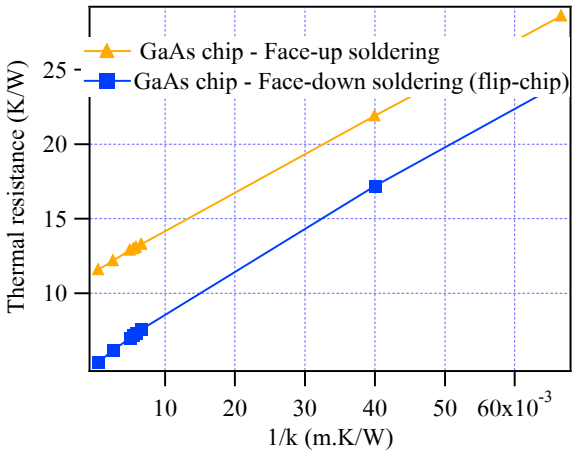

Figure 8 Flip-chip configuration: the laser is soldered face-down on the substrate: the laser junction is close to the heat sink.

5.2. Thermal stress

In Figure 9, we numerically evaluate the influence of the substrate on the maximum interfacial shear stress built-up during soldering of a 2.4 mm long GaAs chip. We assume a maximum temperature variation between room and soldering temperature of 300°C.

In the case of GaAs laser chips, the thermally induced shear stresses at the edge of the AuSn solder layer are approximately 8 to 10 times smaller when using an Al_2O_3 (7.4 MPa) instead of a AlSiC (54 MPa), a AlN (74 MPa) or a Silicon (80 MPa) substrate. The use of the Al_2O_3 substrate gives also smaller shear stresses at the chip–solder layer interface compared to a CuW (18 MPa) or a Kovar substrate (24 MPa). However, for all these substrates, the normal stresses displayed in Figure 10 remain below the GaAs fracture strength (85 MPa).

On the other hand, the estimated interfacial shear stresses are 387 MPa (resp. 168 MPa) when the GaAs chip is bonded onto a Copper (resp. Diamond) substrate. Assuming that the solder exhibits a linear elastic behaviour at such stress values, the normal (tensile) stresses in the GaAs chip are estimated to be 236 MPa (resp. 112 MPa), i.e. above the fracture strength of GaAs. However, as the estimated interfacial shear stresses exceed the yield stress of the gold-tin solder (275 MPa), a plastic deformation is induced in the solder during the cooling phase of the soldering process. This plastic

deformation redistributes the stresses in the solder layer and finally reduces the normal stresses in the GaAs chip [6]. Moreover, considering the creep-induced stress relaxation and slowing down the cooling process, once could further reduce the interfacial stress. This effect has proven to reduce also normal stresses from 130 MPa to 80 MPa in the case of GaAs chips soldered on Diamond substrates [7] and could eventually be applied to the GaAs chip on Copper to avoid chip cracking.

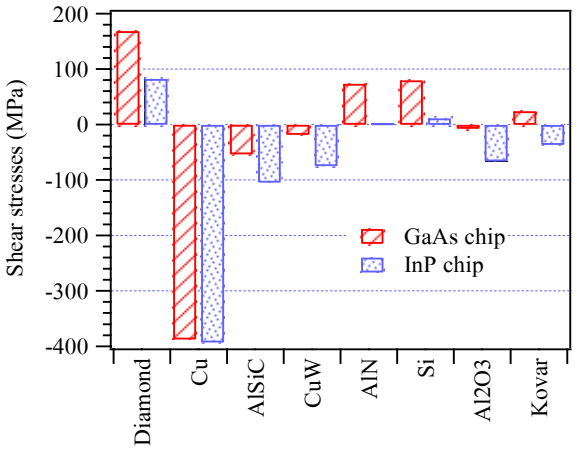

Figure 9 Comparison of the CTE-mismatch induced interfacial shear stresses when a 2.4 mm GaAs or InP chip is soldered to different substrate materials. The influence of the bending in the substrate and in the chip is not considered in these calculations.

For a defined CTE-mismatch between the substrate and the GaAs chip, the interfacial shear stress is limited, if a compliant and/or thick die attach material is used. Indeed, the use of a compliant epoxy material requiring a reduced temperature excursion during the bonding process decreases the shear stresses from approximately 80 MPa (with a AuSn solder) down to 9 MPa.

One can also decrease the interfacial shear stress by increasing the die attach material thickness t_d. Figure 11 represents the dependence of the maximum induced shear stress in the AuSn solder layer in a GaAs chip on a Silicon submount, when the maximum temperature change between the room and the soldering temperature is 300°C. The shear stresses at the substrate-solder and at the chip-solder interfaces are reduced by approximately 40%, when the solder layer thickness is increased from 20 µm to 60 µm. By this means, the normal stresses in the GaAs die are also reduced and the assembly integrity is ensured.

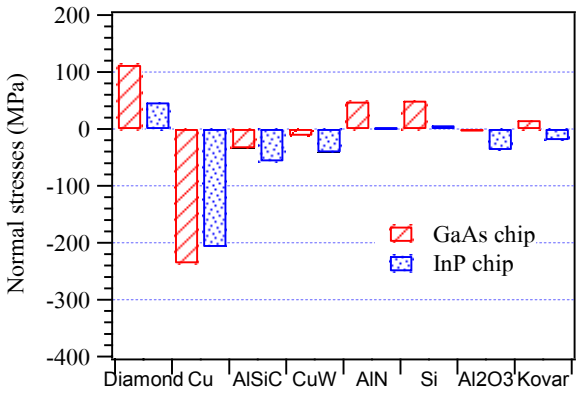

Figure 10 Comparison of the CTE-mismatch induced normal stresses when a 2.4mm GaAs or InP chip is soldered to different substrate materials.

On the other hand, according to equation 4, the influence of the solder thickness on the normal stresses in the chip is negligible for a 2.4 mm long laser chip.

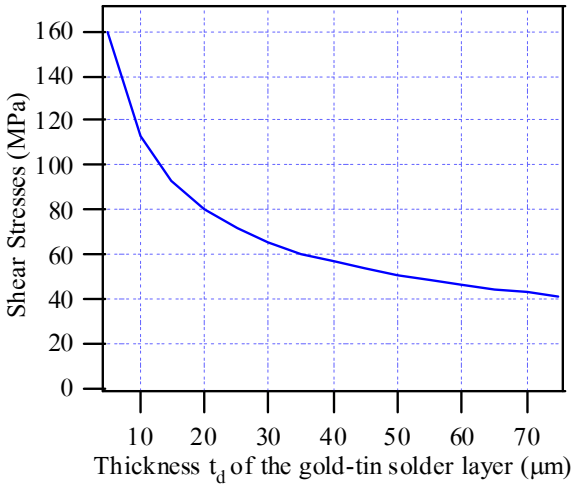

Figure 11 Dependence of the CTE mismatch induced shear stresses as a function of the AuSn solder thickness assuming a difference between room and soldering temperature of 300°C. The interfacial shear stresses are better accommodated with a thick solder layer.

In the InP laser chip configuration, the thermally induced shear stresses at the edge of the AuSn solder layer are optimized when the laser chip is soldered onto a AlN (3 MPa) or a Silicon substrate (12 MPa). AlSiC or CuW materials will give larger shear stresses at the chip-solder interface with -104 MPa and -74 MPa.
For all substrate materials except Cu, the normal stresses at the center of the InP chip stay below the InP fracture strength. For the InP chip soldered on a Copper substrate exceeds the InP fracture strength and the chip is expected

to crack upon a rapid cooling phase of the soldering process.

6. ANALYSIS OF CHIP FAILURE MECHANISMS

Potential laser chip failure mechanisms fall into two categories:
- Thermo-optical failure due to the heat generated at the laser junction.
- Thermo-mechanical failure due to a native thermo-mechanical stress.

We do not consider here the delamination failure mechanism.

The influence of the junction temperature on the thermo-optical failure rate F_H of a laser chip can be described by the Arrhenius equation [8]:

$$F_H = Ae^{\frac{-E_{a1}}{k_B T_j}} \qquad (7)$$

where A is a constant, E_{a1} an activation energy, k_B the Boltzmann constant and T_j the junction temperature.

Similarly, the fracture of material under mechanical load is a thermally activated process. In order to limit the risks of chip fracture, cracks and voids from the dicing and handling operations should be minimized. The thermo-mechanical chip failure rate F_S under an applied stress can be given by the Eyring equation [8]:

$$F_S = B\sigma e^{-\frac{E_{a2}}{k_B T}} \qquad (8)$$

where B is a material parameter, σ the applied stress and E_{a2} is the activation energy for crack propagation.

The default activation energy specified in the Telcordia Generic Requirements GR 468 is 0.4 eV for laser diode module failure estimation [9]. As there is no experimental value available, this value was used in the failure rate calculations described below.

In order to compare the failures rates for the different substrates under investigation, the AlN substrate will be taken as a reference. An ideal heat sink temperature of 0°C and a heat load of 1W will be assumed in the calculations.

Table 3 gives the normalized failure rates FH/FH_{AlN} and FS/FS_{AlN} of a 2.4 mm GaAs chip for all substrates under study. From equation (7), it is clear that the thermo-optical laser chip failure rate only depends on the thermal resistance of the stack. It is thus not surprising to find a similar trend for the thermo-optical failure rate than for the thermal resistivity. In that respect, AlSiC, CuW, AlN and Si give very similar failure rate estimations and Kovar is expected to induce more than twice as much failures as the AlN submount.
As far as the thermo-mechanical stresses - induced failure rates are concerned, the trend is different as there is an interplay of both thermo-mechanical stresses and thermal resistances. The use of CuW and Al_2O_3 gives the most relaxed handling and assembly tolerances.

Substrate	FH/FH_{AlN}	FS/FS_{AlN}
Diamond	0.92	2.2
Cu	0.95	4.7
AlSiC	0.99	0.7
CuW	1	0.2
AlN	1	1
Si 100	1.01	1
Al_2O_3	1.62	0.2
Kovar	2.3	0.7

Table 3 Normalized failure rates of a GaAs chip for all substrates under evaluation. The AlN substrate has been taken as a reference.

Table 4 gives the normalized failure rates FH/FH_{AlN} and FS/FS_{AlN} of an InP chip for all substrates under study. Similarly to the GaAs chip, the thermo-optical failure rate of the InP chip follows the thermal resistances of the stacks and again there, AlSiC, CuW, AlN and Si give very similar failure rates estimations. On the other hand, as far as the thermo-mechanical stresses - induced failures are concerned, the AlN substrate gives, by far, the best failure rates estimations and handling tolerances.

Substrate	FH/FH_{AlN}	FS/FS_{AlN}
Diamond	0.92	24.6
Cu	0.95	113.1
AlSiC	0.99	32.3
CuW	1	23.6
AlN	1	1
Si 100	1.01	3.7
Al_2O_3	1.63	34.3
Kovar	2.33	26

Table 4 Normalized failure rates of a InP chip for all substrates under investigation. The AlN substrate has been taken as a reference.

 ISBN 2-916187-01-4

The extension of these results to transmitter-type lasers (i.e. shorter chips) shows that the impact of the substrate material on the failure rates exhibits similar trends.

Following the weakest link model, the device failure originates from the weakest point. Whether this is the thermo-optical or thermo-mechanical chip failure, will depend on various factors:
- laser chip design
- wafer processing and dicing
- chip handling
- presence of voids in the solder layer

Before applying one or the other chip failure model, the physics of the failure phenomenon must be confirmed experimentally.

7. CONCLUSIONS

A good trade-off between the CTE matching and thermal conductivity of the submount material must be found. The selection of the best suited substrate material for a specific application is driven by the knowledge of the weakest point in the assembly stacks. This weakest point will be affected by several factors from the design to the wafer technologies and the assembly process. Nevertheless, it is clear that AlN, Si and CuW, AlSiC are the best candidates for bonding GaAs lasers chips with a slight advantage for CuW. In the case of InP chips, the AlN submount offers the best performances to avoid thermomechanical chip failures. The model used here can be improved by the integration of other failures mechanisms, e.g. delamination, and by a better knowledge of activations energies.

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