



# Improving the Efficiency of the Oscillation-Based Test Methodology for Parametric Faults

Aboubacar Chaehoi, Yves Bertrand, Laurent Latorre, Pascal Nouet

## ► To cite this version:

Aboubacar Chaehoi, Yves Bertrand, Laurent Latorre, Pascal Nouet. Improving the Efficiency of the Oscillation-Based Test Methodology for Parametric Faults. LATW: Latin American Test Workshop, Feb 2003, Natal, Brazil. pp.234-237. lirmm-00269433

**HAL Id: lirmm-00269433**

**<https://hal-lirmm.ccsd.cnrs.fr/lirmm-00269433>**

Submitted on 3 Apr 2008

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# Improving the Efficiency of the Oscillation-based Test Methodology for Parametric Faults

A. Chaehoi, Y. Bertrand, L. Latorre, P. Nouet

Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier (France)

LIRMM, University of Montpellier / CNRS

Tel.: (+33) 467 418 527 Fax: (+33) 467 418 500 E-mail: [nouet@lirmm.fr](mailto:nouet@lirmm.fr)

## Abstract

*In this paper we introduce the use of Monte-Carlo (MC) simulations in order to facilitate OTM implementation and to evaluate fault coverage quantitatively even for parametric faults. Thanks to a case study, we demonstrate the contribution of MC simulations for both tolerance range and test efficiency determination.*

## 1. Introduction

Oscillation-based Testing Methodology (OTM) consist in reconfiguring the system under test into a closed-loop oscillator. Go/noGo testing is then possible by monitoring only the characteristic parameters of the oscillation. It has been introduced for low-cost testing of various types of Integrated Circuits including digital circuits [1], analog circuits [2] and more recently MEMS [3].

The main advantage of OTM is the low-cost of both DfT insertion and test procedure. Indeed, design for testability using OTM is generally simple and implemented with a very small area overhead. Moreover, the testing procedure itself is easily implemented by monitoring only an oscillating signal on an analog output. The efficiency of the method is then excellent for catastrophic faults that imply non-oscillating behaviors or strong frequency shifts.

However, the method suffers from a loss of efficiency when parametric faults are targeted. First, test preparation is rather difficult as it includes a three step simulation procedure to determine the tolerance range of the monitored parameters [3]. Second, once tolerance ranges have been determined, it is very difficult to evaluate test efficiency in the case of soft faults.

In this paper we introduce the use of Monte-Carlo (MC) simulations in order to facilitate OTM implementation and to evaluate fault coverage quantitatively even for parametric faults. We expect from the statistical approach several improvement of OTM during both tolerance range determination and test

efficiency evaluation. The proposed improvement is validated on a Micro-Electro-Mechanical System (MEMS) designed in our laboratory. Here the MEMS under test can be considered as an analog circuit.

The first section of the paper briefly reviews the design of the MEMS under test (MUT). Parametric faults that may affect our design are then discussed in the second section. Next, both classical and new implementations of OTM are presented and discussed. Finally, efficiency of both approaches are compared in the last section.

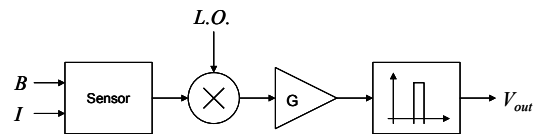
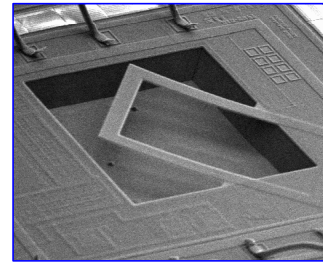
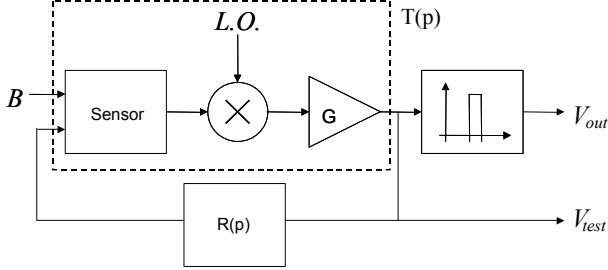


Figure 1: Magnetic field sensing device and schematic view of the measurement system without DfT.

## 2. Overview of the MEMS Under Test

The MEMS under test is a low noise, highly sensitive magnetometer. It is based on a U-shaped micro-mechanical resonator fabricated by post-processing a CMOS die using Front Side Bulk Micromachining (Fig. 1.a). Under the action of an in-plane magnetic field on an electrical current flowing into the beam, the frame is deflected and the obtained stress is detected by resistive strain gauges located in both arms of the frame. These gauges are placed together with reference resistors to form a wheatstone bridge that converts the linear resistance variation into a differential voltage. The frequency of the

signal is then shifted to fit the central frequency of a band-pass filter through a frequency mixer. The complete system (Fig. 1.b) also includes an instrumentation amplifier of gain  $G$  and has demonstrated its ability to serve as a micro-compass [4].



**Figure 2: Schematic view of the modified MUT for OTM.**

The basic idea of OTM consists in reconfiguring the system during test to make it self-oscillating. Both frequency and magnitude of oscillations are then monitored rather than open-loop specifications such as sensitivity, bandwidth... The MUT can be easily turned into an oscillator by connecting a feedback loop  $R(p)$  between the output of the amplifier and the voltage input of the current loop (Figure 2). Assuming a static magnetic field, the open loop response  $T(p)$  is a simple second order system:

$$T(p) = B \times \frac{A/k}{1 + 2\xi \frac{p}{\omega_0} + \frac{p^2}{\omega_0^2}}$$

where  $1/k$  is the mechanical gain,  $\xi$  is the damping coefficient and  $A$  is a complex function of the gauge location, the piezoresistive factor, the magnitude of the current, the amplification... A simple first-order derivative circuit is used for  $R(p)$ . Due to the high quality factor of the mechanical structure, oscillation conditions are fulfilled nearby the mechanical natural frequency  $\omega_0$ . The modified design has been implemented on silicon and oscillation conditions experimentally validated on a set of 25 prototypes.

### 3. Fault modeling

As for all mixed-signal circuits, the fault list for a MEMS may be divided in two classes, the hard faults and the soft faults. The latter are generally ineffective for digital circuits where the intrinsic robustness of the design leads to test only hard faults with the classical “stuck-at” model. For analog circuits, the soft faults must be dealt with a particular care as they can be detected only in the analog domain. A soft fault model generally consists in considering a tolerance range for each candidate parameter while all other parameters of the circuits are assumed to be at their nominal value.

The MUT discussed in this paper is free of digital parts and the behavior of the electro-mechanical component is intrinsically analog. In this section, we introduce a subset of the parametric faults that may affect the MUT. Hard faults are not taken into account as it is obvious that they often lead to a non-oscillating device. These catastrophic faults are then assumed to be easily detected. On the other side, the more hard-to-detect faults are those parametric faults that can be related to process scattering. We have then defined a set of parameters that may affect the mechanical behavior of the sensor. Similarly, it is possible to include parametric faults affecting the value of resistors, the offset of Operational Amplifiers, ...

In this paper, 34 parameters affecting the behavior of the sensor have been taken into account. Finally, the fault list is constructed from the deviation of those parameters:

- material density of each layer composing the mechanical structure (i.e. oxyde, aluminum, polysilicon and passivation nitride),
- resistivity of the aluminum and the polysilicon,
- piezoresistive factor of the polysilicon layer,
- Young’s moduli of each layer composing the mechanical structure,
- Thickness of each layer composing the mechanical structure,
- Geometric dimensions of the structure (width, length, ...).

Each parameter comes with a nominal value and a standard deviation. For those that are not characterized by the CMOS foundry, we have performed a characterization campaign [5]. Fault injection is realized through a VHDL-AMS description of the sensor that supports all the previously listed parameters [6].

### 4. Classical OTM implementation

Classical OTM has been already applied to the previously described design [3]. Main steps of the test setup are recalled to highlight the limitations of the classical method. The specifications of the system under test are called the Direct Parameters (noted  $DP_k$  in the following). Each element in the soft fault list is called a low-level parameter ( $LP_j$ ) and is defined with a nominal value.

The first step of the test preparation consists in simulating the device under test in the normal mode (open loop). All  $LP_j$  are kept nominal excepted one at a time and a tolerance range  $TR_{LP_j}$  is defined for each  $LP_j$  that guarantees all  $DP_k$  are within the specifications of the system.

The second step consists in applying these variations  $TR_{LP_j}$  one at a time (other  $LP_j$  are kept nominal) to the system in test mode (closed loop) and to monitor both frequency and magnitude of the oscillations (called in the

following indirect parameters  $IP_k$ ). For each pair of  $LP_j$  and  $IP_k$ , an acceptance range is calculated for the indirect parameter (noted  $TR_{IP_k}^{LP_j}$  in the following).

Once all individual  $TR_{IP_k}^{LP_j}$  are determined, it is necessary to deduce the overall tolerance on each indirect parameter. At this point two different test strategies can be considered:

- A yield based approach guaranteeing that no fault-free devices will be declared faulty. In this case, the overall tolerance should be calculated as the less constraining range  $TR_{IP_k} = \bigcup_{\{LP_j\}} TR_{IP_k}^{LP_j}$ . This approach ensures the best production yield but does not guarantee that all passing devices will meet specifications.
- A fault coverage based approach guaranteeing that all faulty devices will be detected. In this case, the overall tolerance should be calculated as the more constraining range  $TR_{IP_k} = \bigcap_{\{LP_j\}} TR_{IP_k}^{LP_j}$ . This

approach ensures that all passing devices will meet specifications but at the price of some inappropriate rejections.

This classical implementation of OTM suffers from three main drawbacks:

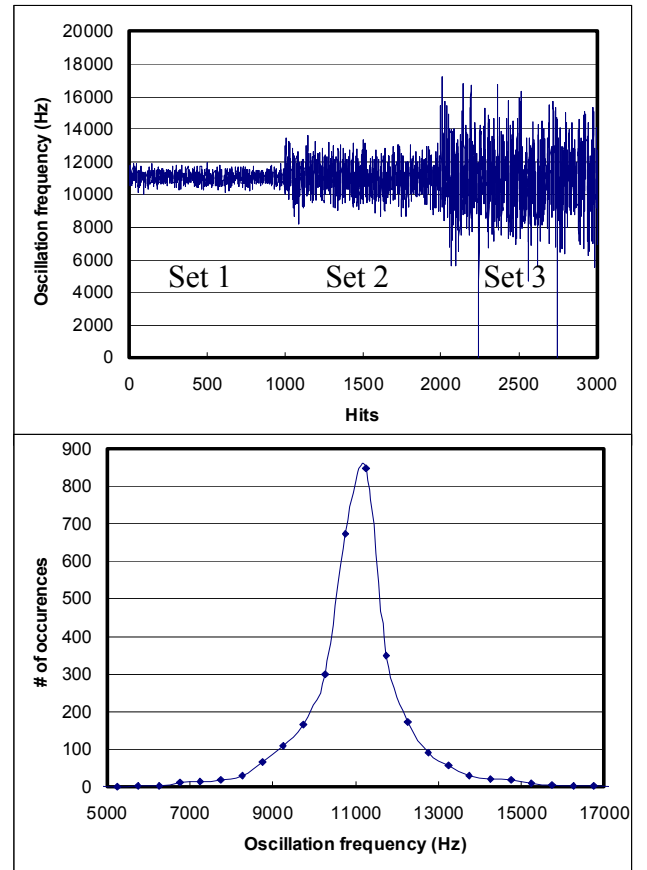
- test preparation is relatively complicated and numerous simulations must be performed,
- it assumes that only one parameter is at a non-nominal value at a time,
- test efficiency is very difficult to evaluate quantitatively.

## 5. New implementation of OTM

In this section, we address the determination of the tolerance ranges on characteristic parameters of the oscillation (frequency and magnitude). The new proposed OTM allows a straightforward determination of this tolerance ranges and moreover the single fault assumption is no more required.

New OTM implementation consists in considering that a soft fault is defined as a set of  $LP_j$  values that leads to at least one  $DP_k$  outside the specifications. This multiple fault assumption will make extensive use of MC simulations to determine the range of correct or incorrect behavior. Starting from a behavioral model of the sensor, both open loop and closed loop systems can be simulated concurrently in a standard microelectronic design framework during a learning phase. Each  $LP_j$  has been associated with a gaussian distribution defined by a nominal value and a standard deviation. For each run, both direct and indirect parameters are monitored with the same set of low-level parameters.

Three sets of 1,000 simulation runs have been defined to obtain populations with various ratio of correct and incorrect behavior. For that, we assume a specific design and we adjusted the standard deviation of each low level parameter to cover three production yield representative of process robustness. We then obtained a low yield production set (Set #3 on figure 3) where only 20 % of the simulations lead to a correct set of  $DP_k$ , a mid yield with 50 % of the runs in the specifications (Set #2) and a high yield process (Set #1) where 93 % of the dies match the open-loop specifications of the system. On figure 3, results obtained for the oscillation frequency (closed loop system) are reported. The evolution of the frequency over the 3000 hits are reported in the following order: high yield process for hits 1 to 1000, medium yield process (hits 1001 to 2000) and finally low yield process (hits 2001 to 3000). The impact of increasing the standard deviation of the gaussian distribution of each  $LP_j$  is clearly demonstrated. On the bottom graph, the gaussian distribution of the simulated oscillation frequency is reported over the 3000 hits.



**Figure 3: Monte-carlo simulations of the closed-loop system : evolution of the oscillation frequency on 3000 hits (top) and Gaussian distribution of the oscillation frequency (bottom).**

For each set, we can determine the minimal value and the maximal value of both indirect parameters (i.e. the frequency of the oscillations and the peak to peak amplitude) that correspond to fault-free initial specifications. In table 1, the tolerance ranges determined for each set are reported and compared with the tolerance ranges previously determined using the classical OTM test setup. The new tolerance ranges are significantly different from those issued from the single fault assumption and are clearly independent of the yield of the population used during this learning step. It is worth noting that the new proposed implementation of OTM is yield oriented as the tolerance ranges are determined in such a way that all good dies will be kept.

	Classical OTM		New OTM		
	Yield	FC	Set 1	Set 2	Set 3
Min. Frequency (Hz)	10159	10761	10365	10373	10378
Max Frequency (Hz)	11617	11576	11666	11675	11683
Min. Amplitude (V)	1,90	2,09	1,96	1,99	1,98
Max. Amplitude (V)	2,40	2,26	2,44	2,41	2,40

**Table 1. Tolerance ranges on indirect parameters for classical OTM and for the new OTM implementation.**

## 6. OTM efficiency

In this section, we address the second limitation of the classical OTM. Efficiency was previously evaluated qualitatively rather than quantitatively or by considering specific faults. Thanks to MC simulations, we are now able to quantitatively compare the efficiency of the classical OTM implementation with the proposed one. Moreover, we will be able to give a metric representative of the efficiency of the test. For each hit, it is possible to determine if the circuit is good or faulty by verifying all direct parameters. On the other side, the circuit is accepted or rejected with respect to the signature of indirect parameters. For each hit we may then obtain:

- good circuits that are accepted (good decision),
- good circuits that are rejected (yield loss),
- faulty circuits that are rejected (good decision),
- faulty circuits that are accepted (escape).

Test results are given in table 2. for the 3000 hits of Monte-Carlo simulations. All previously determined tolerance ranges (see table 1) have been used to calculate the three estimators of the test efficiency (i.e., escape, yield loss and good decisions). Obviously, the tolerance ranges determined using classical OTM with the fault coverage approach are the most suitable for high fault coverage (less than 5 % of escape level) but at the price of an important loss in terms of production yield (four good dies among ten are rejected !!!). Yield loss is seriously improved using new OTM setup whatever the learning set is. Finally, the overall efficiency of the test, i.e. the

number of times where oscillation testing conduct to a good decision, is better than 94% for the new OTM implementation.

	Classical OTM		New OTM		
	Yield	FC	Set 1	Set 2	Set 3
Escape	12,15%	4,17%	11,13%	10,83%	10,98%
Yield Loss	2,20%	40,45%	0,18%	0,49%	0,67%
Overall efficiency	93,27%	76,07%	94,83%	94,80%	94,63%

**Table 2. OTM efficiency evaluated over 3000 hits of Monte-Carlo simulations for various tolerance ranges listed in table 1.**

## 7. Conclusions and perspectives

In this paper we have presented an improved implementation of the OTM that is more efficient for parametric faults. We are proposing to determine the tolerance range on indirect parameters (i.e. the oscillating frequency and the amplitude of the oscillation) by simulating concurrently the initial system and the system in the test mode using monte-carlo simulations. As each parameter is defined by a nominal value and a standard deviation, a soft fault is then a set of parameters that lead at least one characteristic of the system outside the specified limits.

Tolerance ranges on indirect parameters have been determined using a learning step of 1000 hits for different ratios of good circuits versus faulty circuits and this ratio appear to be without notable effect on the tolerance range.

Finally, the tolerance range efficiencies have been evaluated on a set of 3000 hits and the proposed method appears as a serious improvement of both the implementation and efficiency of OTM.

## 8. References

- [1] K. Arabi, H. Ihs, C. Dufaza and B. Kaminska, "Digital oscillation-test method for delay and stuck-at fault testing of digital circuits", Proc. International Test Conference, 1998. Proceedings., International , 1998, pp. 91–100.
- [2] G. Huertas, D. Vazquez, A. Rueda and J.L. Huertas, "Effective oscillation-based test for application to a DTMF filter bank", ITC 1999, pp. 549-555.
- [3] V. Beroulle, Y. Bertrand, L. Latorre and P. Nouet, "Evaluation of the Oscillation-based Test Methodology for Micro-Electro-Mechanical Systems", Proc. 20<sup>th</sup> IEEE VLSI Test Symposium (VTS'2002), pp. 439-444, Monterey, CA, USA, 28 Avril-2 Mai 2002.
- [4] V. Beroulle, Y. Bertrand, L. Latorre and P. Nouet, "Micromachined CMOS Magnetic Field Sensors with WITH Low-noise Signal Conditioning", Proc. IEEE International Conference on Micro Electro Mechanical Systems (MEMS'2002), pp. 256-259.

- [5] L. Latorre, V. Beroulle, M. Dardalhon, P. Nouet, F. Pressecq and C. Oudea, "Characterization of CMOS MEMS technology scatterings", Proc. of the 27<sup>th</sup> International Symposium for Testing and Failure Analysis (ISTFA 2001), Santa Clara (CA), USA, 11-15 November 2001, pp. 373-377.