Dual Mode Hybrid PLL Based Frequency Synthesizer for Cognitive Multi- radio Applications

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DUAL MODE HYBRID PLL BASED FREQUENCY SYNTHESIZER FOR COGNITIVE MULTI-RADIO APPLICATIONS

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ABSTRACT

This paper investigates a novel approach to implementation of multiband frequency synthesizer for cognitive multi-radio applications. The architecture here considered employs a dual-mode PLL (Phase Locked Loop) based frequency synthesizer for data applications, which is capable to switch between a fractional wideband high speed mode and an integer, narrowband and low spur mode after the settling. A secondary integer-N PLL synthesizer is proposed for voice applications. Both synthesizers are driven by the same reference oscillator. The overall architecture is described here and simulated along with frequency plan considering the most diffused standards in the band from 500 MHz to 6 GHz.

1.Introduction

The increasing number of emerging wireless applications and standards calls for a multi-band and multi-standard radio operation. An approach, which is frequently used in multi-standard wireless devices, employs multiple chips, each one dedicated to a particular communication standard. This approach provides the best RF performance for individual standards, but it significantly penalizes the performance in terms of IC integration and power consumption. Therefore, a single multi-radio transceiver able to fulfil requirements of multiple standards becomes a challenge. Suchlike multi-radio devices should be able to cope with various waveforms and types of modulation (high vs. low Peak to Average Power Ratio PAPR), different average power and power control dynamic range, different frequency of operation and different radio bandwidths (narrow vs. wideband operation). In addition to this, the power consumption becomes a very important issue. Different approaches for efficient multi-radio transmitters have been recently proposed and a lot of research efforts have been put particularly in the reconfigurability of RF components and high power efficiency [1], [2]. Moreover, as the frequency spectrum utilization reveals to be very poor [3], a new paradigm in wireless communications based on the spectrum aware cognitive radio principle becomes widely discussed. In order to adapt to the actual transmission request and the radio spectrum accessibility, the cognitive radio concept will require very high flexibility of RF elements.

One of the most challenging components to design in the flexible multi-band RF front-end is undoubtedly the wideband reconfigurable LO (local oscillator). The LO frequency is used to convert the signal from the baseband to the RF and vice versa and it frequently determines overall performance of the system. In the ideal case, only one LO should be able to deliver the appropriate frequency (in quadrature) with respect to requirements of relevant communication standard and common performance metrics such as phase noise, frequency settling time, spurious output, frequency raster etc. Beside the FDD (Frequency Division Duplex) based communication standards, which require simultaneous LO operation in uplink and downlink directions, an additional LO is needed in cases, where the simultaneous voice and data communication is required (e.g. voice GSM/3G voice communications along with Bluetooth/WiFi/WiMAX data communications). Therefore, a frequency plan that suits to the simultaneous radio operation has to be considered. There have been proposed various techniques for multi-band LO operation, including a reconfigurable ADPLL [4], PLL with wideband or distribute VCO [5], [6] or employing multiple PLL's.

This paper deals with the analysis of a CP (Charge Pump) PLL based frequency synthesizer that combines two different modes of operation (fractional-N and integer-N) accompanied by the loop filter switching technique. Advantages and drawbacks of this approach will be pointed out along with particularities and system performance characteristics of both modes of operation. The first section briefly summarizes RF requirements related to the LO design given by communication standards in the band from 500 MHz to 6 GHz. Next, the overall principle and functionality of proposed multi-band synthesizer are given along with simulations and behaviour analysis of both modes of operation. Subsequently, different modes of operation are proposed and attributed to different communication standards, according to their requirements.

2.Multi-Radio Requirements

Table 1 summarizes LO requirements in terms of the phase noise, settling time and channel raster, given by different communication standards. Stars correspond to more critical requirements. It can be seen, that the most critical requirement in terms of the phase noise and RF channel raster is claimed by the GSM standard. In terms of settling time, Mobile WiMAX (802.16e) calls for the fastest frequency switching performance (more detailed study of LO RF requirements can be found in [7]). These requirements will be considered in the initial design of the synthesizer architecture.

Table 1: LO requirements given by different standards.

Standard	Phase Noise	Settling Time	Ch. Raster
GSM	☆☆☆☆	☆☆	☆☆☆☆
UMTS	☆	☆☆☆	☆
Bluetooth	☆	☆☆☆	☆
802.16e	☆☆	☆☆☆☆	☆☆☆
802.11a/b/g	☆	☆☆	☆

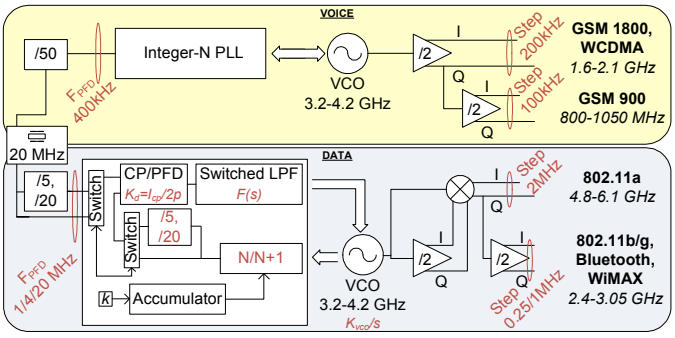

Figure 1: Overall scheme of the proposed multiband frequency synthesizer.

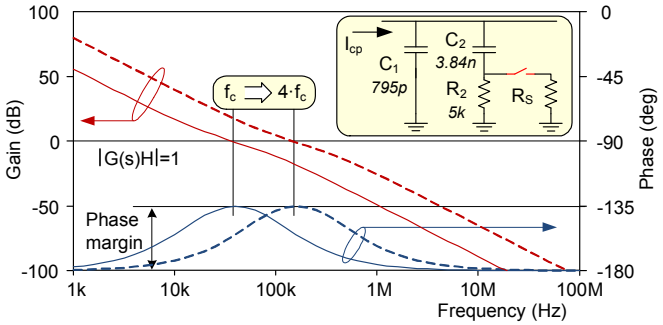

Figure 2: Open loop gain and the phase for variable loop filter. Loop bandwidth has been increased by factor of 4 while the stability remains unaffected (phase margin=46°).

3.Multistandard Operation

Figure 1 presents the overall scheme of the multiband synthesizer. To ensure simultaneous voice and data communications, the multiband synthesizer has been designed for each service separately. The upper LO dedicated to the voice link employs an integer-N PLL, which satisfies GSM/WCDMA LO requirements, while the second LO dedicated to data communication employs a fast hybrid fractional-N/integer-N PLL with switched loop filter. Both PLL circuits use the same 20 MHz crystal reference and moreover, use an identical but separate wideband VCO with capacitor bank operating in the band of 3.2 to 4.2 GHz. This frequency of operation has been chosen due to the use of divide-by-2 prescalers for quadrature signal generation. This approach to the quadrature signal generation offers an accurate I and Q signals with minimal mismatch (when the VCO exhibits an accurate 50% duty cycle [8]), a very low power consumption and savings in terms of the die area compared to quadrature VCO design. Moreover, an important feature is that the VCO frequency is separated from the desired RF frequency, which should prevent pulling of the VCO frequency by the RF output signal of the transmitter [8]. A quadrature balanced mixer has been considered for the quadrature signal generation of 802.11a/b/g, WiMAX (802.16e) and Bluetooth standards. The frequency plan has been chosen according to particular requirements given by multiple standards (RF frequency and channel resolution). Next two paragraphs summarize pros and cons of the integer-N and fractional-N PLL topology. A behaviour analysis of the switched loop filter speed-up mode in association with the fractional-N mode will be presented afterwards.

3.1 Integer-N Mode

The integer-N PLL offers relatively low circuit complexity and low power consumption but at the price of higher in-band noise and worse settling time performance compared to the fractional-N PLL. Nevertheless, integer-N PLL can already fulfil even very high GSM phase noise demands [9].

3.2 Fractional-N with switched loop filter

Fractional-N synthesizers have become very popular and widely used in a range of RF applications because they allow the comparison PFD (Phase Frequency Detector) frequency to be significantly higher than the required frequency resolution. Higher PFD frequency automatically leads to wider loop bandwidth (as the loop BW is to be $< 0.1F_{PFD}$) and therefore significantly improves settling time performance compared to the integer-N PLL. However, the main drawback lies in the overall complexity of additional circuitry for fractional spur reduction (e.g. higher order ΔΣ dithering), which consumes considerable energy and die area. Moreover, a wider loop bandwidth of the PLL results in higher phase jitter and spurious suppression degradation.

Several enhancements to the fractional-N PLL have been published in [8] and [10]. A significant settling time improvement can be achieved by means of loop filter switching. The loop filter is switched to the wideband mode during the frequency transition and then, after a certain programmable period, is shifted back to the normal narrowband value. To understand the switching principle, let us have a look at the PLL control theory and the PLL linearized model. The effect of a closed feedback loop on the input reference signal φ_{in} can be described by the closed loop transfer function T(s) as:

$$T(s) = \frac{\varphi_{out}(s)}{\varphi_{in}(s)} = \frac{G(s)}{1 + G(s)H} = \frac{\frac{K_d K_{vco}}{s} F(s)}{1 + \frac{K_d K_{vco}}{s} F(s) \frac{1}{N}}, \quad (1)$$

where the $G(s)$ represents the open loop transfer function and H corresponds to the division factor $1/N$. K_d is the gain of the CP/PFD detector and equals to $I_{cp}/2\pi$, K_{vco} is the VCO gain in MHz/V and $F(s)$ refers to the transimpedance of the second order loop filter as depicted in Fig. 2.

$$F(s) = \frac{1 + sC_2R_2}{s(C_1 + C_2)\left(1 + s\frac{C_1C_2R_2}{C_1 + C_2}\right)}. \quad (2)$$

The angular open loop crossover frequency ω_c and the phase margin θ_c are defined at the point where the magnitude of the loop gain reaches unity. This can be expressed as $\|G(s)H\| = 1\ (0dB)$, where

$$G(s)H = \frac{K_d K_{vco} F(s)}{sN} = \frac{I_{cp} K_{vco} F(s)}{2\pi sN} \quad (3)$$

$$G(s)H\big|_{s=j\omega_c} = -\frac{I_{cp}K_{vco}}{2\pi\omega_c^{\,2}N}\,\frac{1+j\omega_c T_2}{1+j\omega_c T_1}\,\frac{1}{C_1+C_2}, \qquad (4)$$

and then, the open loop phase margin θ_c at the crossover frequency ω_c reads

$$\theta_c[rad] = \pi + \arctan(\omega_c T_2) - \arctan(\omega_c T_1)\,. \qquad (5)$$

T_2 and T_1 correspond to time constants of zero and the pole in the loop filter transfer function respectively ($T_2=C_2R_2$, $T_1=C_1C_2R_2/(C_1+C_2)$).

Now, let us consider a situation, where the crossover frequency ω_c is increased by factor α in order to increase the loop bandwidth and decrease the settling time. This adjustment is applied only during the frequency transition. To ensure the loop stability at $\alpha\cdot\omega_c$, the phase margin defined by the equation (5) has to remain constant. This can be done by means of reducing the value of T_2 and T_1 by the factor α with help of a parallel resistor R_s as displayed in Fig. 2. Moreover, the product of all elements in (4) has to be increased by factor of α^2 as the angular frequency ω_c in (4) is in the power of two. This can be done by means of increasing the charge pump current I_{cp} by factor α^2 [10]. Another way to increase the product of all elements in (4) by α^2 is by changing the charge pump current I_{cp} along with modifying the division factor N [12]. This approach brings a new degree of flexibility, and moreover, it resolves certain drawbacks of the fractional PLL.

4.Hybrid Mode of Operation and Simulation Results

Due to very high settling time requirements given by the Bluetooth and WLAN/WiMAX standards (< 50µs), the above mentioned technique has been adopted for the branch of the data carrier generation of the multistandard synthesizer, as depicted in Fig. 1. As the fractional-N PLL mode is employed only during the frequency transition, the fractional spurious suppression circuitry commonly needed in fractional-N PLL's does not need to be implemented, which results in a significant power supply and area savings.

The hybrid integer-N/fractional-N PLL has been designed to deliver the most straighten frequency raster of the WiMAX standard (250 kHz). Moreover, the required maximum integrated phase noise of 1° rms has been considered in the loop bandwidth optimization. The frequency applied to the PFD varies between three values. Direct 20 MHz reference is applied to the PFD during the fractional-N speed-up mode. The additional dividers are disabled during this phase. In this mode, various bandwidths of the PLL can be set (resulting wide loop bandwidth is a multiplicative of the reference loop bandwidth by the factor α). The reference loop bandwidth here considered corresponds to the integer-N PLL loop bandwidth during the settled mode and equals to 20 kHz. 20 kHz has been chosen as the optimal value in order to satisfy requirements in terms of the phase jitter imposed by the Mobile WiMAX, which is to be less than 1° rms. This value is critical since the integration frequency can start at about 1/20 of the tone spacing (modulated carrier spacing) and ends up at ½ of the channel bandwidth [13]. Therefore, the integration of the phase noise can start at as low as few hundred Hertz, depending on the FFT size of the OFDM and considered channel bandwidth.

Table 2: PLL parameters as a function of the factor α.

Factor α	$I_{cp(/5)}$; $I_{cp(/20)}$	$R_{(/5)}$ & $R_{(/20)}$	Settling Time (to 10 Hz) [µs]
2	4/5 I_{cp}; 4/20 I_{cp}	$R_2/2$	168
4	16/5 I_{cp}; 16/20 I_{cp}	$R_2/4$	61
6	36/5 I_{cp}; 36/20 I_{cp}	$R_2/6$	38
8	64/5 I_{cp}; 64/20 I_{cp}	$R_2/8$	28

Frequency dividers by 20 and by 5 are employed in the hybrid architecture only during the settled integer-N mode, after the frequency transition. The alternative frequency division enables a dual frequency step of the synthesizer, namely step of 1 and 4 MHz, depending on the choice of the communication standard. 1 MHz step of the PLL applied to the frequency mixture/division circuitry (see Fig. 1) corresponds to the frequency step of 250 kHz required by the WiMAX standard. In order to keep the crossover frequency and the phase margin constant for both integer-N configurations, the charge pump current I_{cp} has to be increased by factor of 4 in the 1 MHz step mode as the division N is increased by the same factor; (I_{cp}=314 µA ⇒ I_{cp}=1.25 mA). This measure enables a simple integer-N PLL reconfiguration without the need of modifying the loop filter components.

To ensure the loop stability during the fractional-N wideband high-speed mode, the PLL parameters I_{cp}, N and R_2 have to be adjusted according to the required bandwidth enlargement factor α, as presented in Tab. 2. $I_{cp(/5)}$ and $I_{cp(/20)}$ represent the resulting charge pump current in the multi-wideband mode comparatively to the charge pump current I_{cp} (charge pump current during the settled integer-N mode). $I_{cp(/5)}$ and $I_{cp(/20)}$ correspond to the required charge pump current for frequency steps of 4 and 1 MHz respectively. The multi-band open loop performance is described in Fig. 3 for four wideband configurations (α=2, 4, 6, 8) as well as for the integer-N set-up. Corresponding settling time performance for different factors α is depicted in Fig. 4. Time to lock to 10 Hz frequency error is presented in Tab. 2.

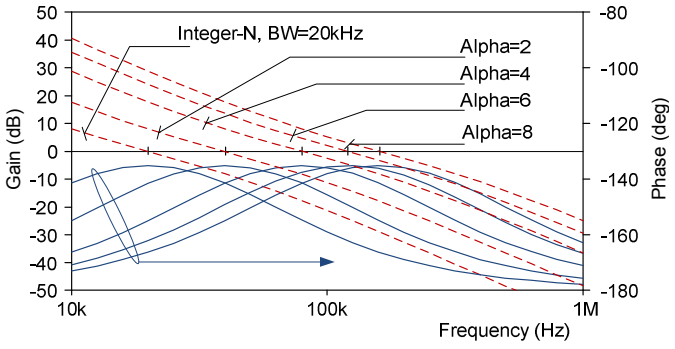

Figure 3: Loop gain (red dashed line) and phase of proposed PLL synthesizer for different factors α. The maximum loop bandwidth 160 kHz is at α=8.

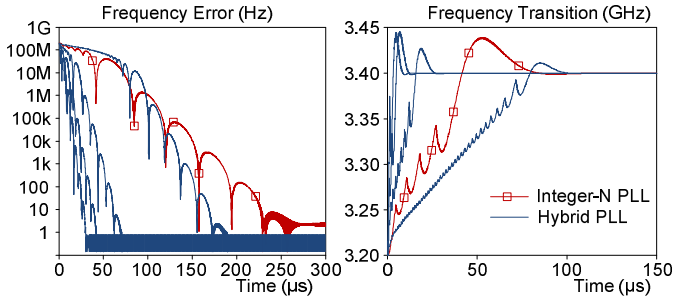

Figure 4: Settling time performance of proposed hybrid synthesizer for different factors α. First figure shows the frequency error in reference to the frequency 3.4 GHz.

Phase noise performance of both loop configurations is presented in Fig. 5. It can be seen, that the in-band phase noise of the integer-N 1 MHz step configuration is deteriorated by 6 dB compared to the 4 MHz step configuration. This is because the comparison frequency of the PFD has been decreased by factor of 4 and at the same time, the division ratio of the PLL has been increased by the same factor, which results in a noise addition to the noise floor, as pointed in (6).

$$L[dBc\ /\ Hz] = PN\ Floor + 10\log(F_{PFD}) + 20\log(N). \quad (6)$$

L is the resulting in-band phase noise, F_{PFD} is the comparison PFD frequency and N is the PLL division ratio. This fact has been considered in the loop bandwidth optimization for the WiMAX 1 MHz step configuration and, as a result, 20 kHz loop bandwidth has been chosen as the optimal value, even though the charge pump current had to be increased significantly (by factor 4 compared to the 4 kHz step mode). The integrated phase noise σ, integrated within the band 400 Hz to 5 MHz has reached 0.48° and 0.76° rms in the 4 and 1 MHz step frequency configuration respectively. It has been found that the required 1° rms phase jitter given by the WiMAX standard has been passed when the loop bandwidth reached 40 kHz. Since the fractional-N wideband mode is employed only during the frequency transition, the phase jitter performance was not an issue.

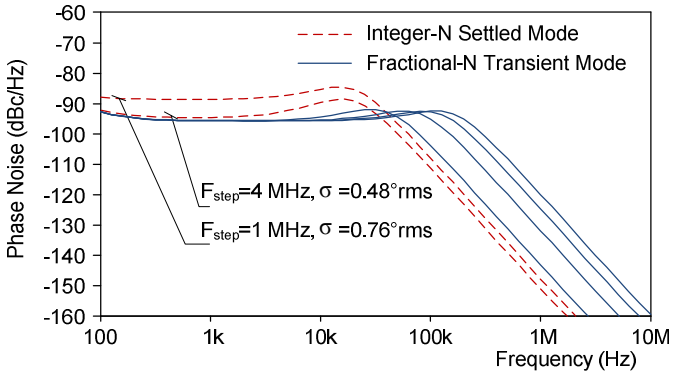

Figure 5: Phase noise performance of proposed hybrid synthesizer for four factors of α and both integer-N configurations at 3.3 GHz.

5.Conclusion

An innovative approach to the multiband frequency synthesis has been studied and simulated. The overall architecture based on the hybrid integer-N/fractional-N PLL with a switched loop bandwidth has been described, including a convenient frequency planning for multiple standards. It has been demonstrated that significant settling time improvement can be achieved by simultaneous optimization of the charge pump current and the division ratio, which in turn results in an important charge pump current reduction compared to the classical switched loop technique. This architecture provides a new protocol of optimization and moreover, a higher degree of flexibility, which results from the simultaneous tuning of the charge pump current and the division ratio.

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