Low temperature Trench IGBT static and dynamic operating modes investigation based on simulation and experiments

Stephane Azzopardi, Adel Benmansour

Low temperature Trench IGBT static and dynamic operating modes investigation based on simulation and experiments

Stéphane Azzopardi

Adel Benmansour

October 2004

Acknowledgements

The authors would like to thank Mr. Masayasu Ishiko from Toyota CRDL and Mr. Hamada Kimimori Toyota Motor for their support and their help during the project.

We would also like to thank the colleagues of Mr. Masayasu Ishiko (Ms. Sachiko Kawaji, Mr. Tomoyuki Shoji and Mr. Takahide Sugiyama) for their advices for the simulation.

Contents

1 Outlines 5
1.1 Introduction 5
1.2 Objectives 5
2 Project schedule 6
3 Background 7
4 Trench IGBT structure description 8
5 Experiments 9
5.1 *Static mode* 9
5.1.1 Equipment 9
5.1.2 Experimental test conditions 10
5.1.3 Test bench 10
5.1.4 Results and discussion 11
5.1.5 Observations 12
5.2 *Switching mode with inductive load* 12
5.2.1 Equipment 12
5.2.2 Power module description 13
5.2.3 Test circuit 14
5.2.4 Test bench 16
5.2.5 Experimental test conditions 17
5.2.6 Methodology 17
5.2.7 Results 18
5.2.8 Observations 35
6 2D Physically-Based Simulation Using ISE 36
6.1 *Equipment* 36
6.1.1 Computer 36
6.1.2 Software version 36
6.2 Static mode 36
6.2.1 Configuration 36
6.2.2 Test conditions 36
6.2.3 Simulation file 37
6.2.4 Simulation results 42
6.2.5 General discussion 47

6.2.6 Simulations troubles 47
6.3 *Switching mode with resistive load* 47
6.3.1 Configuration 47
6.3.2 Test conditions 48
6.3.3 Simulation file 48
6.3.4 Simulations results 49
6.3.5 General discussion 50
6.3.6 Simulations troubles 50
6.4 *Switching mode with inductive load* 50
6.4.1 Configuration 50
6.4.2 Test conditions 51
6.4.3 Simulation file 51
6.4.4 Taking into account thermal effect in physical simulations 55
6.4.5 Simulations results 55
6.4.6 Discussion - Troubles 57
6.4.7 Trial for improving the convergence 58
6.5 *Switching mode with inductive load: improvement of the circuit* 59
6.5.1 Configuration 59
6.5.2 Simulation file 59
6.5.3 Results and discussion 61
6.5.4 *Observations* 61
7 Global Discussion 62
7.1 About the results 62
7.2 About the project organization 62
8 Conclusion 63
9 References 65
10 Annexes 66
10.1 Annex 1: Mitsubishi Power Module data sheet CM150DY-24NF 66
10.2 Annex 2: Power module photography 67
10.3 Annex 3: Concentration profile of CM300DU-12F and CM200DU-24F 68
10.4 Annex 4: SEM and TEM Analysis 69
10.5 Annex 5: Paper 1 submitted to IPEC 05 71
10.6 Annex 6: Paper 2 submitted to IPEC 05 72

1 Outlines

1.1 Introduction

The present project entitled “Low temperature IGBT static and dynamic operating modes investigation based on simulation and experiments” has been elaborated between Masayasu Ishiko, Senoir Researcher at Toyota Central Research Laboratory and Development (CRLD) (Japan) and Stéphane Azzopardi, Associate Professor from the Laboratory IXL of the Graduate School of Engineering ENSEIRB located on the campus of the Bordeaux University (France).

The duration of this project was six months. It started on February 1st 2004 until July 31st 2004.

The main persons (in bold) involved in that project were:

TOYOTA	IXL
Masayasu Ishiko	**Stephane Azzopardi (Associate Pr.)**
Tomoyuki Shoji	**Adel Benmansour (Master)**
Sachiko Kawaji	**Renaud Roy Pelat (Internship)**
	Christian Zardini (Pr.)

Table 1 – Persons involved in the project

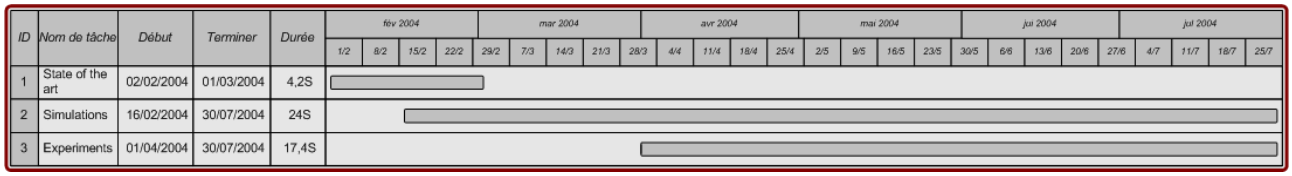
1.2 Objectives

The objectives of this study were to investigate the low temperature Trench IGBT behavior based on simulations and experiments.

On one hand, the goal was to focus on the simulations at low temperature of Trench IGBT using the physically based 2D device simulator from ISE. The basic simulation file was provided by Toyota CRDL. By low temperature, it means a value down to -40°C. On another hand, in addition to simulations, experiments have been carried. The relationship between experiments and simulations permitted to evaluate to behavior of the device at low temperature by pointing out the trends. In each case, static and switching analyses have been studied.

2 Project schedule

The global project schedule is proposed in figure 1.



ID	Nom de tâche	Début	Terminer	Durée
1	State of the art	02/02/2004	01/03/2004	4,2S
2	Simulations	16/02/2004	30/07/2004	24S
3	Experiments	01/04/2004	30/07/2004	17,4S

Figure 1 - Global project schedule

During the first month of the project, the goal was to have an overview of the studies of IGBT at low temperature which were available in the literature. Both simulations and experimental analysis have been selected for the state of the art.

After receiving the basic file (on February 6th) for ISE simulation of a Trench IGBT, data have been implemented in the simulator Dessis© after a purchase of a personal computer. The analysis of the proposed file took about one month in order to have a precise overview of the Trench IGBT structure associated with data sent by Mr. Masayasu Ishiko on February 17th. Then the basic simulations, such as Ic-Vce, Ic-Vge and BVCEO, could start.

In parallel with these simulations, the experimental static test bench has been realized using some Planar IGBT samples available at IXL, and the test on the Trench IGBT sample provided by Toyota CRLD on April 28th could start.

The key point of the project was the switching behavior under inductive load.

A specific test circuit allowed to investigate the switching behavior of the IGBT has been designed which allows to investigate both turn-on and turn-off transients.

At the end of July all planned simulations and experiments were performed. However, a lack of information could not allow to overcome the non convergence of some simulations.

Finally, the present report and the two papers submitted to IPEC 05 at the end of the project have been written.

3 Background

Technical progress in power electronics depends on the development in the fields of power circuit topologies, power devices technologies and control techniques. Since the 80's, significant new developments have been made in the area of power electronics devices, more precisely for the Insulated Gate Bipolar Transistor (IGBT) [1-2]. Widely used for the medium voltage and medium current application ranges (300-1500V/50-300A), for instance motors drives, DC/DC converters, it allows a good trade-off between the switching speed, the on-state voltage drop and the ruggedness [3].

More recently, Hybrid Electric Vehicle like PRIUS started becoming very popular in Japan and US. However, for some countries such as Canada, Russia and even from north European such kind of cars will be submitted to low temperature environment. This condition is stressful for the power hybrid assembly but it is also necessary to wonder what can happen to the power semiconductor devices. It is well known that the switched power becomes higher and higher and IGBTs used in converters are submitted to high temperature changes, which disturb physical parameters of silicon, and change their behavior. In the other way, what can be the behavior of IGBT submitted to low temperature down to -40°C or -50°C?

In the literature it is possible to find some data related to cryogenic operations on power semiconductor devices [4-5-6], but it needs some very specific and quiet expensive equipment. Furthermore, only very few data are available regarding the low temperature operations of Trench-IGBT [7]. We propose to investigate the behavior of Trench IGBT at low temperature from 25°C down to -40°C or -50°C.

First experiments are presented followed by the simulations using the 2D physically-based device simulator from ISE.

4 Trench IGBT structure description

The planar and trench structures of IGBT are depicted in figure 2. Both devices are punch-through type.

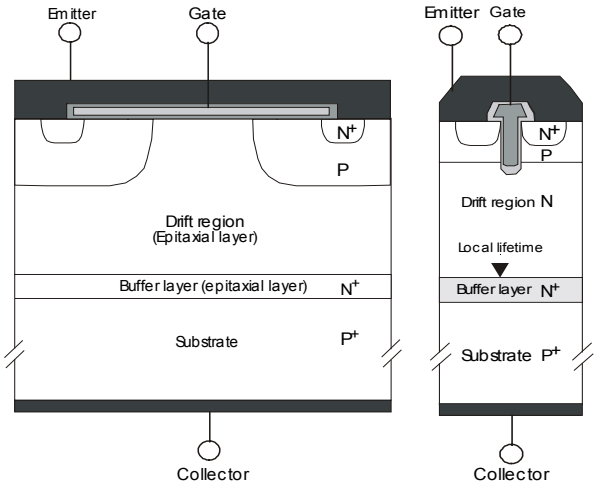


Figure 2 - Devices structure of P- and T-IGBTs

The Planar IGBT is a planar device presenting a small drift region and including a buffer layer. This layer allows to control the minority carriers injection coming from the collector layer. Moreover, the drift region is smaller, and the carriers lifetimes are considerably reduced by using an uniform electron irradiation process in order to improve the switching performances. However, this process is highly sensitive to temperature, and then the increase of the carrier lifetime with the temperature is in part responsible for the rise of the switching losses. The channel, located under the gate oxide, is parallel to the surface of the chip.

As for the Trench IGBT, the gate oxide and conductive polysilicon gate electrode of the device are formed in a deep narrow trench bellow the chip surface. A local lifetime control, using heavy ion irradiation process and allowing to keep a low on-state voltage drop in the drift region, is used. The merit of this process is its low sensitivity to temperature. This structure allows a reduction of the on-state voltage drop by suppressing the JFET resistance which results from the constriction of the current flow in the region between adjacent cells in the planar structure. Furthermore, the vertical channel requires less chips area permitting an increase in cell density. However high current densities can be responsible for high self-heating inducing certainly a low ruggedness.

The Trench IGBT power module used in this study is a CM150DY-24NF from Mitsubishi Power Semiconductor. All the data concerning the Trench IGBT chip and the power module have been provided by Toyota CRLD are presented in Annexes 1 to 4.

5 Experiments

5.1 *Static mode*

5.1.1 Equipment

5.1.1.1 Climatic chamber

An overview is given in figure 3. It allows to vary the temperature from +200°C down to -60°C. Thank to thermocouples placed in the chamber, the temperature is regulated.

Figure 3 – Climatic chamber

5.1.1.2 Curve tracer

The curve tracer TEKTRONIX 371A and a special cable have been used as depicted in figure 4. The cable allows an extension of the device stand which can be located directly in the climatic chamber. The cable can withstand high and low temperature values.

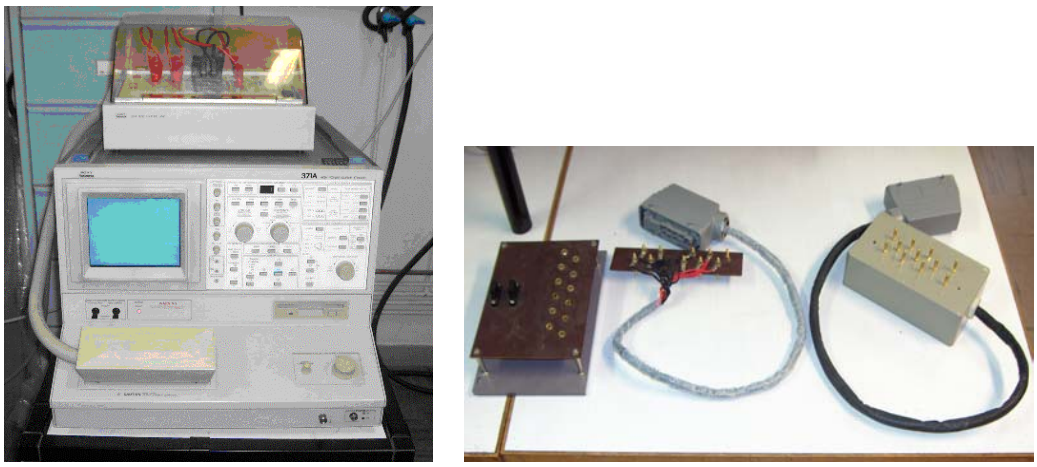


Figure 4 – Curve tracer and the specific cable for high and low temperature measurement

5.1.1.3 Personal computer with Labview

In order to get back the various curves from the curve tracer, an application software based on Labview has been developed. It allows the configuration of the curve tracer for all main power devices and to upload data toward EXCEL.

5.1.2 Experimental test conditions

The test conditions are the same as for the simulations and are summed up in tables 2 to 4.

Rg	**Ic**	**Vce**	**Vg**	**T**
-	-	Δ	[6V to 15V]	[+25°C to -40°C]

Table 2 – Test conditions for Ic-Vce

Rg	**Ic**	**Vce**	**Vg**	**T**
-	-	10V	Δ	[+25°C to -40°C]

Table 3 – Test conditions for Ic-Vge

Rg	**Ic**	**Vce**	**Vg**	**T**
-	-	Δ	-	[+25°C to -40°C]

Table 4 – Test conditions for BVCEO

5.1.3 Test bench

The complete test bench is depicted in figures 5 (a) and (b). The original cable has been exchanged with the specific cable for low temperature measurements.

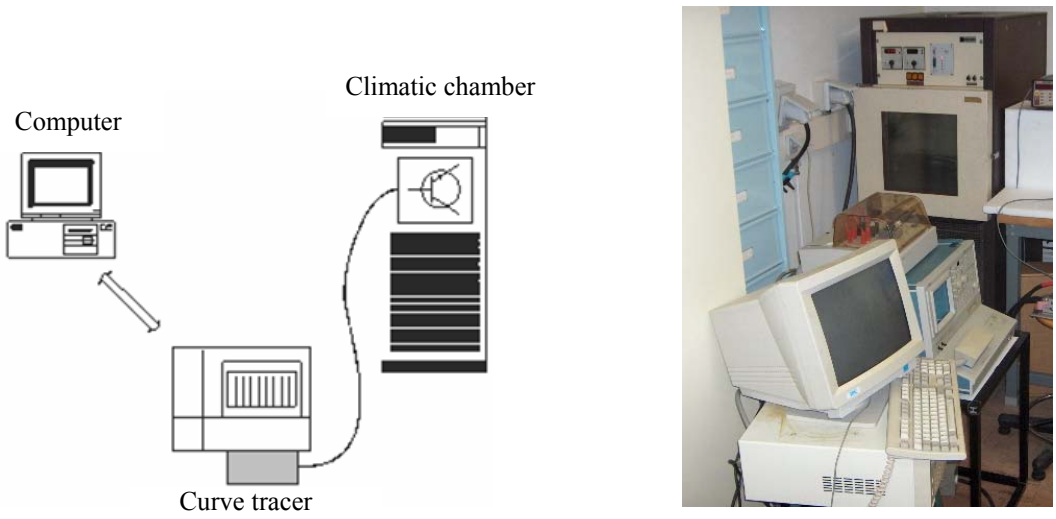


Figure 5 – Description of the complete static test bench (a) schematics and (b) photo

5.1.4 Results and discussion

As it can be observed in figure 6, the dynamic breakdown voltage of the Trench IGBT decreases from 1400V down to 1280V, when the temperature decreases. This phenomenon induces a reduction of the maximum value of the electric field within the structure, as well as the reduction of the depletion region extension. Furthermore, and it can not be possible to see it on this curve, the leakage current also decreases as the intrinsic carrier concentration n_i is reduced. Note that this breakdown voltage variation is also very important for high temperature values.

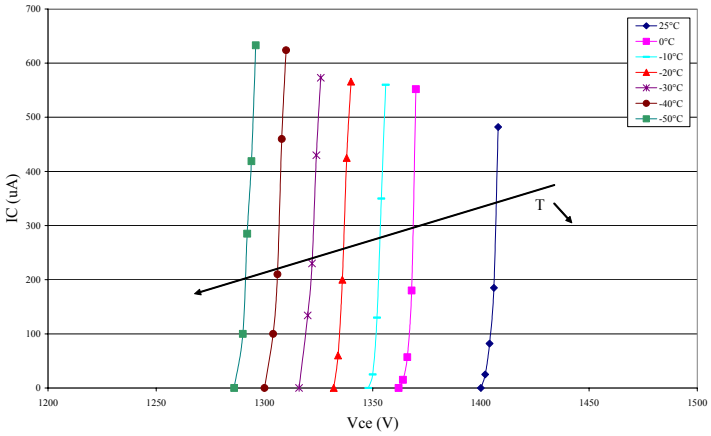


Figure 6 – BVCEO characteristics for T = [25°C down to -50°C]

As depicted in figure 7, it is important to see that a low temperature induces an increase of the threshold voltage as reminded in [7]. This is directly linked to the reduction of the intrinsic carrier concentration n_i when the temperature decreases.

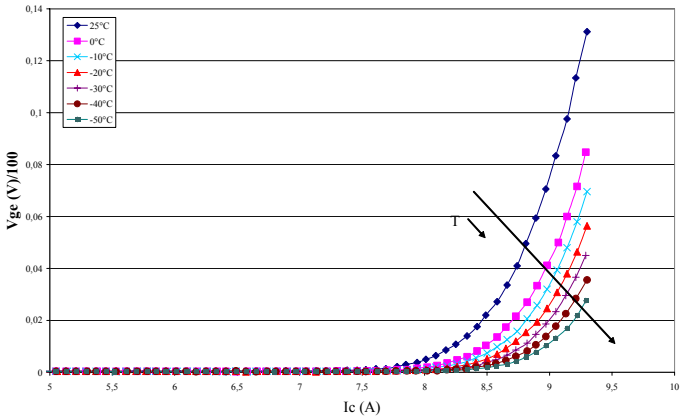


Figure 7 – Ic- Vge characteristics for T = [25°C down to -50°C]

One of the most important effects of the temperature reduction can be analyzed in figure 8 where the gate voltage was about 9.55V. For the given current value, it increases the on-state voltage drop because of the reduction of the current gain of the bipolar part of the IGBT, lowering the minority carrier injection. As a consequence, the conductivity modulation is less effective leading to an

increase of the on-state power losses.

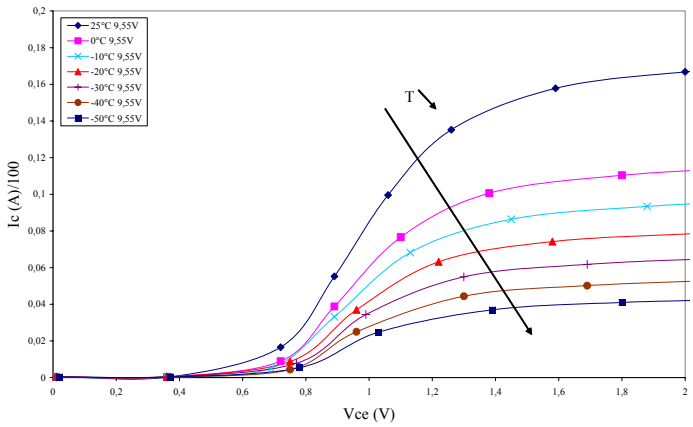


Figure 8 – Ic- Vce characteristics for T = [25°C down to -50°C]

Furthermore, when the temperature decreases, the collector current decreases too. For low doping levels, the carrier mobility in silicon increases with the reduction of the temperature which induces an increase of the saturation current level. However, for the given current level the saturation current is reduced (figure 8). Then it is possible to say that the electron current from the MOS component is not a dominant factor. The decrease of the electron current from the MOS component is higher than the decrease of the current gain of the bipolar component of the Trench IGBT. Furthermore, we may also consider that the gate voltage value is not so high compare to the threshold voltage value and this will have an effect on the device behavior [5].

5.1.5 Observations

The analysis of the static characteristics when the temperature decreases has shown an unusual behavior of the device, especially regarding the Ic-Vce characteristics. We have to keep in mind that the gate voltage was equal to 9.55V, and maybe it could be more interesting to focus on a higher gate emitter voltage. Moreover, these trends are confirmed by the simulations (6.2.4.2).

5.2 *Switching mode with inductive load*

5.2.1 Equipment

5.2.1.1 Climatic chamber

It has been already described in 5.1.1

5.2.1.2 Oscilloscope

The experimental collector-emitter voltage and collector current waveforms of the DUT have been

measured with the voltage probe TEKTRONIX P5050 and the current probe TEKTRONIX TCP220. For the switching power losses measurements, the use of the TEKTRONIX oscilloscope model TDS5054 allowed to compensate the delay between the voltage and the current probes using a calibration source.

5.2.2 Power module description

This study focuses on IGBT dice attached to power modules as described hereafter. However, it is possible to use single IGBT chip package to perform the same test circuit configuration. The power modules which will be used to design this test circuit can be observed on the figure 9.

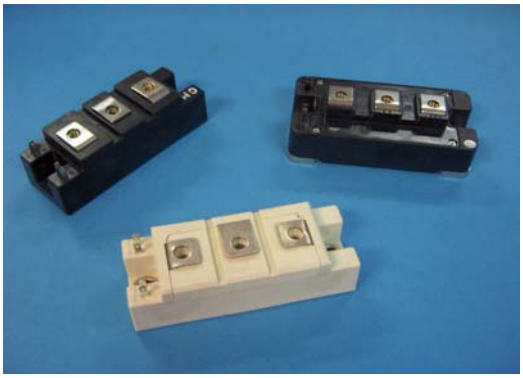


Figure 9 – Single-leg inverter power module external view

Nowadays many manufacturers propose such power module arrangement including two IGBTs and two freewheeling diodes as shown in figure 10. The main advantages come from the reduction of the stray inductance and also the possibility to change in once a full single-leg inverter. The main drawback is that in case of one device fails (diode or IGBT), it is necessary to change the complete module unit.

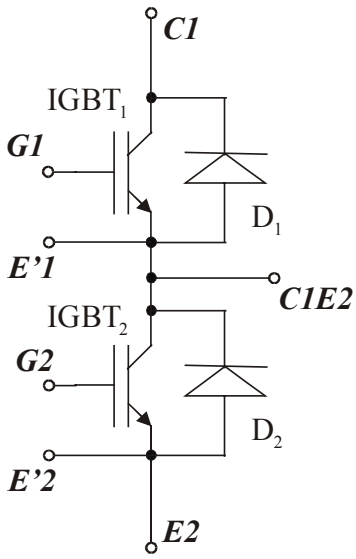


Figure 10 – Single-leg inverter power module arrangement

5.2.3 Test circuit

Power circuit: Based on the power module described in figure 10, and by considering the power devices IGBT2 and D1, and adding some external passive components, it is possible to obtain a first version of the test circuit as depicted in figure 11.

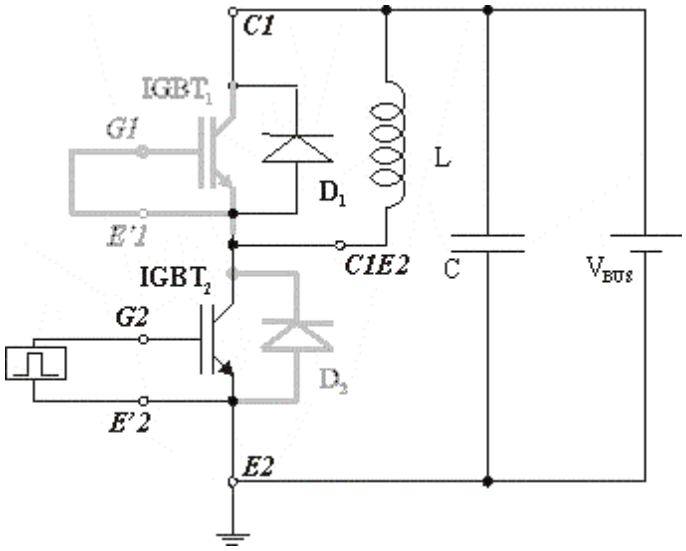


Figure 11 – First version of the test circuit

It can be easy to notice that if this test circuit is used, the measure of the collector current of IGBT2, which is the Device Under Test (DUT), will not be possible since the current of the available connection C1E2 corresponds to the current running through the inductor.

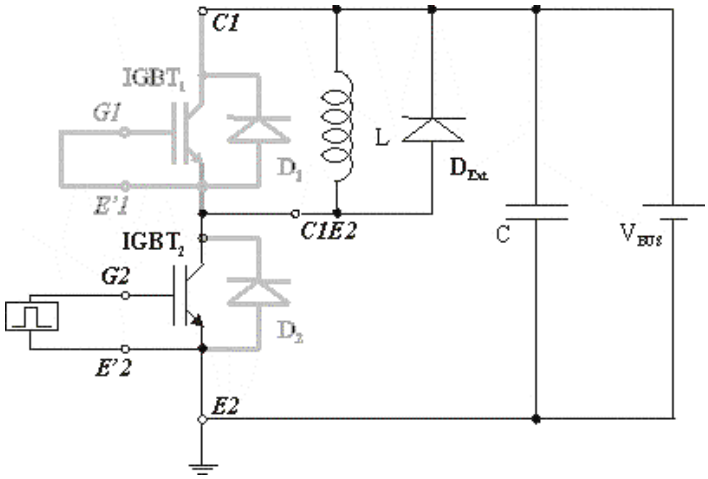


Figure 12 – Second version of the test circuit

This current will be equal to the collector current when the device has been switched on, but it will

be equal to the current of the freewheeling diode when the device has been switched off. Then, the characterization of the DUT will not be fully efficient for turn-on and turn-off. This is the main drawback of using such kind of power module to characterize a power transistor.

In order to obtain the full current waveform of the DUT, it is necessary to add an external diode (Dext) as shown in figure 12. In order to reduce the influence of the reverse recovery phenomenon of the diode, it is highly recommended to use a Schottky diode.

Finally, figure 13 illustrates the test circuit design: very simple and does not need so many external devices.

Figure 13 – Power test circuit

Command circuit: The command circuit has been developed with the help of a PIC microcontroller. It is easy to set up the various pulse durations thanks to a keyboard as shown in figure 14.

Figure 14 – Command board

Also as it can be seen in figures 15 and 16, two kinds of pulse configurations can be selected.

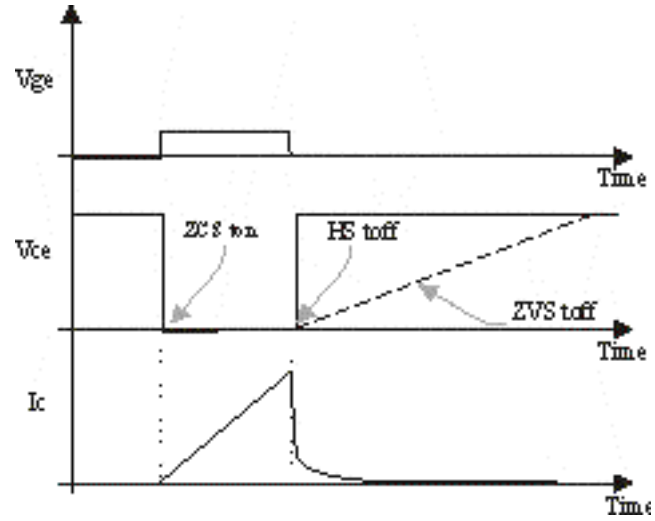


Figure 15 – Single-pulse configuration

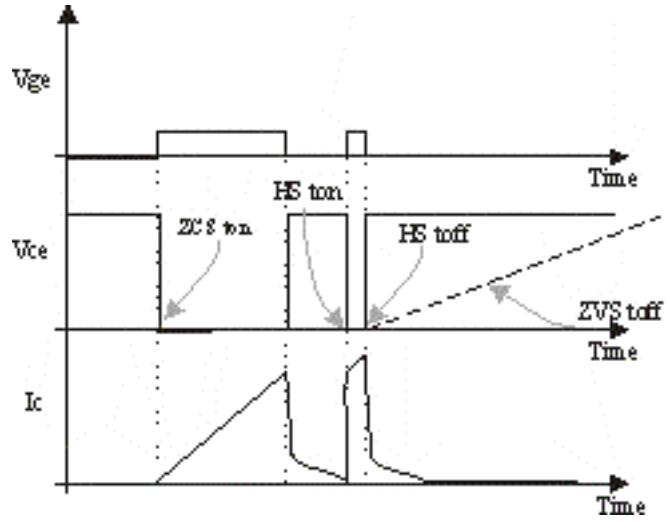


Figure 16 – Double-pulse configuration

The first one allows to switch the device on and off under a single or repetitive pulse based on a specific period. The main drawback is that only the hard switching turn-off, the zero-voltage switching turn-off by adding an external capacitor to the test circuit and the zero-current switching turn-on can be studied. It is not possible to focus on the hard-switching turn-on.

The second configuration permits to have a second pulse applied to the gate electrode which can afford a study of all previous switching modes but also the hard switching turn-on. It has to be noticed that the second pulse should be as short as possible if the user wants to keep a constant current for turn-on and turn-off.

5.2.4 Test bench

The complete test bench for the hard switching including the climatic chamber, the oscilloscope and

the test circuit is depicted in figure 17. The test circuit has been placed in the climatic chamber including the capacitor. However, the inductance was placed externally to facilitate the connection of the current probe and also to avoid the low temperature having an influence on the core properties.

Figure 17 – Overview of the complete switching test bench

5.2.5 Experimental test conditions

The test conditions are indicated in table 5. Due to the low temperature limit of the capacitor the lowest experimental temperature has been fixed to about -40°C. Furthermore, two gate resistance values have been chosen for the test. It could be interesting to investigate a wider range of gate resistance value to see the influence of this external parameter on the device behavior. The value of the collector current has intentionally been limited to 20A. This is due on one hand to the limitation of the capacitor as it will be shown hereafter, and on the other hand that it was difficult to arrange a high current safety test bench using the climatic chamber. Also we focused only on inductive load.

Temperature	Gate Resistance	Current	Load type
25°C, 0°C, -10°C, -20°C, -30°C, -40°C	2.2Ω, 4.7Ω	5A, 10A, 15A, 20A	inductive

Table 5 – Test conditions hard switching

5.2.6 Methodology

Since the test circuit is inserted in a climatic chamber, all the external components, and especially

the capacitor, have to withstand the lowest temperature. In our case, a -40°C low temperature limit capacitor has been used. Furthermore, during the switching measurements, it could not be possible to leave the current and voltage probes inside the climatic chamber since it is not recommended to use them under 0°C. As a consequence, to obtain experimental waveforms, it was necessary to open the window of the climatic chamber, to connect the probes and to send the pulse as quick as possible. Then the probes could be removed until the next measurement.

5.2.7 Results

The whole hard-switching transient has been divided in three parts: turn-on, on-state and turn-off phases. The full waveforms observation is also presented.

5.2.7.1 Influence of the temperature on the collector current and collector-emitter voltage

The figures 18 (a), (b), (c) and (d) to 21 (a), (b), (c) and (d) illustrates the collector current and the collector emitter voltage waveforms for a gate resistance equal to 2.2 Ω and a current load varying from 5A to 20A. At first sight, we have to notice that the turn-on is not so "clean" since there are lots of oscillations. The connection wire has been carefully realized but we had to manage also the placement of the module inside the climatic chamber. Also it can come from the decoupling capacitor characteristics which may not be so good for such application especially when the current load is high and the temperature is low as it will be pointed out hereafter. It is true that the choice of the capacitor was not optimized.

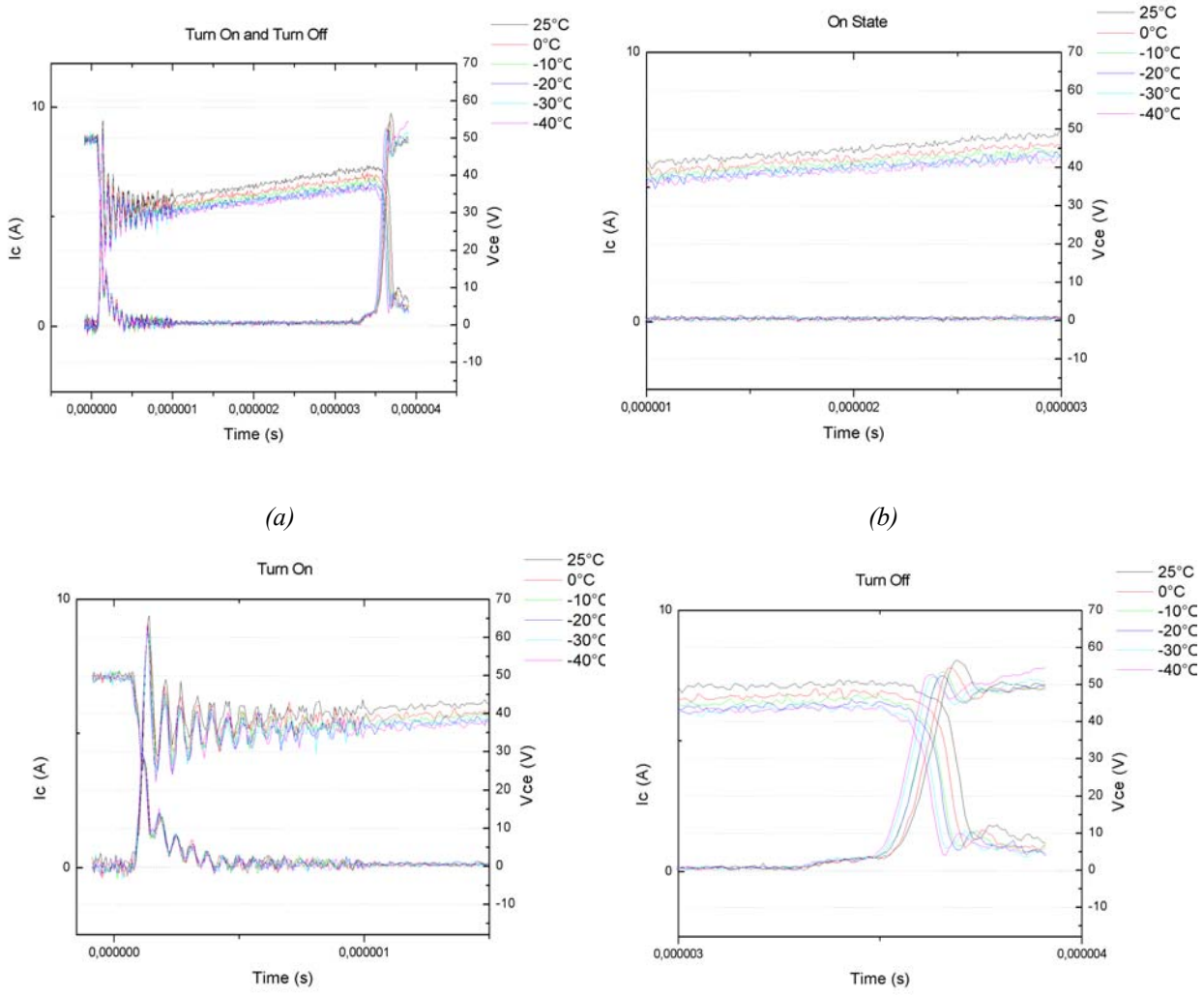
By considering figures 18(c), 19(c), 20(c) and 21(c) showing the turn-on, it can be noticed that the temperature variation does not influence so much the device behavior. Mainly the IGBT is governed by the MOSFET component during the turn-on transient which is not so sensitive to the temperature variation. The current overshoot is meanly due to the reverse recovery phenomenon of the freewheeling diode. The figures 20(c) and 21(c) illustrate the weakness of the decoupling capacitor since at -30°C and -40°C, the current could not ramp to 20A. The low temperature modifies the thermal properties of the capacitor and this component behaves abnormally. Furthermore, the collector emitter voltage is also affected by this weakness.

The on-state waveforms depicting by figures 18(b), 19(b), 20(b) and 21(b) illustrate the reduction of the collector current when the temperature decreases. This aspect is in relation which the static device behavior. The on-state voltage stays relatively low and does not change so much with the temperature reduction.

The turn-off transient illustrating in figures 18(d), 19(d), 20(d) and 21(d) give several information on the IGBT behavior. First it can be seen that the current tail is not so strongly affected by the

temperature. In fact, for low temperature, the gain of the bipolar component is already low and a reduction of the temperature does not affect at all the component. It can be observed that the di/dt and the dv/dt are slightly modified by the reduction of the temperature. However for a collector current value equal to 20A and a temperature equal to -30°C and -40°C the waveforms are dramatically disturbed. We suppose again that the component responsible for that is the decoupling capacitor and not the DUT itself since the current ranking of the IGBT module is 150A and the current load is only 20A. At least we can also notice that the turn-off occurs earlier for low temperature.

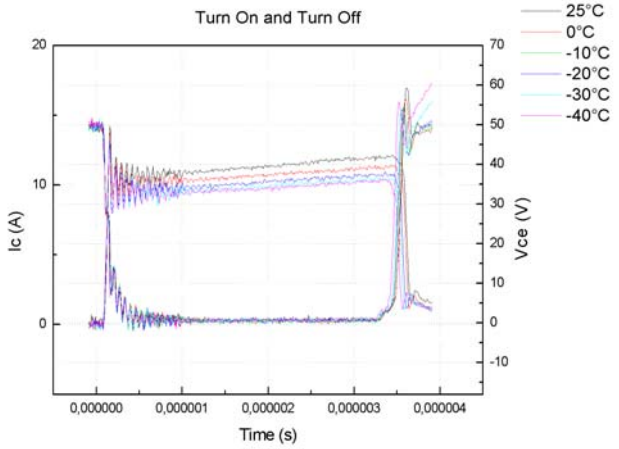
The figures 22 (a), (b), (c) and (d) to 25 (a), (b), (c) and (d) illustrates the collector current and the collector emitter voltage waveforms for a gate resistance equal to 4.7 Ω and a current load varying from 5A to 20A. The same comments can be made on the influence of the temperature on the collector current and collector-emitter voltage waveforms.



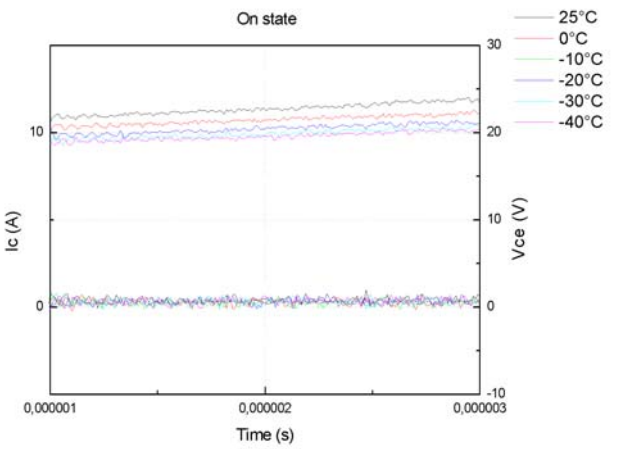
(a) *(b)*

(c) *(d)*

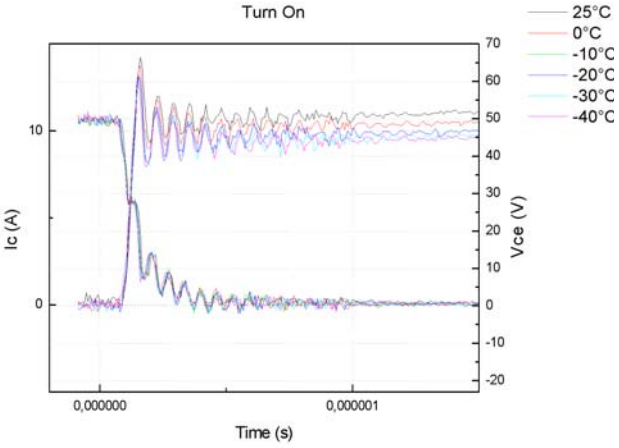
Figure 18 – Hard-switching for T = [25°C down to -40°C], Rg=2.2 Ω and Ic=5A
(a) full waveforms (b) on-state (c) turn-on and (d) turn-off



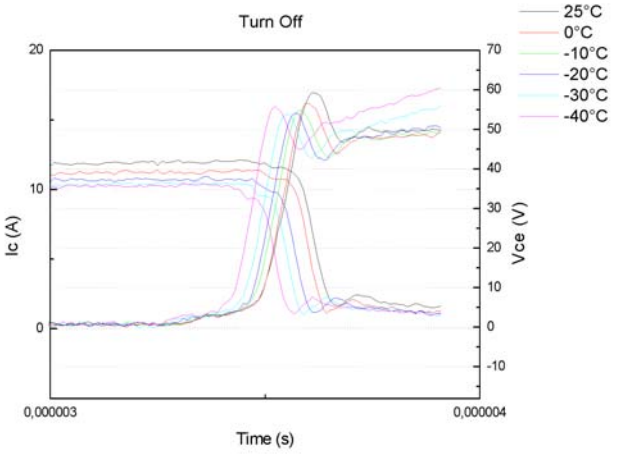
(a)



(b)

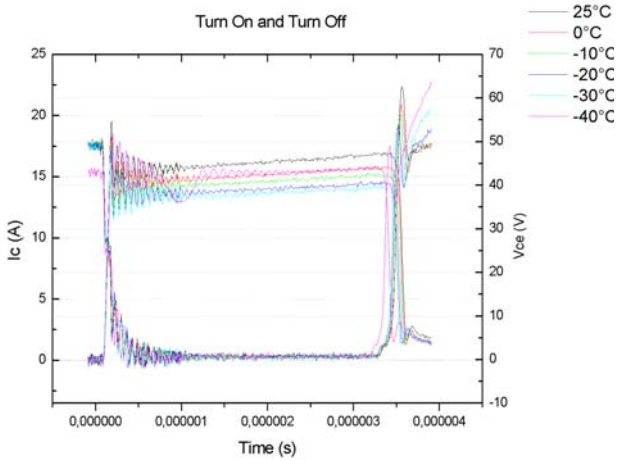


(c)

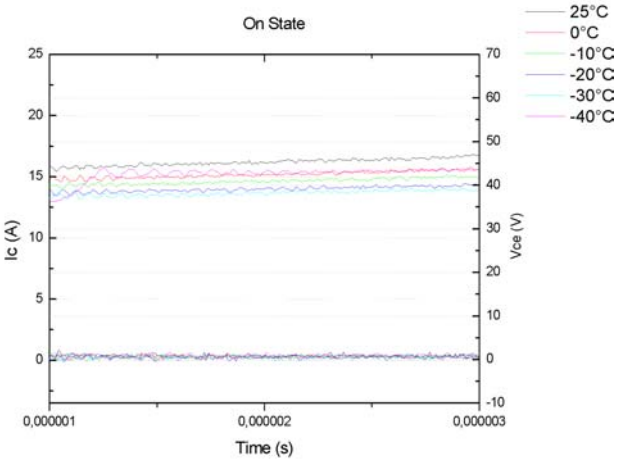


(d)

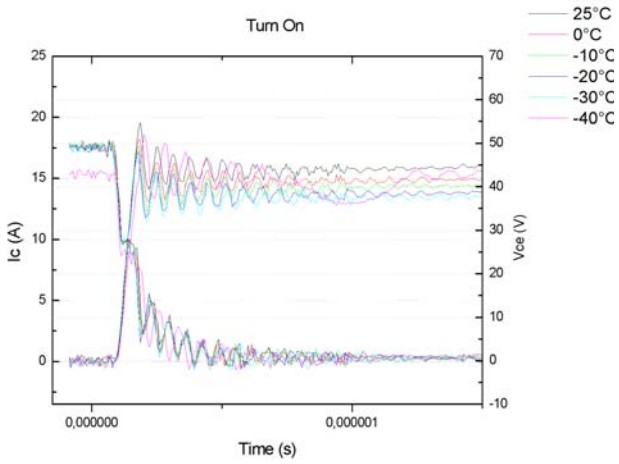
Figure 19 – Hard-switching for T = [25°C down to -40°C], Rg=2.2 Ω and Ic=10A
(a) full waveforms (b) on-state (c) turn-on and (d) turn-off



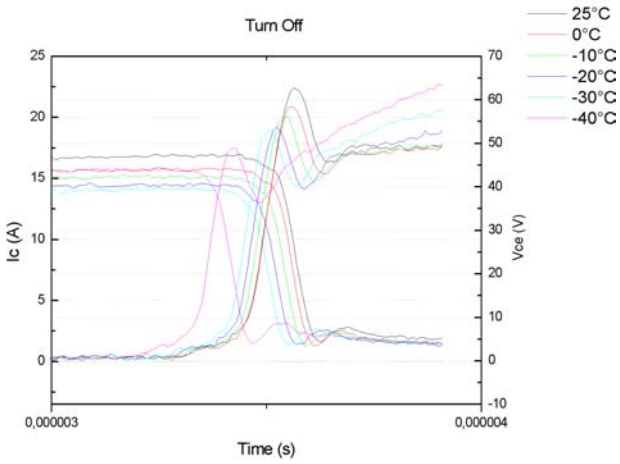
(a)



(b)

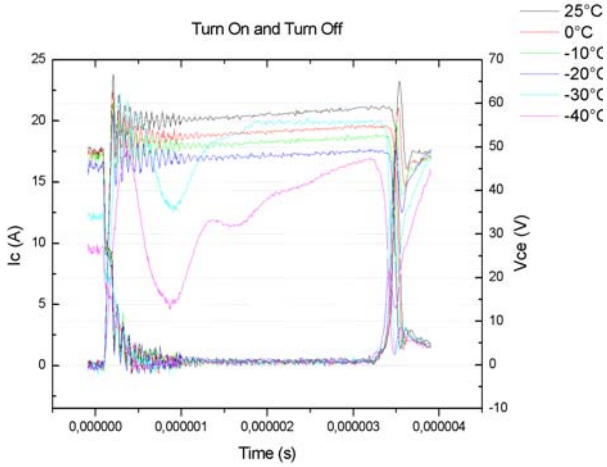


(c)

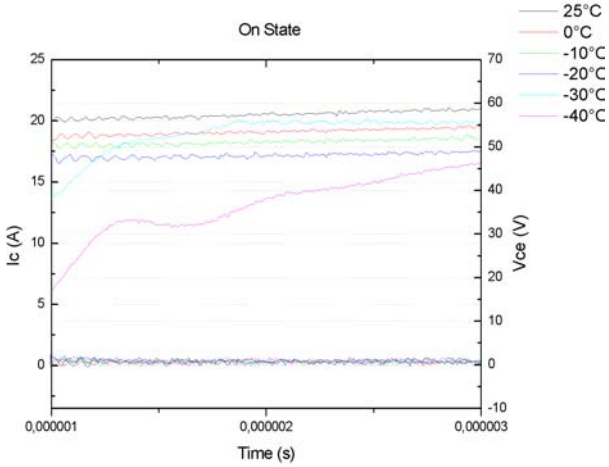


(d)

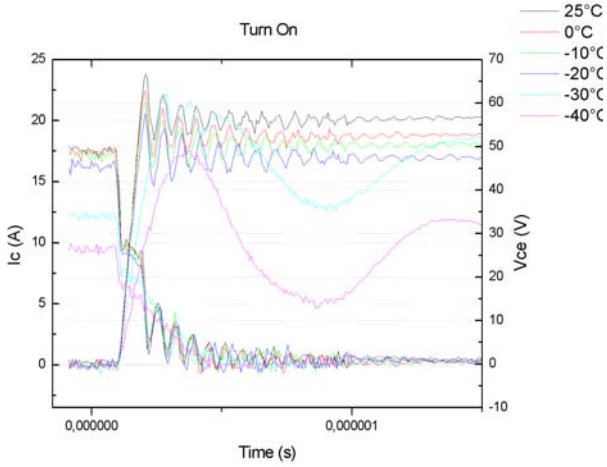
Figure 20 – Hard-switching for T = [25°C down to -40°C], Rg=2.2 Ω and Ic=15A
(a) full waveforms (b) on-state (c) turn-on and (d) turn-off



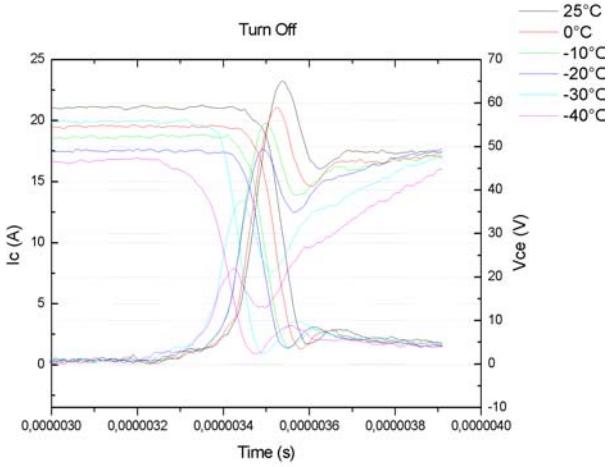
(a)



(b)

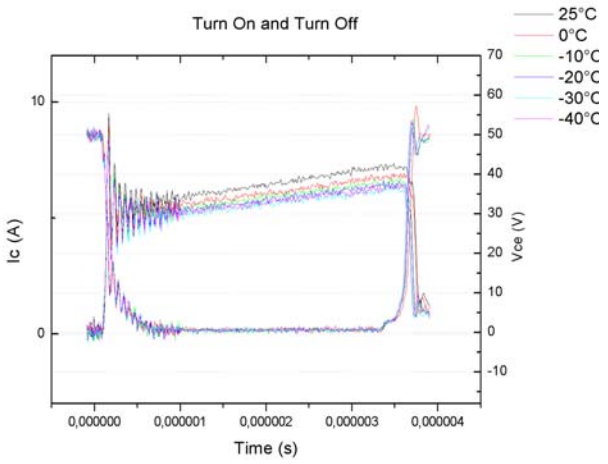


(c)

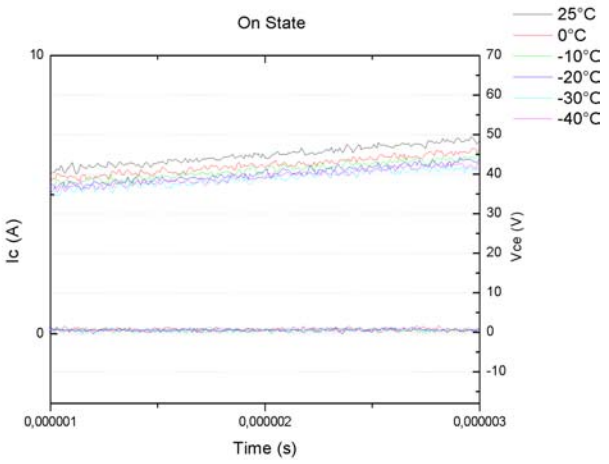


(d)

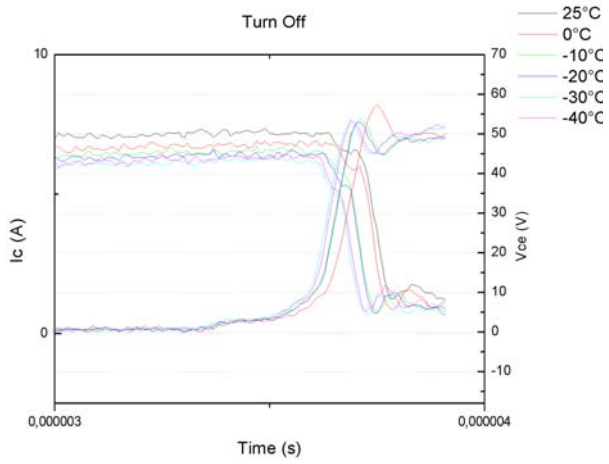
Figure 21 – Hard-switching for T = [25°C down to -40°C], Rg=2.2 Ω and Ic=20A
(a) full waveforms (b) on-state (c) turn-on and (d) turn-off



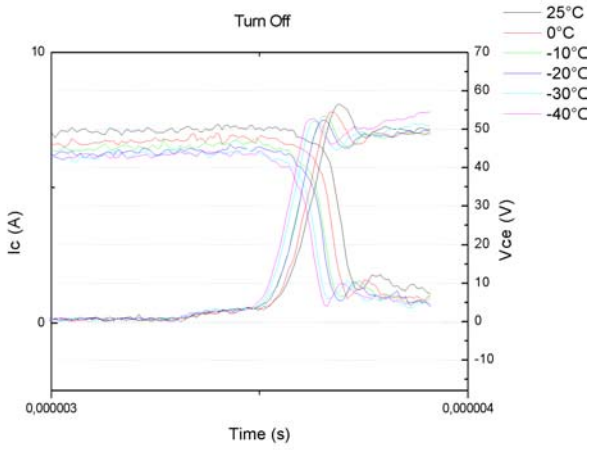
(a)



(b)

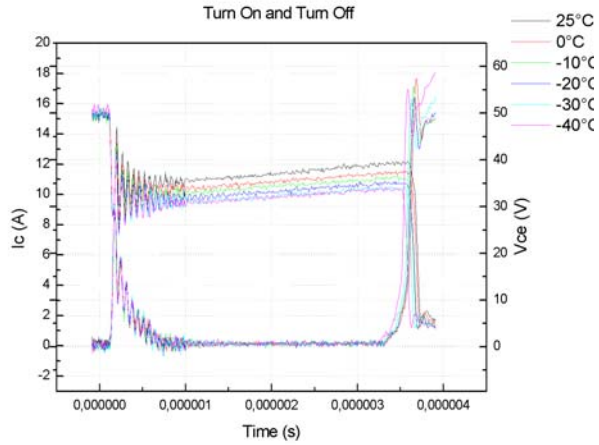


(c)

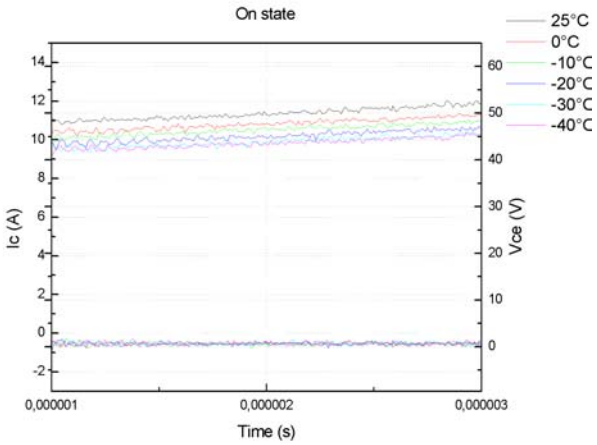


(d)

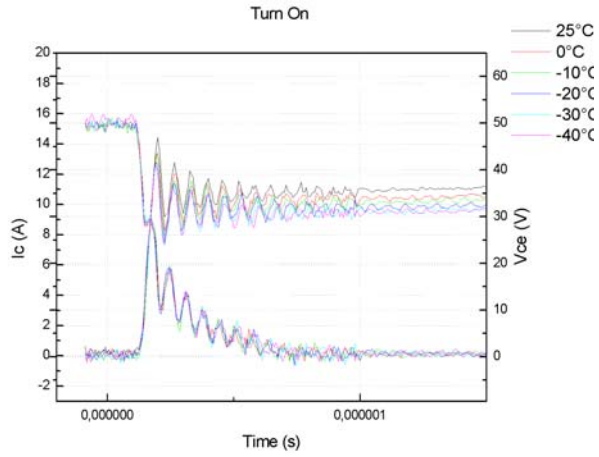
Figure 22 – Hard-switching for T = [25°C down to -40°C], Rg=4.7 Ω and Ic=5A
(a) full waveforms (b) on-state (c) turn-on and (d) turn-off



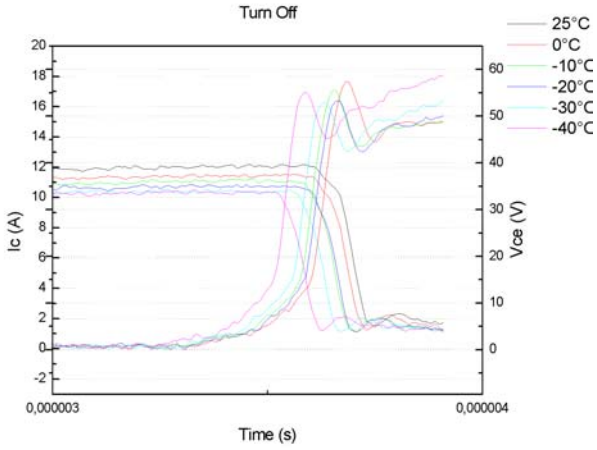
(a)



(b)

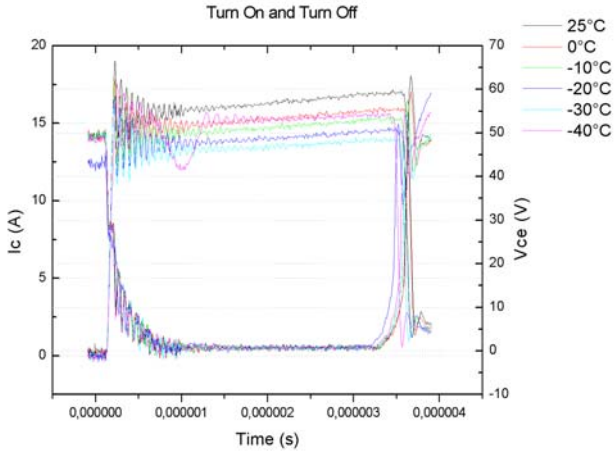


(c)

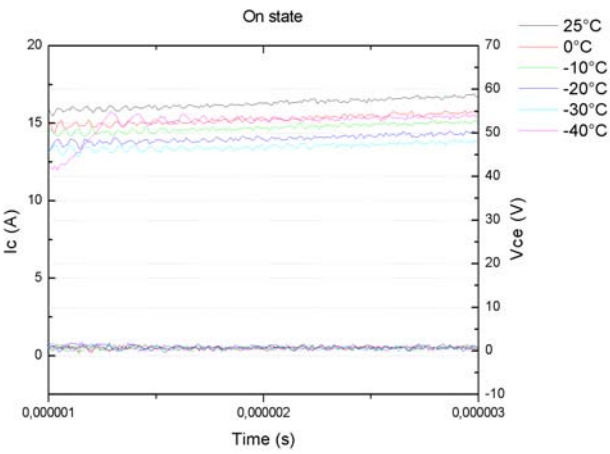


(d)

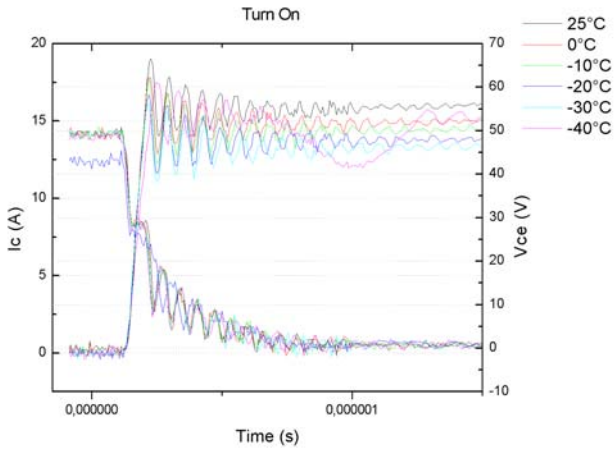
Figure 23 – Hard-switching for T = [25°C down to -40°C], Rg=4.7 Ω and Ic=10A
(a) full waveforms (b) on-state (c) turn-on and (d) turn-off



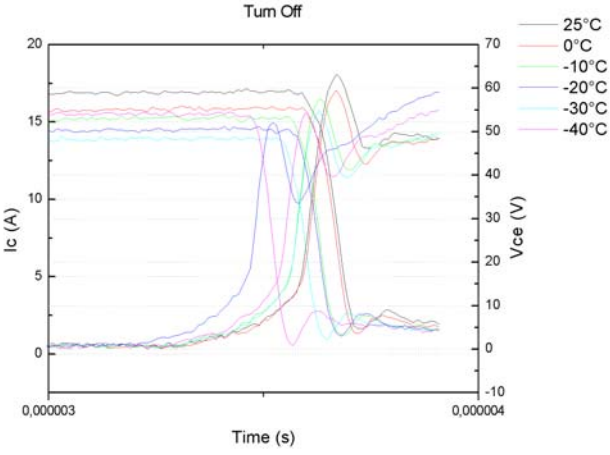
(a)



(b)



(c)



(d)

Figure 24 – Hard-switching for T = [25°C down to -40°C], Rg=4.7 Ω and Ic=15A
(a) full waveforms (b) on-state (c) turn-on and (d) turn-off

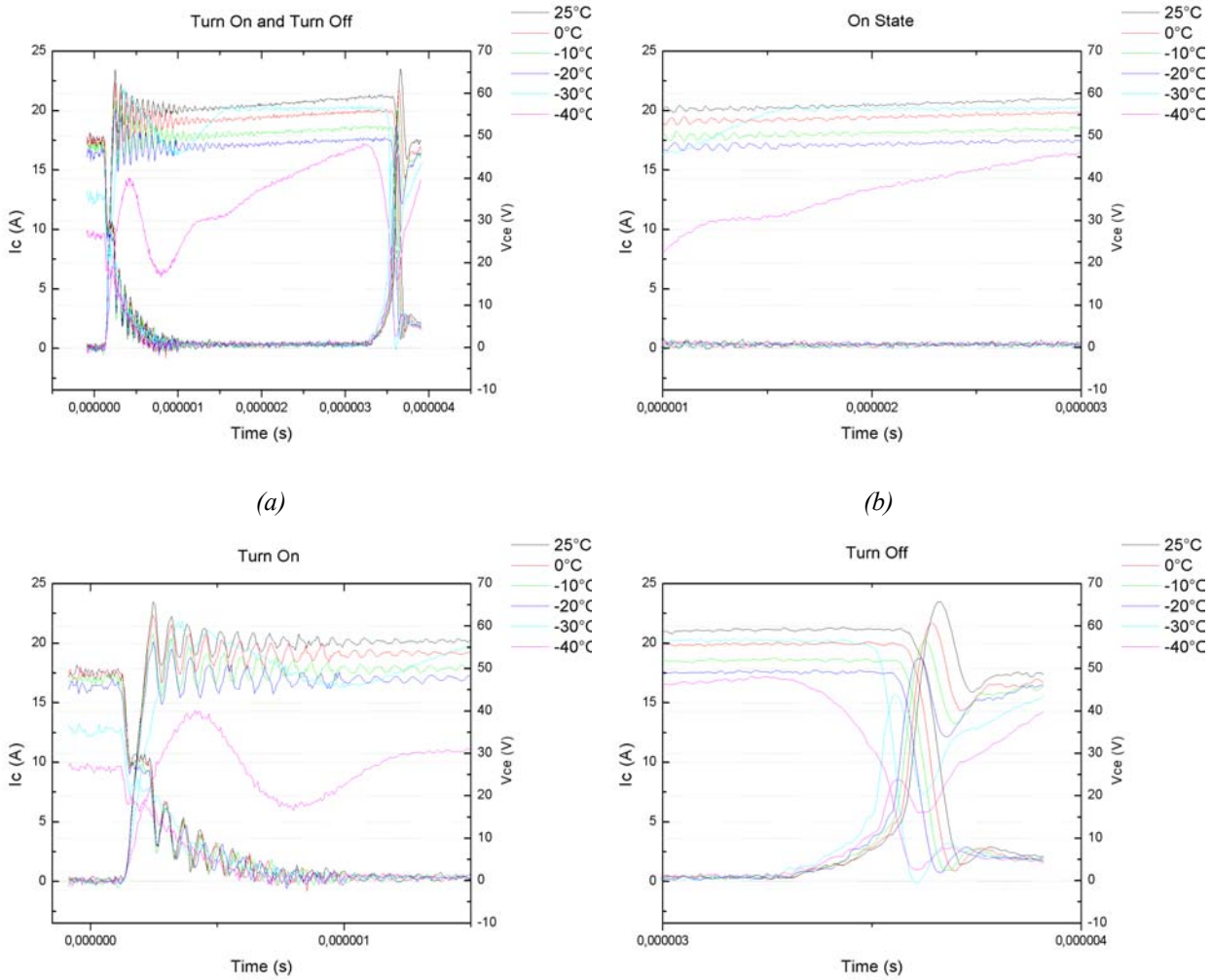


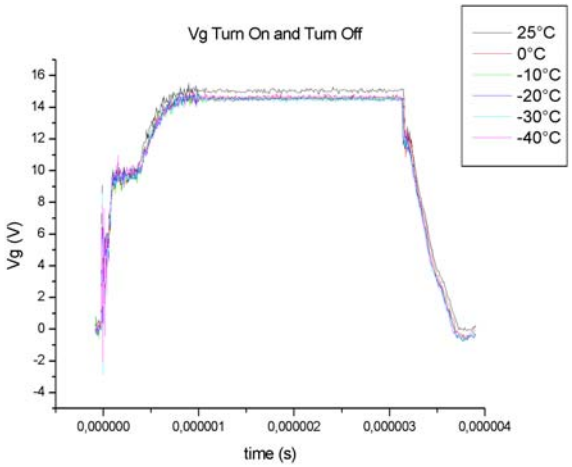
Figure 25 – Hard-switching for T = [25°C down to -40°C], Rg=4.7 Ω and Ic=20A
(a) full waveforms (b) on-state (c) turn-on and (d) turn-off

5.2.7.2 Influence of the temperature on the gate-emitter voltage

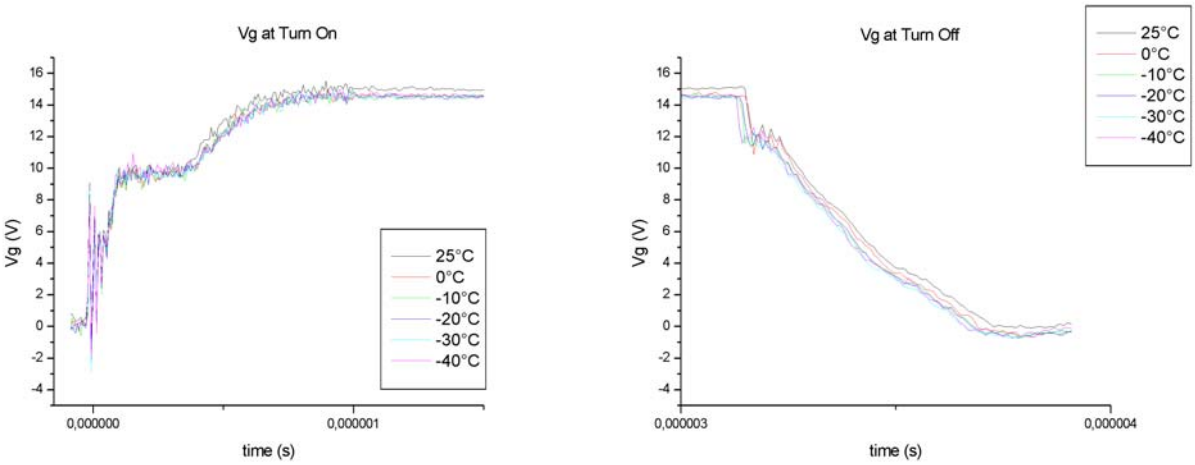
The figures 26 (a), (b) and (c) to 29 (a), (b) and (c) illustrates the gate emitter voltage waveforms for a gate resistance equal to 2.2 Ω and a current load varying from 5A to 20A, whereas the figures 30 (a), (b) and (c) to 33 (a), (b) and (c) illustrates the gate emitter voltage waveforms for a gate resistance equal to 4.7 Ω for the same current load conditions.

At first sight it can be noticed that the temperature does have a dramatic influence on these waveforms. When considering the turn-on waveforms for both gate resistance values (figures 26(b), 27(b), 28(b), 29(b), 30(b), 31(b), 32(b) and 33(b)), there is no change. The turn-off waveforms illustrates the same trends except for the turn-off waveforms for a temperature of –40°C and a current load of 10A, 15A and 20A, as depicted in figures 27(c), 28(c), 29(c), 31(c), 32(c), 33(c). Even if the gate resistance value becomes higher, the low temperature induces an earlier turn-off of

the gate-emitter voltage. This has a direct effect on the collector current and collector emitter voltage waveforms inducing an earlier turn-off.

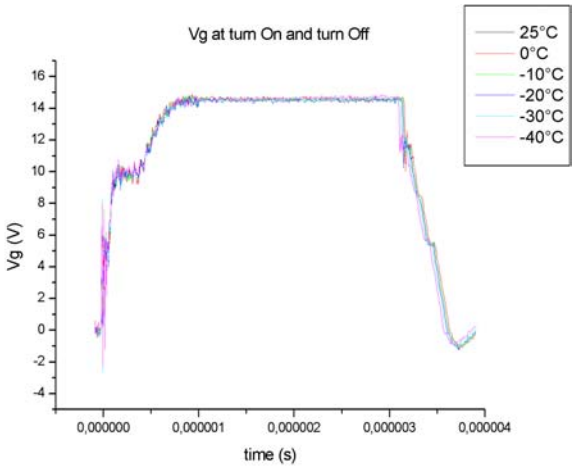


(a)

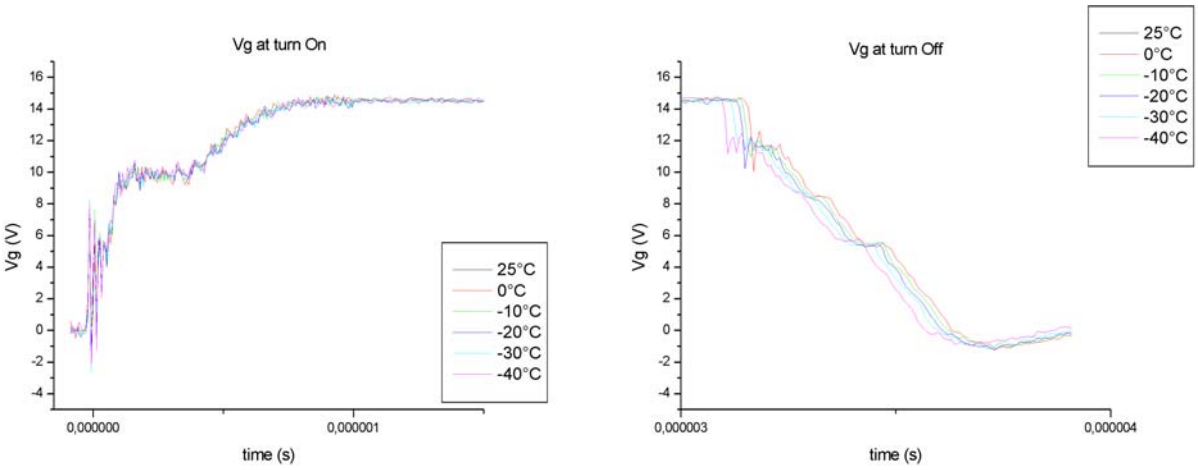


(b) *(c)*

Figure 26 – Hard-switching for T = [25°C down to -40°C], Rg=2.2 Ω and Ic=5A
(a) full waveforms (b) turn-on and (c) turn-off

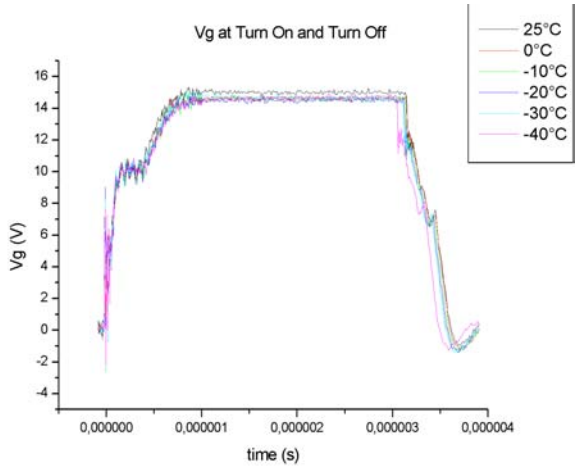


(a)

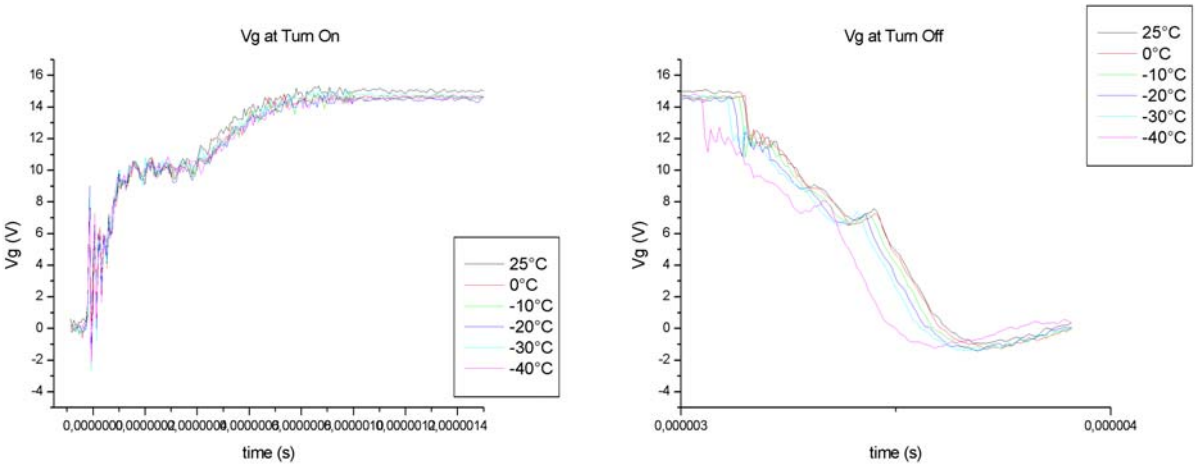


(b) *(c)*

Figure 27 – Hard-switching for T = [25°C down to -40°C], Rg=2.2 Ω and Ic=10A
(a) full waveforms (b) turn-on and (c) turn-off

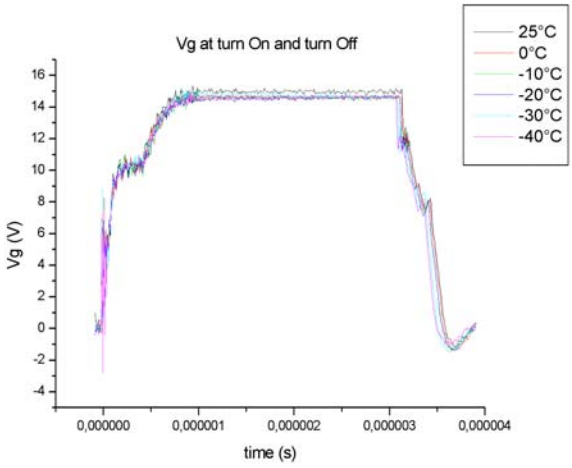


(a)

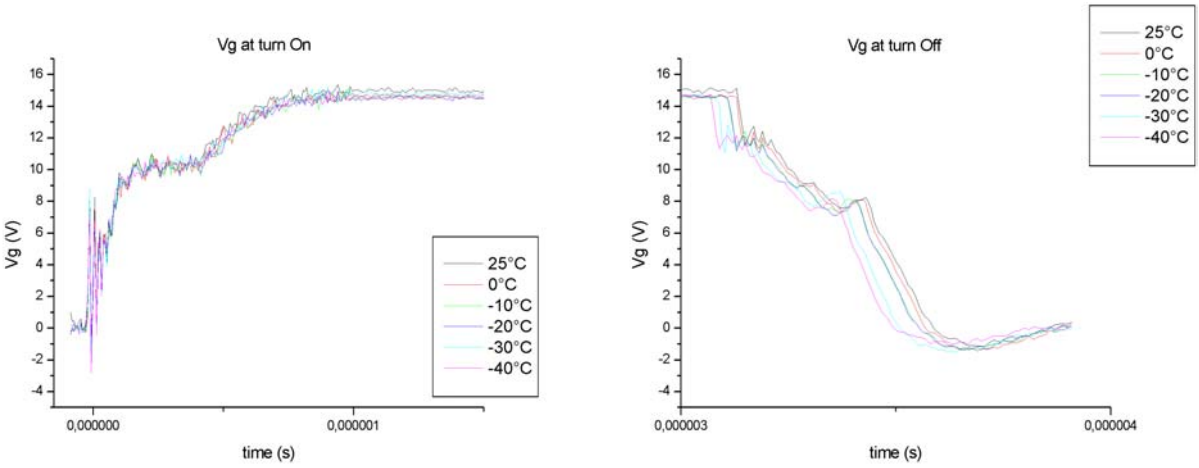


(b) *(c)*

Figure 28 – Hard-switching for T = [25°C down to -40°C], Rg=2.2 Ω and Ic=15A
(a) full waveforms (b) turn-on and (c) turn-off

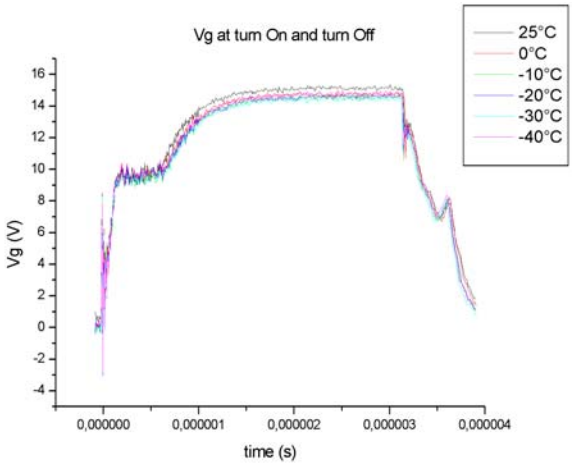


(a)

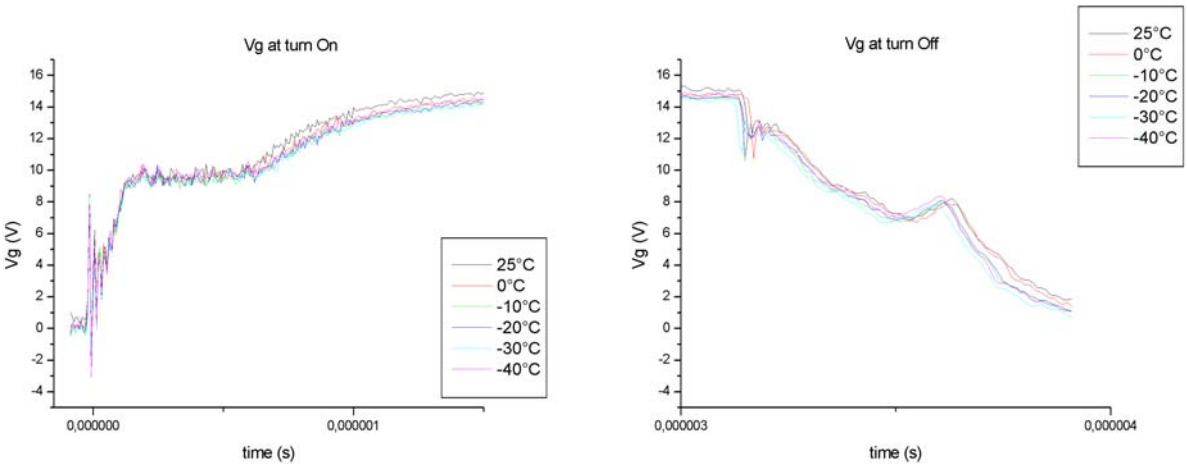


(b) *(c)*

Figure 29 – Hard-switching for T = [25°C down to -40°C], Rg=2.2 Ω and Ic=20A
(a) full waveforms (b) turn-on and (c) turn-off

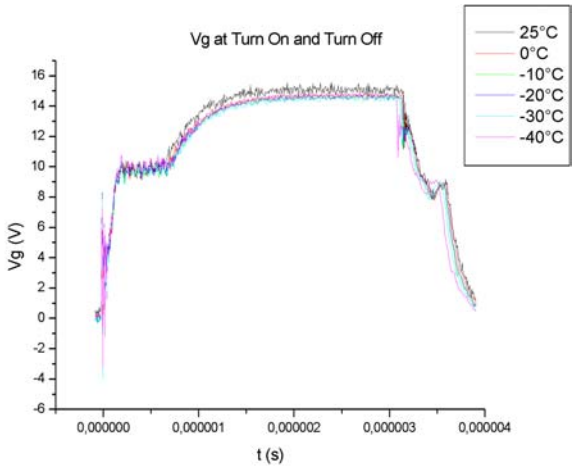


(a)

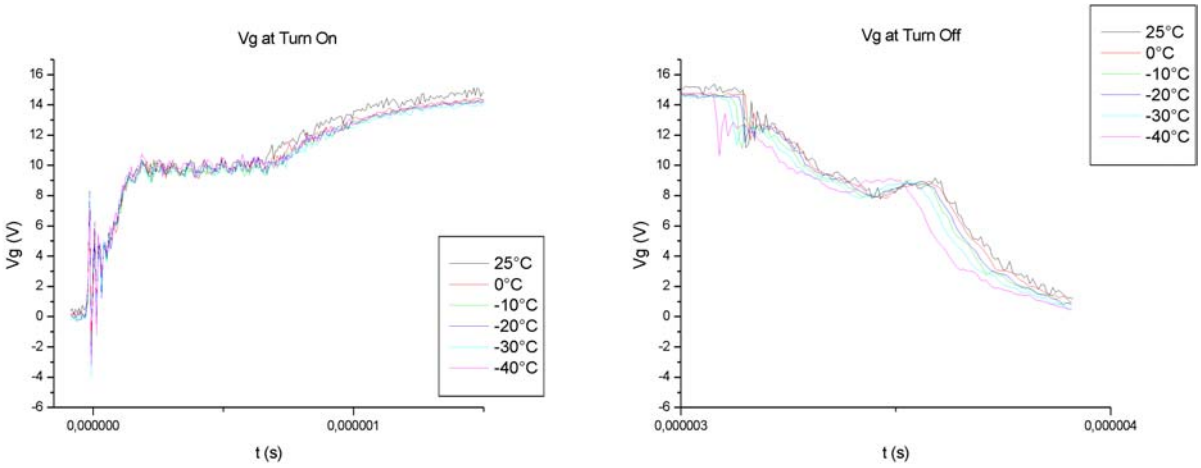


(b) *(c)*

Figure 30 – Hard-switching for T = [25°C down to -40°C], Rg=4.7 Ω and Ic=5A
(a) full waveforms (b) turn-on and (c) turn-off

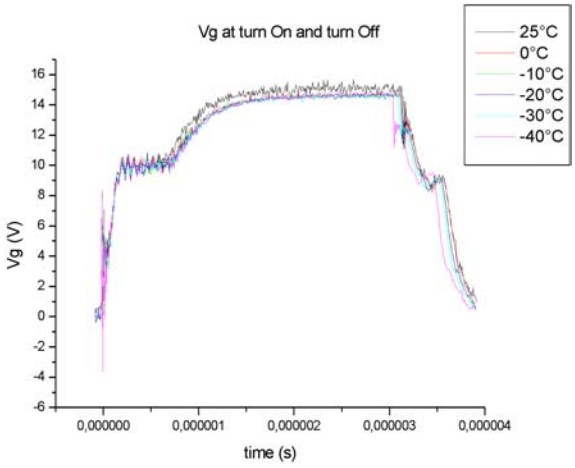


(a)

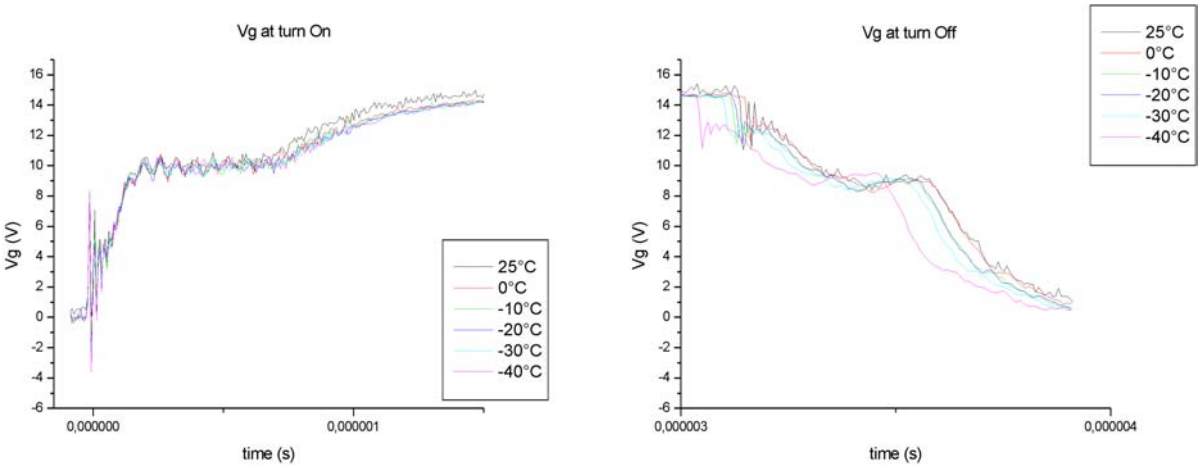


(b) *(c)*

Figure 31 – Hard-switching for T = [25°C down to -40°C], Rg=4.7 Ω and Ic=10A
(a) full waveforms (b) turn-on and (c) turn-off

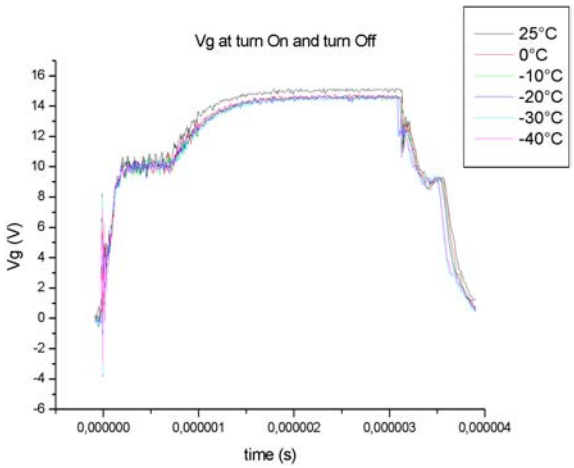


(a)

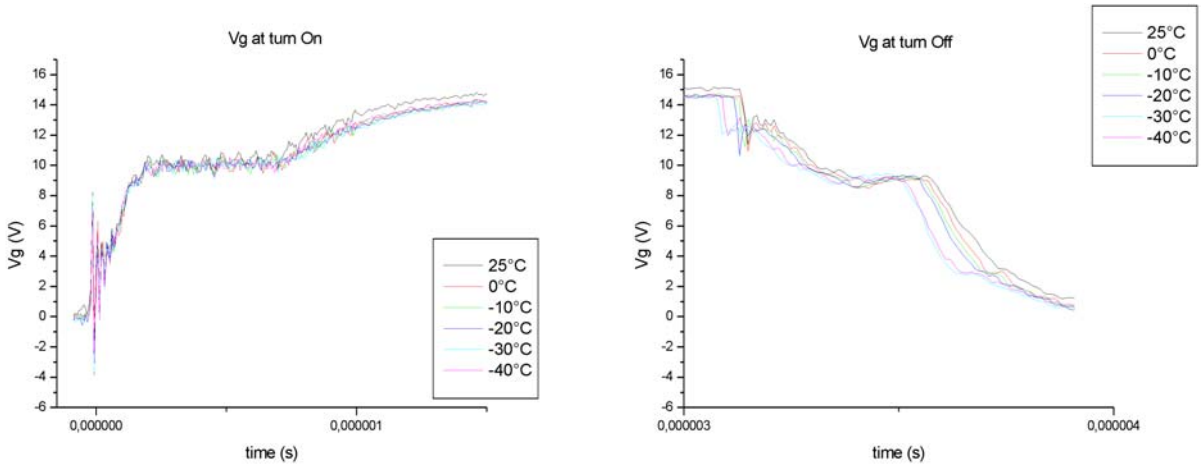


(b) *(c)*

Figure 32 – Hard-switching for T = [25°C down to -40°C], Rg=4.7 Ω and Ic=15A
(a) full waveforms (b) turn-on and (c) turn-off



(a)



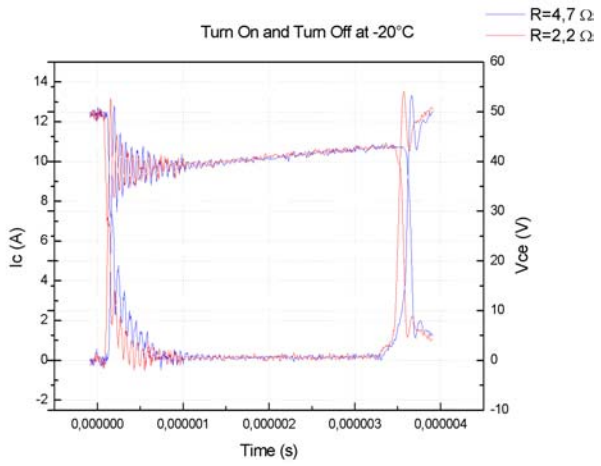
(b) *(c)*

Figure 33 – Hard-switching for T = [25°C down to -40°C], Rg=4.7 Ω and Ic=20A
(a) full waveforms (b) turn-on and (c) turn-off

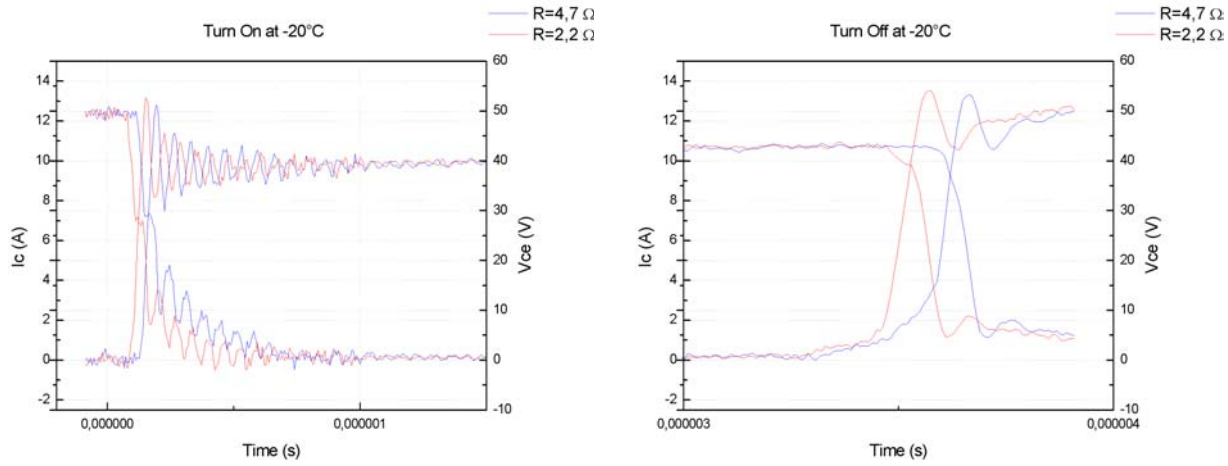
5.2.7.3 Influence of the gate resistance on the collector current, the collector-emitter voltage and gate-emitter voltage

The collector current and the collector-emitter voltage waveforms are quiet the same as for a gate resistance equal to 2.2 Ω or 4.7 Ω except that the switching transients are a little bit delayed and also that the oscillation are reduced. The effect of the gate resistance variation can be observed in figures 34 (b) and (c) for the turn-on and turn-off respectively. For the turn-on, the effect of the gate resistance variation is to delay the transient of the device but also changes slightly the di/dt. The turn-off is also influenced by the gate resistance variation. The turn-off transient is delayed but also has a little effect on the dv/dt.

When we focus on the gate-emitter voltage waveforms (figure 35 (a), (b) and (c)), it is obvious to see that the higher gate resistance value changes dramatically the shape of the voltage. First it induces a higher turn-on transient due to the Miller effect as depicted in figure 35(b), then the plateau is longer reducing the switching time and the establishment of the requested load current especially if this current is high. During the turn-off phase, it is also clear that as indicated in figure 35(c), the reduction of the gate pulse is delayed. These gate resistance considerations on gate device are well known and its value has to be precisely determined in order to use the device in the best configuration.

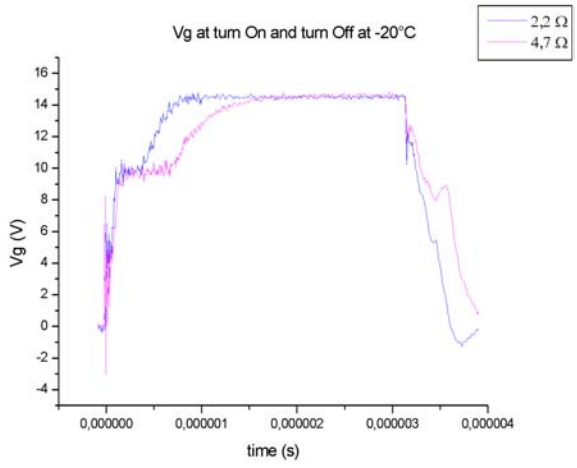


(a)

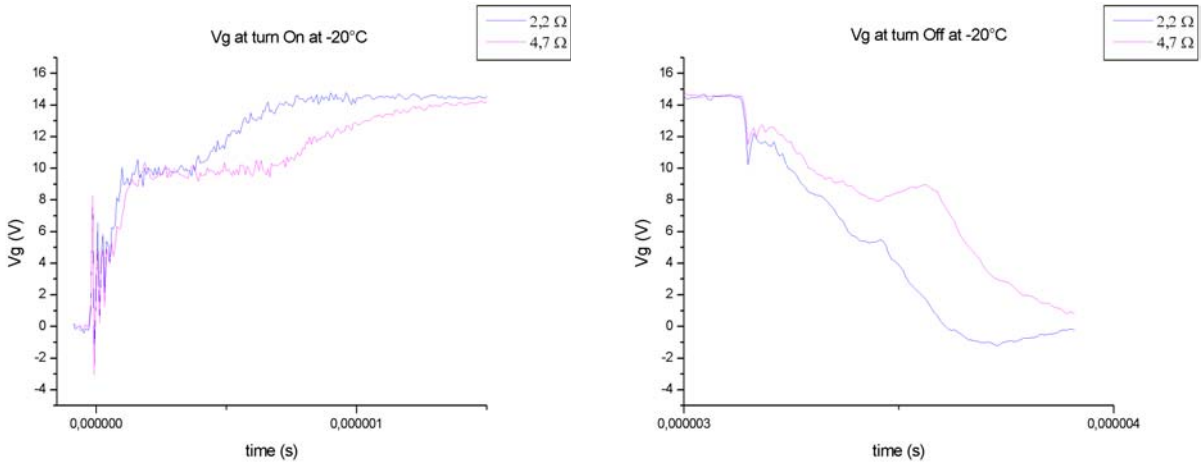


(b) *(c)*

Figure 34 – Hard-switching for Rg = [2.2 Ω and 4.7 Ω], Ic =15A and T=-20°C (collector current and collector-emitter voltage)
(a) full waveforms (b) turn-on and (c) turn-off



(a)



(b) *(c)*

Figure 35 – Hard-switching for Rg = [2.2 Ω and 4.7 Ω], Ic=15A and T=-20°C (gate-emitter voltage)
(a) full waveforms (b) turn-on and (c) turn-off

5.2.7.4 Power losses

To estimate the losses during the switching, we just took into consideration the instantaneous peak power for both turn-on and turn-off as depicted in figure 36. We did not consider the energy but only the instantaneous peak power. The use of the oscilloscope TEKTRONIX TDS5054 allows to compensate the current and voltage probes to get an accurate value of the current-voltage product.

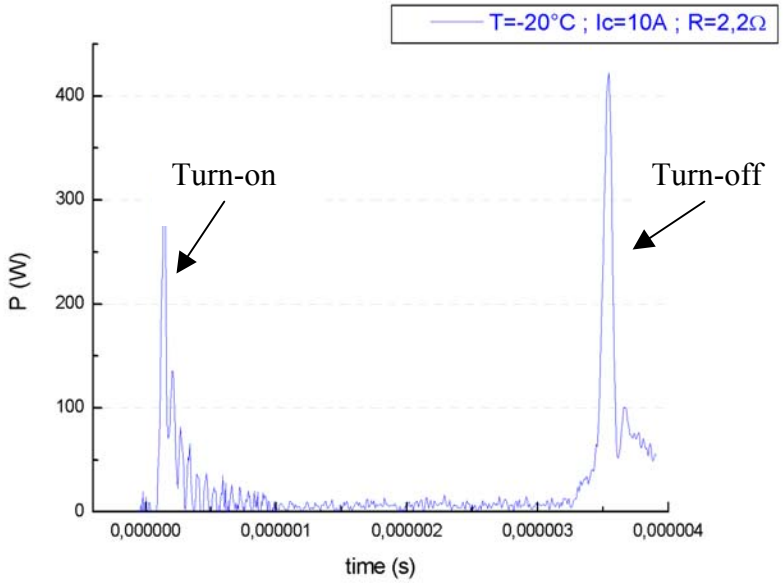


Figure 36 – Instantaneous peak power during transient for T=-20°C, Ic=10A and Rg = 2.2 Ω

All the instantaneous peak powers have been computed during the measurements and these data are presented in table 6 and 7 for two values of the gate resistance.

	Rg=2,2 Ω							
	Turn-on				Turn-off			
	5A	10A	15A	20A	5A	10A	15A	20A
25°C	228.8	358.8	473.2	561.6	326.4	582.4	820.8	1034
0°C	215	327.6	430	494	280.8	499.2	699.6	850
-10°C	225	265.2	425.6	480	275.4	385.4	630	747
-20°C	213.2	315	395.2	432.4	248.4	441	556.8	616
-30°C	210	316.8	399.6	494	250	423	547.2	850
-40°C	212.8	310	357	158.4	240	438.6	537.6	195

Table 6 – Instantaneous peak power for Rg=2.2 Ω

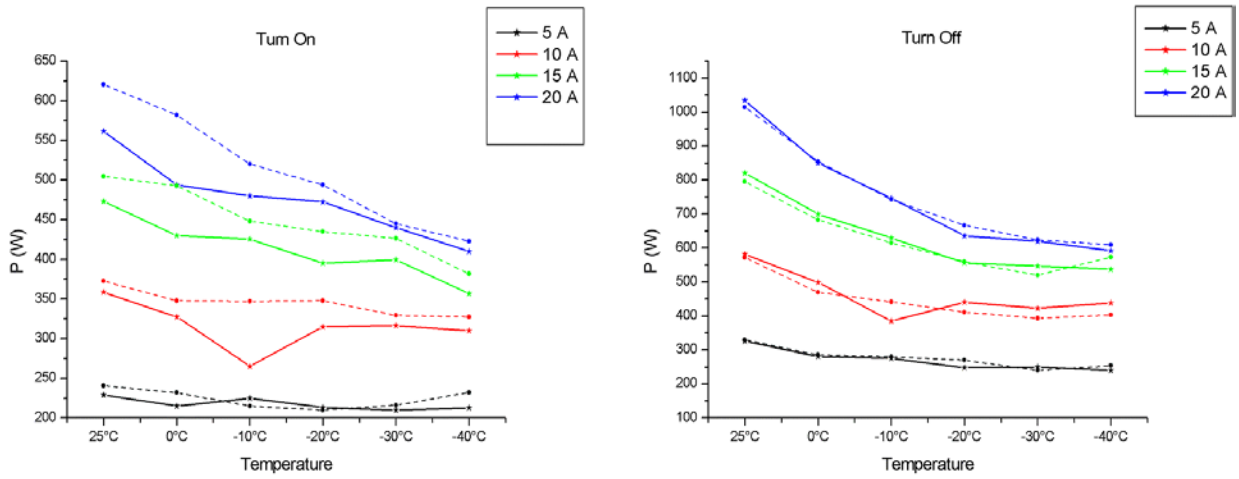
	Rg=4,7 Ω							
	Turn-on				Turn-off			
	5A	10A	15A	20A	5A	10A	15A	20A
25°C	240.8	372.6	504.6	620.6	330	572.4	795.2	1014.8
0°C	232	348	493	582	285.6	470	683.4	855
-10°C	215	347.2	448.2	520	280	441.6	615.6	742.6
-20°C	210	348	435	494	270	411.6	560	667.4
-30°C	216	329.4	426.6	342	240	393.6	520.2	624
-40°C	232.2	327.6	381.8	169.6	253.8	402.8	573.4	193.6

Table 7 – Instantaneous peak power for Rg=4.7 Ω

In order to have a better overview of the influence of the temperature, the gate resistance and the collector current values on the instantaneous peak power, some graphs have been made.

The first graphs are depicted in figures 37 (a) and (b). They illustrate the influence of the temperature on the instantaneous peak power losses during the transients for different collector current values. At first sight, it is possible to see that theses losses are lower for turn-on than for turn-off and they depends of course on the collector current level. However, it has been observed in some studies that depending on the test conditions, the turn-on losses of the Trench IGBT can be very high due to its high input capacitance inducing a longer collector current rise time [8]. For the turn-on since the MOSFET component is slightly independent of the temperature variation, this has

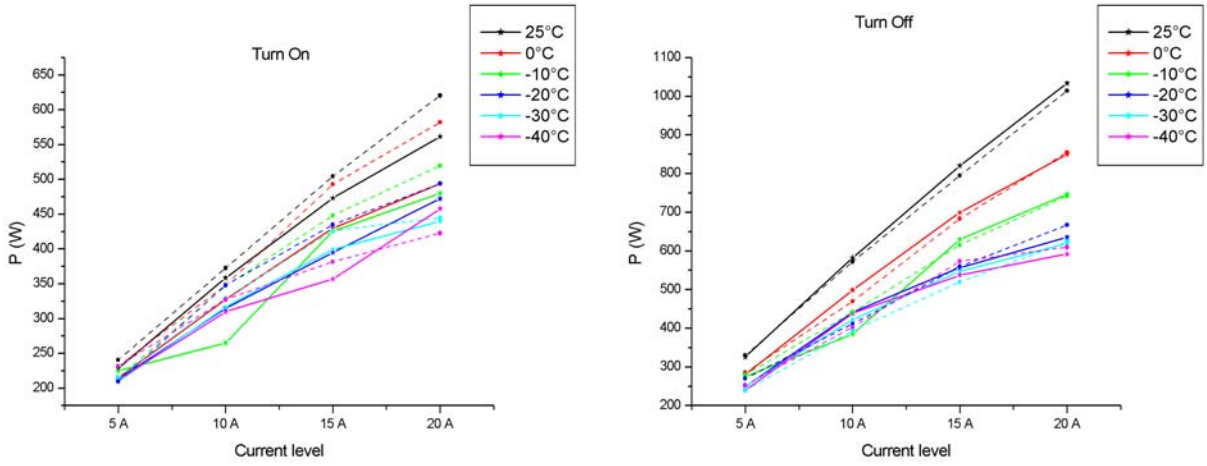
a low effect also on the power losses. As for the turn-off phase as the minority carrier concentration depends on the gain of the bipolar component which is strongly reduced, then the collector current tail is shorted and hence the instantaneous peak power is decreased. Furthermore, whatever the gate resistance value, the trends are the same: the losses are reduced when the temperature decreases. However, it is normal to observe that higher the gate resistance value, higher the instantaneous peak power losses.



(a) *(b)*

Figure 37 – Influence of the temperature on the instantaneous peak power losses (a) turn-on (b) turn-off
The dash lines correspond to Rg=4.7 Ω and the full line to Rg=2.2 Ω

The graphs depicted in figures 38 (a) and (b) show the influence of the collector current level on the instantaneous peak power losses during the transients for different temperature values. It is interesting to notice that the influence of the temperature is higher when the collector current value is high. Whereas during turn-on, this trend is not so obvious since the MOSFET component is not so affected by the temperature, when we consider the turn-off phase, there is a larger effect of the temperature for high current level. This phenomenon is mainly due to the self-heating which is more important within the device structure for a higher collector current inducing an increase of the gain of the bipolar component responsible for higher minority carrier concentration. This minority carrier concentration is responsible for the storage charge and the current tail.



(a) *(b)*

Figure 38 – Influence of the current load on the instantaneous peak power losses (a) turn-on (b) turn-off
The dash lines correspond to Rg=4.7 Ω and the full line to Rg=2.2 Ω

5.2.8 Observations

It is obvious to notice that the turn-on characteristics are disturbed by oscillations. A better care should be considering on the decoupling capacitor and on the module connections.

Furthermore, the experiments at -30°C and -40°C for a collector current equal to 20A were highly disturbed by the behavior of the decoupling capacitor. This can be directly observed on the current waveforms. The lowest temperature limit has been given for -40°C but it has to be highlighted that this value is not real.

6 2D Physically-Based Simulation Using ISE

6.1 *Equipment*

6.1.1 Computer

A personal computer (3Ghz) with a high RAM capacity (2Mo) has been bought in order to allow ISE to avoid swap on hard-disk and to increase to computation speed.

Both Windows and Linux have also been installed on the computer and the ISE software has been implemented on the Linux partition.

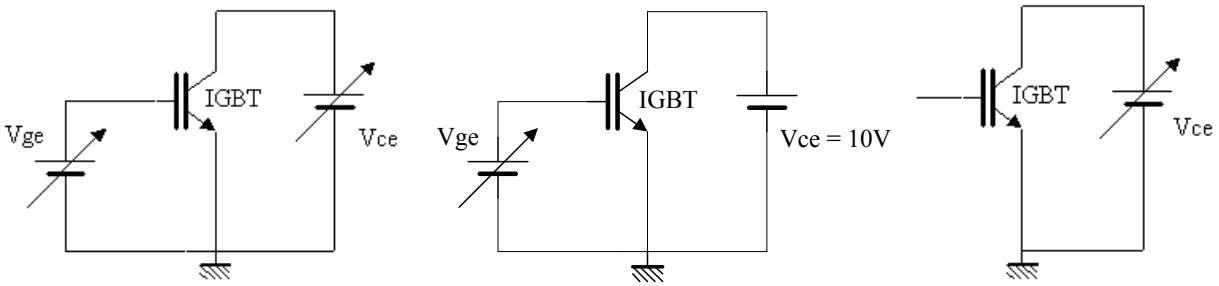
6.1.2 Software version

The installed version of ISE is the latest version: v9.0.12 for Dessis and V9.2 for Tecplot. We hoped that as a latest version this software was going to converge for any kind of simulations.

6.2 Static mode

6.2.1 Configuration

The basic test circuits used for the static simulations are depicted in figures 39 (a) to (c).



(a) Ic-Vce *(b) Ic-Vge* *(c) BVCEO*

Figure 39 - Basic test circuits for static simulations

6.2.2 Test conditions

The associated test conditions are summed up in tables 8 to 10.

Rg	Ic	Vce	Vg	T
-	-	Δ	[6V to 15V]	[+25°C to -40°C]

Table 8 – Test conditions for Ic-Vce

Rg	Ic	Vce	Vg	T
-	-	10V	Δ	[+25°C to -40°C]

Table 9 – Test conditions for Ic-Vge

Rg	Ic	Vce	Vg	T
-	-	Δ	-	[+25°C to -40°C]

Table 10 – Test conditions for BVCEO

6.2.3 Simulation file

The file used for the simulation is given hereafter. This file was provided by Toyota CRDL (in black) and some parts have been modified or added in this file (in red) according to the convenience of the authors. We assumed that this simulation file was in good agreement with the experimental data obtained with the power module CM150DY-24NF.

```
*****common specfication*****

#include "parameters.ini"

Plot {
       eCurrent/Vector hCurrent/Vector
       eDensity hDensity
       ElectricField/Vector
       eQuasiFermi hQuasiFermi
       eEparallel hEparallel
       Potential SpaceCharge
       temperature
       TotalHeat
       hlifetime elifetime
       SRH Auger eMobility hMobility
       Doping
       AvalancheGeneration
       hAvalanche eAvalanche
     }

#CurrentPlot {
      #temperature(  (1 0)   (1 4.5)  )
      #AvalancheGeneration( Maximum(Semiconductor Material="Silicon") )
      #hCurrentDensity( Maximum(Semiconductor Material="Silicon")  )
      #hJouleHeat( Maximum(Semiconductor Material="Silicon") )
            #}
```

Determination of Vth

```
***** Vth (Vd=10V) *****

#if @<"@condition@" == "Vth">@

Physics {
```

```
     *****AreaFactor for 1cm2*****
      temperature=@temp@
          AreaFactor = @AF@
          Mobility ( DopingDependence
                     HighFieldSaturation
                     NormalElectricField
                     CarrierCarrierScattering (BrooksHerring)
                   )
          EffectiveIntrinsicDensity( oldSlotboom )
          Recombination (
                          SRH(DopingDependence Exptempdep)
                          Auger
                          Avalanche(Lackner)
                        )
        }
Math {
  Newdiscretization
       extrapolate
       Avalderivatives
       derivatives
       digits=7
       iterations=25
       RelErrControl
       ErrRef(electron)=1e10
       ErrRef(hole)=1e10  BreakCriteria{ Current( Contact="collector"maxval=0.1)
}
     }

File {
        grid      = "@grid@"
        doping    = "@doping@"
        current   = "@plot@"
        output    = "@log@"
        plot      = "@dat@"
        lifetime  = "@doping@"
        parameter = "tau_Nref.par"
        save      = "n@node@_Vth"
    }


Electrode {
            { name= emitter   voltage=0 }
            { name= collector voltage=0  }
            { name= gate      voltage=0 barrier=0.2 }
          }

Solve {

  ##NewCurrentFile=tmp_

  *****initial*****
       poisson
       coupled { poisson electron hole}


  *****VCE ramping *****
       Quasistationary (
                         InitialStep=1e-3 MaxStep=0.01 MinStep=1e-6
                         increment=1.5
                         Goal {name=collector value=10}
                       )
```

We have preferred obtaining the entire curve, then, we removed the *BreakCriteria.*

```
        { coupled { poisson electron hole } }

*****gate upto 15V*****

        Quasistationary (
                          InitialStep=1e-2 MaxStep=0.1 MinStep=1e-6
                          Goal {name=gate value=15})
        { coupled { poisson electron hole }}
```

We have increased a little bit the precision :

```
  Quasistationary (
       InitialStep=1e-4 MaxStep=0.1 MinStep=1e-8
       Goal { Voltage=15 Name="gate" } )
```

```
  ###Save (FilePrefix="n@node@_Vth")

  ##NewCurrentFile="" }
```

Determination of Ic=f(Vce) curves for various Vge

```
***** Vce_Ic (Vge=15V) *****

#elif @<"@condition@" == "VceIc">@

Physics {
     *****AreaFactor for 1cm2*****
          AreaFactor = @AF@
      temperature=@temp@
          Mobility ( DopingDependence
                     HighFieldSaturation
                     NormalElectricField
                     CarrierCarrierScattering (BrooksHerring)
                   )
          EffectiveIntrinsicDensity( oldSlotboom )
          Recombination (
                         SRH(DopingDependence Exptempdep)
                         Auger
                         Avalanche(Lackner)
                        )
        }

Math {
  Newdiscretization
       extrapolate
       Avalderivatives
       derivatives
       digits=7
       iterations=25
       RelErrControl
       ErrRef(electron)=1e10
       ErrRef(hole)=1e10
      BreakCriteria{ Current( Contact="collector"maxval=200) }
     }


File {
        grid      = "@grid@"
```

We have preferred obtaining the entire curve, then, we removed the *BreakCriteria.*

```
        doping    = "@doping@"
        current   = "@plot@"
        output    = "@log@"
        plot      = "@dat@"
        lifetime  = "@doping@"
        parameter = "tau_Nref.par"
        save      = "n@node@_VceIc"
    }


Electrode {
            { name= emitter   voltage=0 }
            { name= collector voltage=0  resist=3e5}
            { name= gate      voltage=0 barrier=0.2 }
          }

Solve {

  ##NewCurrentFile=tmp_

  *****initial*****
        poisson
        coupled { poisson electron hole}

  *****gate upto 15V*****
        Quasistationary (
                          InitialStep=1e-2 MaxStep=0.1 MinStep=1e-6
                          Goal {name=gate value=15})
        { coupled { poisson electron hole }}

  ##Save (FilePrefix="n@node@_statvg15V")

  ##NewCurrentFile=""

  *****VCE ramping *****
        Quasistationary (
                          InitialStep=1e-3 MaxStep=0.05 MinStep=1e-6
                          increment=1.5
                          Goal {name=collector value=30}
                        )
        { coupled { poisson electron hole } }
      }
```

We have investigated the influence of Vge :

Value=@VGE@

Determination of the IGBT breakdown voltage BVCEO

```
Thermode {
            { name= "collector"    temperature=@temp@
      }
            { name= "emitter" temperature=@temp@
      }
 }

 #CurrentPlot {
             #temperature(  (1 0)   (1 4.5)  )
      #AvalancheGeneration( Maximum(Semiconductor Material="Silicon") )
      #hCurrentDensity( Maximum(Semiconductor Material="Silicon")  )
      #hJouleHeat( Maximum(Semiconductor Material="Silicon") )
            #}

Physics {
     *****AreaFactor for 1cm2*****
```

```
          AreaFactor = @AF@
          Mobility ( DopingDependence
                     HighFieldSaturation
                     NormalElectricField
                     CarrierCarrierScattering (BrooksHerring)
                   )
          EffectiveIntrinsicDensity( oldSlotboom )
          Recombination (
                          SRH(DopingDependence Exptempdep)
                          Auger
                          Avalanche(Lackner)
                        )
                          AnalTep
                    Thermodynamic
         }

Math {
  Newdiscretization
       extrapolate
       Avalderivatives
       derivatives
       digits=7
       iterations=25
       RelErrControl
       ErrRef(electron)=1e10
       ErrRef(hole)=1e10
     }

File {
        grid      = "@grid@"
        doping    = "@doping@"
        current   = "@plot@"
        output    = "@log@"
        plot      = "@dat@"
        lifetime  = "@doping@"
        parameter = "tau_Nref.par"
        save      = "n@node@_VceIc"
    }

Electrode {
            { name= emitter   voltage=0 }
            { name= collector voltage=0  resist=3e5}
            { name= gate      voltage=0 barrier=0.2 }
          }

 Thermode {
            { name= "collector"    temperature=@temp@
      }
            { name= "emitter" temperature=@temp@
      }
 }

Solve {

  ##NewCurrentFile=tmp_

  *****initial*****
       coupled { poisson }
       coupled { poisson electron hole }
       coupled { poisson electron hole temperature }
```

```
##Save (FilePrefix="n@node@_statvg15V")

##NewCurrentFile=""

*****VCE ramping *****
      Quasistationary (
                        InitialStep=1e-3 MaxStep=0.05 MinStep=1e-9
                        increment=1.5
                        Goal {name=collector value=1500}
                      )
      { coupled { poisson electron hole temperature} }
    }
```

6.2.4 Simulation results

6.2.4.1 Analysis

The internal dynamics of the Trench IGBT were analyzed along the cut-line xx' of the 2D structure as depicted in figure 40. This cut-line runs from the emitter electrode (y=0µm) to the collector electrode (y=370µm)

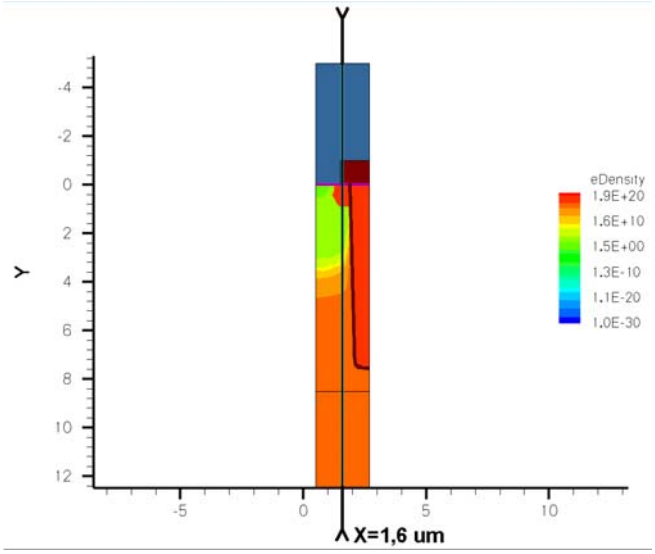


Figure 40 - xx' cutline for 1D analysis (zoom on the upper part of the device)

The results are presented as 1D curve showing some typical internal parameters such as concentrations, electric field, impact carrier generation …. The simulation results correspond to the last computed point.

6.2.4.2 Ic-Vce characteristics

The simulation results are depicted in figure 41 (a) and (b). No limit has been added in the simulation file and therefore we obtained to full curve with the *AREA FACTOR* provided with the simulation file.

These curves have been obtained with a gate-emitter voltage equal to 9.55V. For this gate level, it is

obvious to notice that when the temperature decreases the saturation current level is reduced. For low doping levels, the carrier mobility in silicon increases with the reduction of the temperature which induces an increase of the saturation current level. However, for the given current level the saturation current is reduced. Then it is possible to say that the electron current from the MOS component is not a dominant factor. The decrease of the electron current from the MOS component is higher than the decrease of the current gain of the bipolar part of the Trench IGBT. Furthermore, we may also consider that the gate voltage value is not so high compare to the threshold voltage value and this will have an effect on the device behavior [5].

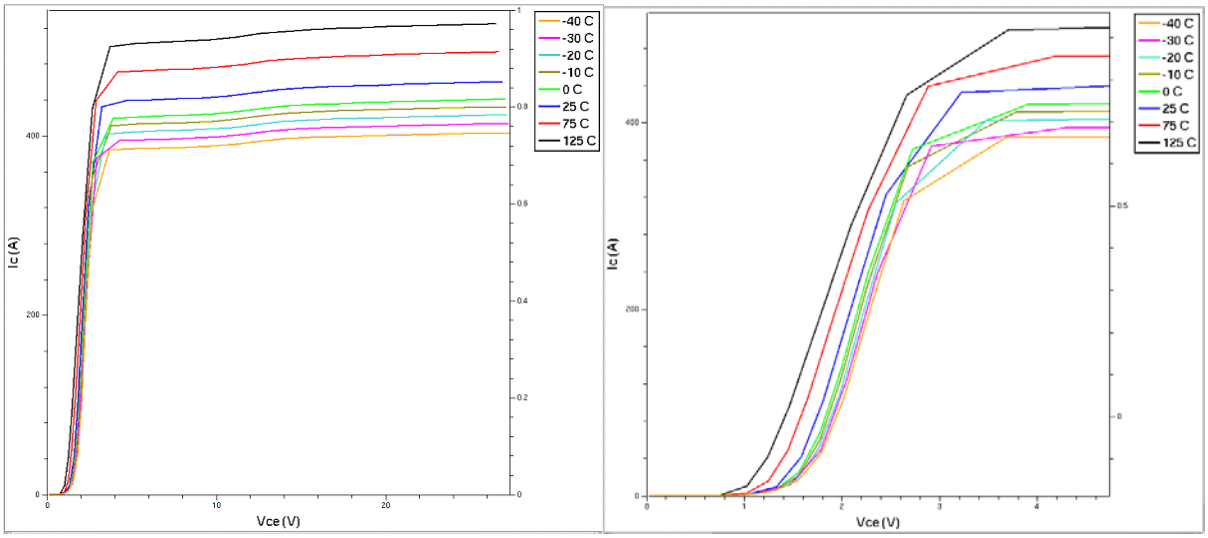
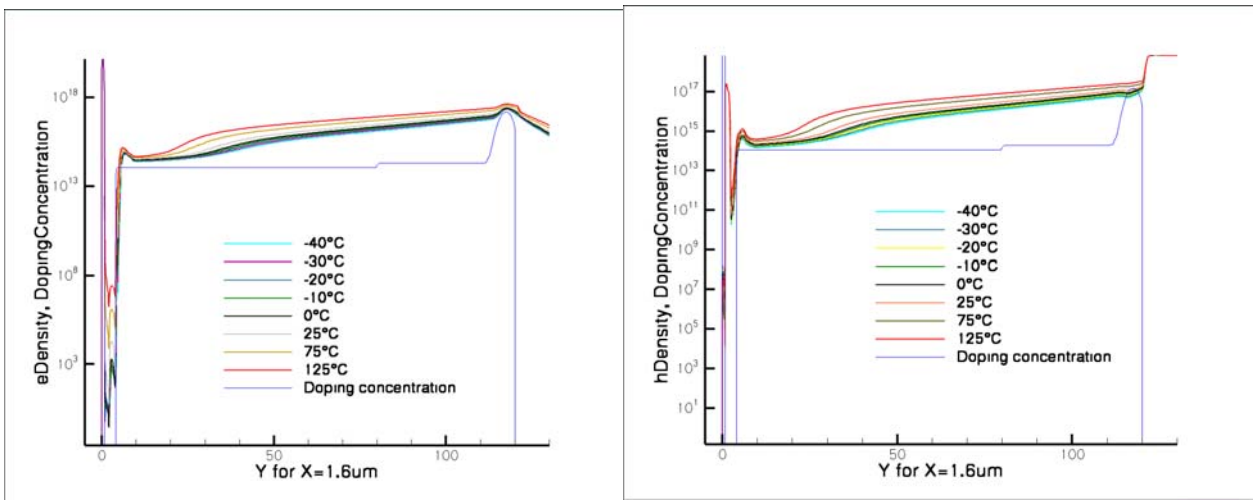


Figure 41 - (a) Ic-Vce curve (b) zoom for low Vce values

Also it can be observed that for the given current value, it increases the on-state voltage drop because of the reduction of the current gain of the bipolar part of the IGBT, lowering the minority carrier injection. As a consequence, the conductivity modulation is less effective leading to an increase of the on-state power losses.

Figures 42 (a) and (b) illustrate the electrons and holes concentration within the structure at the end of the simulation (Vce=30V and Ic=400A). Even if the IGBT is not used in such kind of configuration, since the device is only used as a switch, it is possible to observe the high level injection in the drift region (free carriers concentration above the doping concentration). In both cases, the electrons and holes concentrations decrease when the temperature is reduced. Also it is possible to observe that only for high temperatures the concentration becomes high, and for the other temperature values the concentrations are quiet the same.

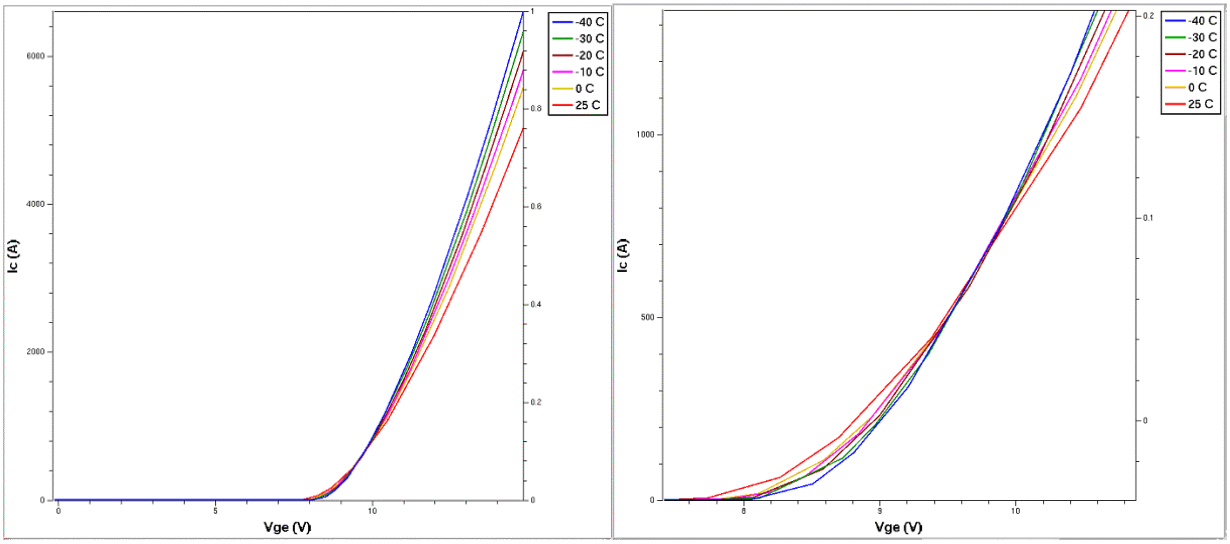


(a) *(b)*

Figure 42 - (a) Electrons concentration (b) holes concentration

6.2.4.3 Ic-Vge characteristics

The transfer characteristics are shown in figures 43 (a) and (b). For these simulations too, we have chosen to take the whole simulation by removing the break criterion. The collector-emitter voltage has been set up to 10V.



(a) *(b)*

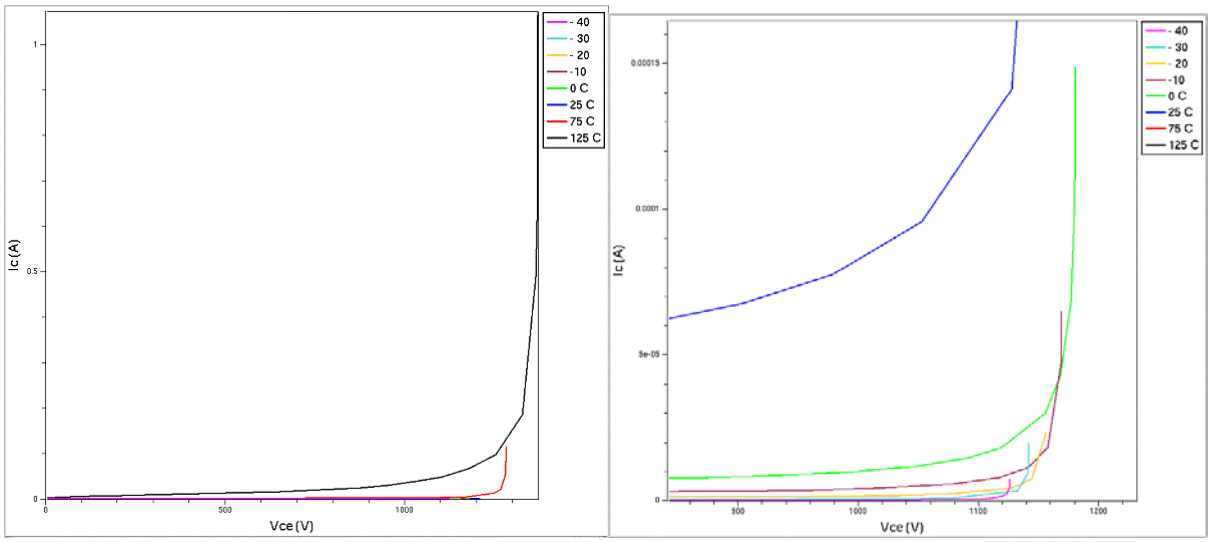
Figure 43 - (a) Ic-Vge curves (b) zoom for low Vge values

It can be noticed that under a certain level of current the temperature coefficient is negative but above this level it becomes positive. By considering the figure 43(b), we observe that the temperature reduction induces an increase of the threshold voltage. This is directly linked to the threshold voltage expression as reminded in [7]. However this variation is not so important.

Note that for this static operation we do not present internal dynamics.

6.2.4.4 Breakdown voltage BVCEO characteristics

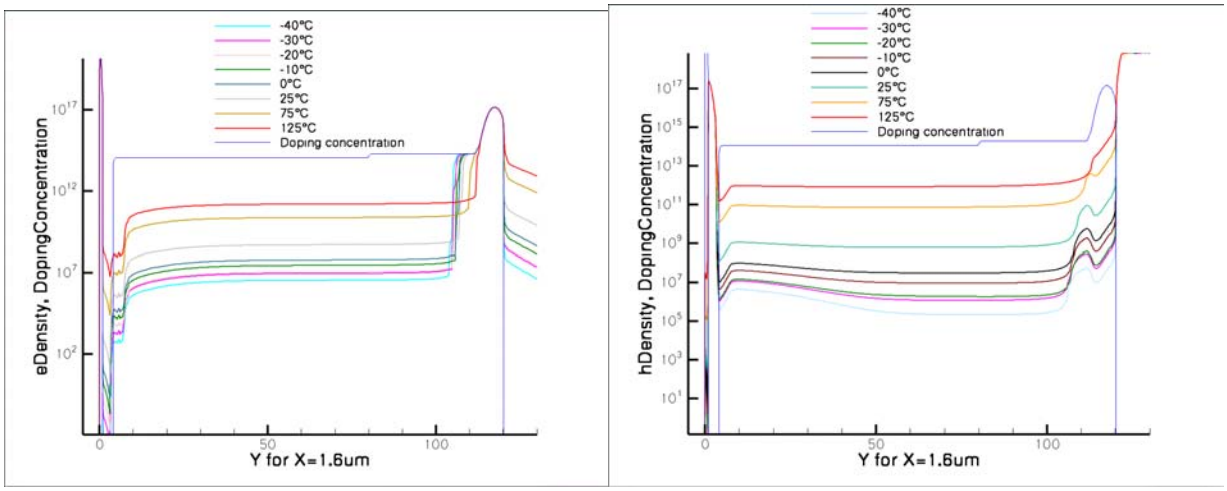
In power electronics applications, since the device is mainly used as a switch, the device behavior during the off-state depends mainly on the breakdown voltage characteristic. In figures 44 (a) and (b), it is possible to observe the variation of the breakdown voltage for a temperature varying from -40°C to +125°C. It is obvious to notice that the leakage current rises when the temperature increases. Furthermore, the reduction of the temperature is responsible for the decrease of the static breakdown voltage which is equal to 1400V at +125°C and to 1125V at -40°C.



(a) *(b)*

Figure 44 - (a) BVCEO curves (b) zoom for very low leakage currents

The analysis of the device structure illustrated by figures 45 (a) and (b) allows to say that the drift region is under low level injection since the carriers concentration is lower than the doping concentration level.



(a) *(b)*

Figure 45 - (a) Electrons and (b) holes concentrations

This configuration is normal since the ending point of the simulation is represented by a high voltage value and a very low current level. The temperature reduction has a decreasing effect on the carriers concentration.

Under high voltage, the device structure is submitted to high electric field as depicted in figure 46. The temperature variation does not influence so much the electric field distribution. The maximum electric field is reduced with the temperature reduction. Furthermore, lower the temperature more this influence is reduced. Associated to the electric field distribution, figure 47 illustrates the space charge extension in the whole device. Its change is directly linked to the electric field distribution variation.

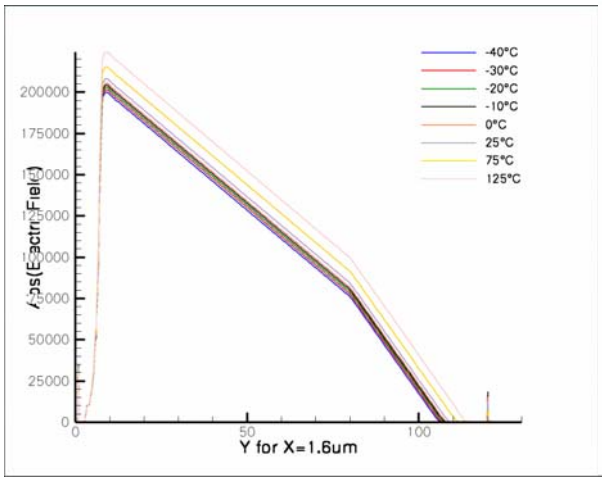


Figure 46 - Electric field

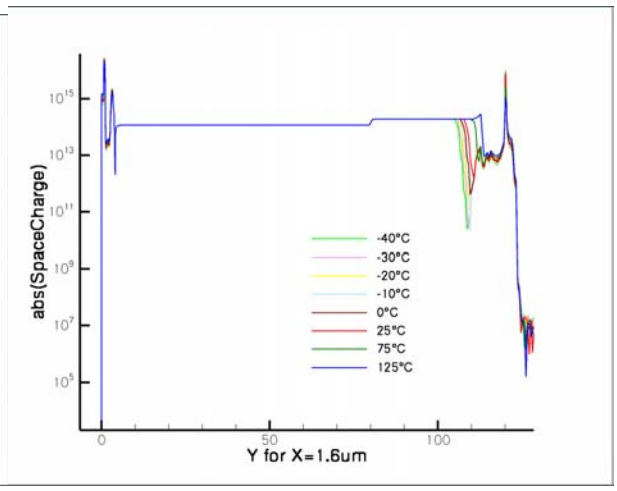


Figure 47 - Space charge within the device

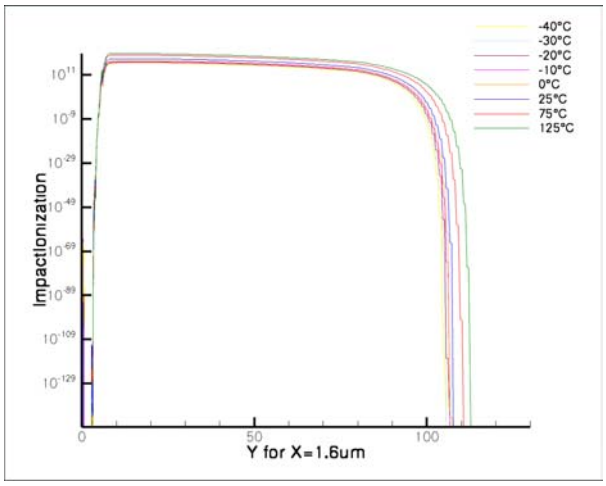


Figure 48 - Carriers generation by impact

The carriers generation by impact which is an important phenomenon during the blocking phase is shown in figure 48. The temperature variation has no significant effect on this carrier generation, which is slightly reduced when the temperature decreases.

6.2.5 General discussion

When the junction temperature of the device is decreased, the static behavior of the Trench IGBT is influenced and the external current and voltage waveforms are modified. The effect of the low temperature has the same effect as the high temperature but in the opposite way. There is no significant or special phenomenon which can bring a specific behavior of the device. The very low temperature values were not studied in this first approach according to the project requests.

6.2.6 Simulations troubles

During the static operating mode simulation, no trouble was found. The convergence was effective for all static characteristics as well as for all temperature values.

6.3 *Switching mode with resistive load*

6.3.1 Configuration

The investigation of the switching under resistive load was based on the test circuit shown in figure 49.

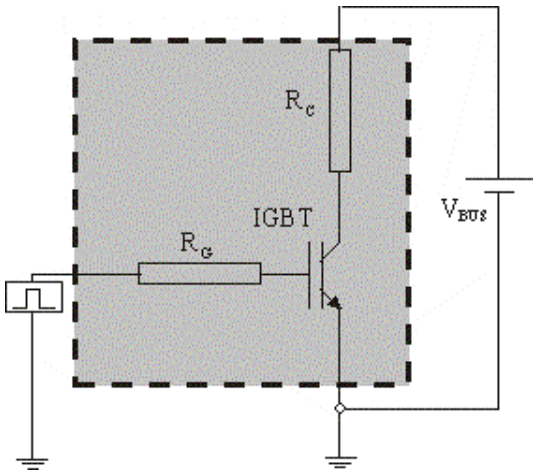


Figure 49 - Resistive load switching test circuit (in grey the 2D IGBT structure)

The gate was pulsed at the value of 15V. The resistive load is attached directly the collector contact of the IGBT structure. The value of the resistance is depending on the *AREA FACTOR* and the voltage value used for the DC bus. The gate resistance is also attached to the resistive contact of the gate. Its value depends on the *AREA FACTOR* and also is linked to a potential barrier.

No mixed simulation was used for this part.

Note: for this switching configuration the internal dynamics analysis was not done since the load for this project is inductive.

6.3.2 Test conditions

The test conditions are the same as for the static simulation in 5.2.2. The thermal effects are taken into account with *THERMODE* element. The details are given in 6.4.3.

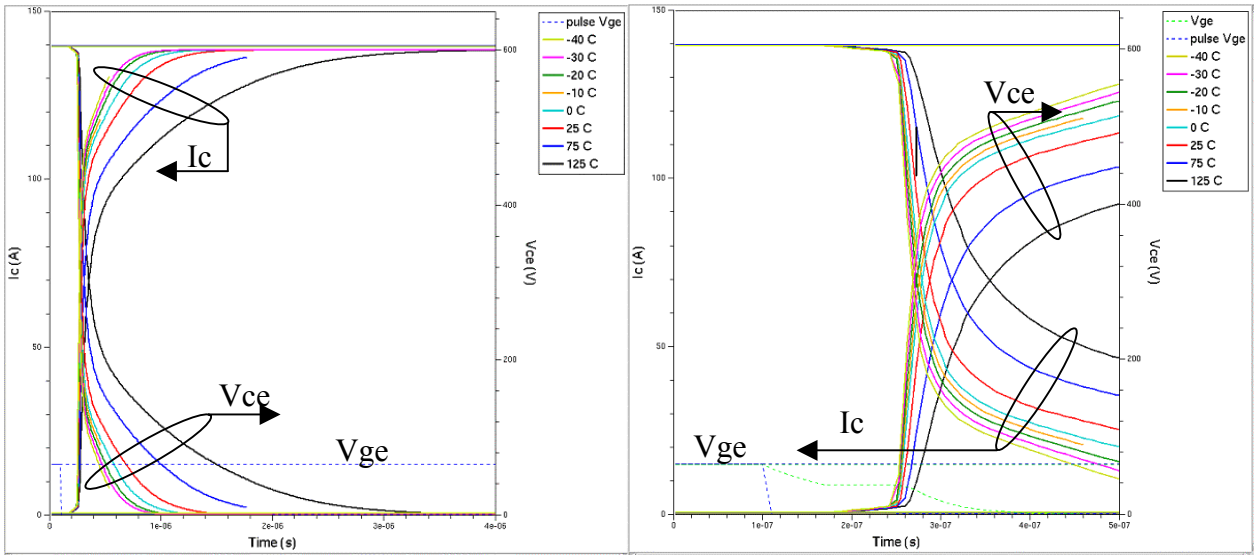
6.3.3 Simulation file

```
****** R_stat300V preparation for turn_off*****
#elif @<"@condition@" == "IcRload">@

Physics {
     *****AreaFactor for 1cm2*****
          AreaFactor = @AF@
      temperature=@temp@
          Mobility ( DopingDependence
                     HighFieldSaturation
                     NormalElectricField
                     CarrierCarrierScattering (BrooksHerring)
                   )
          EffectiveIntrinsicDensity(oldSlotboom)
          Recombination (
                          SRH(DopingDependence Exptempdep)
                          Auger
                          Avalanche(Lackner)
                        )
         }

Math {
  Newdiscretization
       extrapolate
       Avalderivatives
       derivatives
       digits=7
       iterations=25
       RelErrControl
       ErrRef(electron)=1e10
       ErrRef(hole)=1e10
       NoCheckTransientError
       transient=BE
           }

File {
        grid      = "@grid@"
        doping    = "@doping@"
        current   = "@plot@"
        output    = "@log@"
        plot      = "@dat@"
        lifetime  = "@doping@"
        parameter = "tau_Nref.par"
       save      = "n@node@_R_SW"
     }

Electrode {
            { name= emitter   voltage=0 }
            { name= collector voltage=0 Resist=@<AF*VDD/140>@}
            { name= gate      voltage=0
                              voltage= (15 at 0, 15 at 1e-7, 0 at 1.1e-7)
```

```
            Resist=@<AF*1>@ barrier=0.2 }
        }
Solve {
  ##NewCurrentFile=tmp_
       poisson
       coupled { poisson electron hole}
       Quasistationary (
                         InitialStep=1e-2 MaxStep=0.1 MinStep=1e-6
                         Goal {name=gate value=15}
                       )
       { coupled { poisson electron hole } }
       Quasistationary (
                         InitialStep=0.005 MaxStep=0.1 MinStep=1e-6
                         Goal {name=collector value=@VDD@}
                       )
       { coupled { poisson electron hole } }

  ##Save (FilePrefix="n@node@_R_stat@VDD@V")
  ##NewCurrentFile=""

       Transient ( InitialStep=1.0e-9 MaxStep=1e-8 MinStep=1e-12
                   InitialTime=0 FinalTime=5e-6
                   Increment=1.5 Decrement=2.0
                 )
       {
         coupled (digits=7 iterations=25){ poisson electron hole }
       Plot (FilePrefix="n@node@" time=(4e-7;6.1e-7;7.25e-7;1.08e-6;2e-6)
NoOverwrite)
       }

##  System("rm tmp_n@node@_des.plt")
```

6.3.4 *Simulations results*

The collector current, the gate-emitter and the collector-emitter voltages of the Trench IGBT for resistive load switching is presented in figures 50 (a) and (b).



(a) *(b)*

Figure 50 - Current and voltage waveforms under resistive load for (a) turn-on and (b) turn-off

Whereas the temperature variation has a strong influence for high value (+75°C and +125°C), this effect is not so important when the temperature is reduced.

The turn-on transient under low temperature does not exhibit a specific behavior and the device waveforms are slightly modified. The turn-on transient of IGBT is directly linked to the MOSFET component which behavior is not so much influenced by the temperature variation. However we must noticed that for high temperature this influence is more emphasized.

The turn-off phase of IGBT usually presents a current tail which depends strongly on the temperature. For the low temperature values (from 0°C down to -40°C), it is possible to observe that the tail is reduced when the temperature decreases. The minority carrier responsible for the storage charge in the drift region is reduced since the gain of the bipolar component is also reduced when the temperature is lowered.

6.3.5 General discussion

When the junction temperature of the device is decreased, the switching behavior under resistive load of the Trench IGBT is influenced and the external current and voltage waveforms are slightly modified. The effect of the low temperature has a reduced effect contrarily to the high temperature.

However, there is no significant or special phenomenon which can bring a specific behavior of the device.

6.3.6 Simulations troubles

No specific troubles were encountered during these simulations under resistive load. The convergence was instantaneous for each simulation and the lowest temperature value was -40°C, as requested.

6.4 *Switching mode with inductive load*

6.4.1 Configuration

The typical test circuit for inductive load test is depicted in figure 51. This circuit allows to investigate only the turn-off of the IGBT. Note that for the turn-on, the current shape allows eventually to investigate a zero current turn-on. But this configuration was not requested for the present project.

The use of a freewheeling diode allows to keep a continuing current flow once the IGBT has been

turned off. The use of a mixed simulation permits to use external component such as resistance, inductance and diode. The gate pulse was set up to fix the maximum collector current peak value. Some parasitic elements not plotted in figure 51 have also been added as it can be seen in the text program.

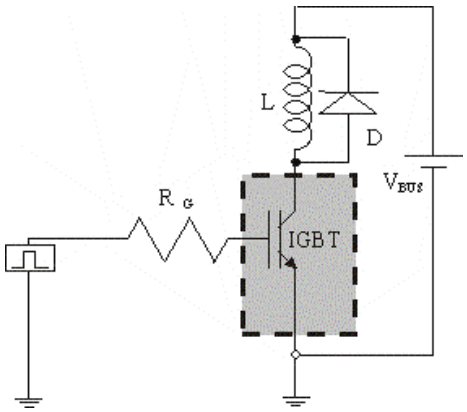


Figure 51 - Inductive load single gate pulse switching test circuit (in grey the 2D IGBT structure)

6.4.2 Test conditions

The test conditions are the same as for the static simulation in 6.2.2.

6.4.3 Simulation file

The basic simulation file was provided by Toyota CRDL. According to the troubles we got, we modified this file. As for the electrothermal simulation, a discussion regarding the use of *THERMODE* is proposed just after.

```
*************Clamped inductive load simulation*********************

#elif @<"@condition@" == "Avalanche">@

#if @init_avalanche@ == 0

Physics {
        *  AreaFactor normalizes to an area of 1 cm^2
      temperature=@temp@
      AreaFactor = @AF@
      Mobility ( DopingDependence
                  HighFieldSaturation
                  NormalElectricField
                  CarrierCarrierScattering (BrooksHerring)
                )
        EffectiveIntrinsicDensity( Slotboom )
        Recombination (
                  SRH(DopingDep ExpTempdep)
                  Auger
                  Avalanche (Lackner Eparallel)
                  )
#     AnalTep
#     Thermodynamic
        }
```

```
Math {
        RelErrcontrol
        Digits=5
        Iterations=8
        Derivatives
        AvalDerivatives
        #NoAutomaticCircuitContact
      NewDiscretization
      DirectCurrentComp
      #method=pardiso
      extrapolate
     }

File {
        grid      = "@grid@"
        doping    = "@doping@"
        current   = "@plot@"
        output    = "@log@"
        plot      = "@dat@"
        lifetime  = "@doping@"
        parameter = "tau_Nref.par"
        save      = "n@node|-1@_L_stat@VDD@V"
     }

Electrode {
            { name= emitter   voltage=0 }
            { name= collector voltage=0 }
            { name= gate      voltage=0 }
          }

Solve {

        * Inital Solution
        poisson
        coupled { poisson electron hole}

        * Quasistat the collector to @VDD@ Volt
        Quasistationary (
                InitialStep=1e-5 MaxStep=0.5 MinStep=1e-12
                Increment=2 Decrement=3
                Goal {name=collector value=@VDD@}
                )
        { coupled { poisson electron hole } }
      }

#else

****** gate on time @tav@ usec*****

***** Define thermal electrode *****
Thermode {
         { name= "top" temperature=300  SurfaceResistance=30}
         #{ name= "bottom" temperature=300  SurfaceResistance=0.3}
        }

Physics {
        ***AreaFactor normalizes to an area of 1 cm^2
        temperature=@temp@
        AreaFactor = @AF@
       Mobility ( DopingDependence
```

```
                    HighFieldSaturation
                    NormalElectricField
                    CarrierCarrierScattering (BrooksHerring)
                  )

        EffectiveIntrinsicDensity(Slotboom)
        Recombination (
                  SRH(DopingDep ExpTempdep)
                  Auger
                  Avalanche (Lackner Eparallel)
                  )
      AnalTep
      Thermodynamic
        }

Math {
        RelErrcontrol
        Digits=5
      Iterations=100
        Derivatives
        AvalDerivatives
        NoAutomaticCircuitContact
        NewDiscretization
      DirectCurrentComp
      NoCheckTransientError
        #transient=BE
      extrapolate
      NotDamped=100
    ##BreakCriteria{ LatticeTemperature( maxval=900) }
        -MetalConductivity
     }
************************************************************
* L_load Avalanche simulation
* Transient turn-off under inductive load.
************************************************************
File    {
       output  = "@log@"
}

Dessis igbt{
  Electrode {
        { name= collector   voltage=@VDD@ }
        { name= emitter voltage=  0 }
        { name= gate    voltage=  0 } #barrier=0.2 }
  }

  File {
        grid    = "@grid@"
        doping  = "@doping@"
        lifetime = "@doping@"
        parameter = "tau_Nref.par"
  }
}

System        {
       igbt ig1(collector=node1 gate=node2 emitter=0){
              File {
                    plot    = "@dat@"
                    current = "@plot@"

****** L_load_Avalanche simulation*****
```

```
                    load    = "n@node|-1@_L_stat@VDD@V_des"
                }
        }
         r r1     (node1 node3)    {r=0.01}
         l l1     (node3 node4)    {l0=100e-6}          * 100uH
         r r2     (node4 node5)    {r=0.01}             * 10 mOhm
         v v1     (node5 0)        {type="dc" dc=@VDD@} * Battery
         r r3     (node2 node6)    {r=5}                * 5.0 Ohm

###         v v2     (node6 0) {type="pwl" pwlfile="ava80u.pwl"}

*** its also possible to do like this
**          v v2     (node6 0) {type="pwl" pwlfile="ava@tav@u.pwl"}
            Vsource_pset v2 (node6 0) { pwl = (
                                        0.e0   0
                                        10e-9   0
                                        30e-9  15
                                        @<tav+0.03>@e-6    15
                                        @<tav+0.05>@e-6    0
                                        @<tav*1.6>@e-6 0
                                      )
                            }

         plot "n@node@_circ.plt" (
              time() node1 node2 node3 node4 node5 node6 node7 node8 i(l1 node3)
i(r3 node2)
         )
        initialize (node1=@VDD@ node2=0)
}

Solve {
         coupled (iterations=50 digits=5) {poisson}
         coupled(iterations=50 digits=5)  { hole electron poisson }
         coupled(iterations=50 digits=5)  { poisson contact circuit temperature}
         #coupled(iterations=100 digits=5)  { hole electron poisson contact
circuit}
         #coupled(iterations=100 digits=5)  { hole electron poisson contact
circuit temperature}

         Transient ( InitialStep=10e-9 MaxStep=1e-6
                   Minstep=1e-30
                     InitialTime=0 Finaltime=@<tav*1.6>@e-6
                     #Increment=1.5 Decrement=2.0
                   increment=1.3 decrement=2
                    )
         {
         coupled(iterations=50 digits=5)  { hole electron poisson contact circuit
temperature}
Plot (FilePrefix="n@node@" time=(Range=(@tav@e-6 @<tav+30>@e-6) Intervals=30)

#Plot (FilePrefix="n@node@" time=(40.7e-6;40.8e-6)

 NoOverwrite)

         }
}

#endif   !!! Avalanche

#endif
*****************************************************
```

We have fixed directly a *Finaltime= 2^{e}-5*

We have fixed the time plots:

```
Plot   (FilePrefix="n@node@"   time=(1.1e-8;5e-
6;1.0156e-5;1.1e-5) NoOverwrite)
```

6.4.4 *Taking into account thermal effect in physical simulations*

When considering thermal effect in simulations, it is important to see what kind of real operation the simulation will evaluate. If the operating mode does not induce self heating within the device structure, then the thermodynamic option is not needed. In opposite, if the self heating has a great impact on the device behavior the thermodynamic option has to be used.

Depending on the collector current level running through the device, the self heating generated is important or not. The use of thermodynamic induces higher computing time consumption and gives the same result as in the case of isothermal simulations. The table 11 illustrates the different simulation configuration which has been tested for this project.

Thermodynamic simulation with :	**Fixed temperature** ***Temperature=@temp@***	**Converge domain**
Coupled solve		
2 thermodes (Collector, emitter)	Yes	[-10°C ; 25°C]
1 thermode (Collector)	Yes	[-10°C ; 25°C]
1 thermode (Collector)	No	Only 25°C
No thermodynamic simulation	Yes	[-10°C ; 125°C]

Table 11 – Consideration of the thermal effect for simulation

The mathematic and electron command *COUPLED* has been used to insure a coupled equation resolution between the holes continuity equation, the Poisson equation. If the *COUPLED* command is not use, the simulation can provide a result only for 25°C.

The thermal contacts referenced as *THERMODE* in ISE are necessary in case of non isothermal simulation. It can be noticed that one or two thermal contacts can be used. The most realistic configuration is the use of one thermal contact on the collector side which normally is linked to the base plate of the power module and which is fixed to a specific temperature. This simulation can induce very complicated computation since the emitter contact is thermally “free”.

In any case, it can be seen that simulation can be done for various temperatures but these temperature values can not go under -10°C. This will be discussed in the paragraph 6.4.6.

6.4.5 *Simulations results*

The use of a single gate pulse allows to obtain the simulation waveforms depicted in figure 52. The times in red indicate the instants which can be used to analyze the device dynamics by considering

the internal device structure. The 15V gate pulse length has been determined to set up the maximum load current to 50A. The collector emitter voltage was set up to 300V.

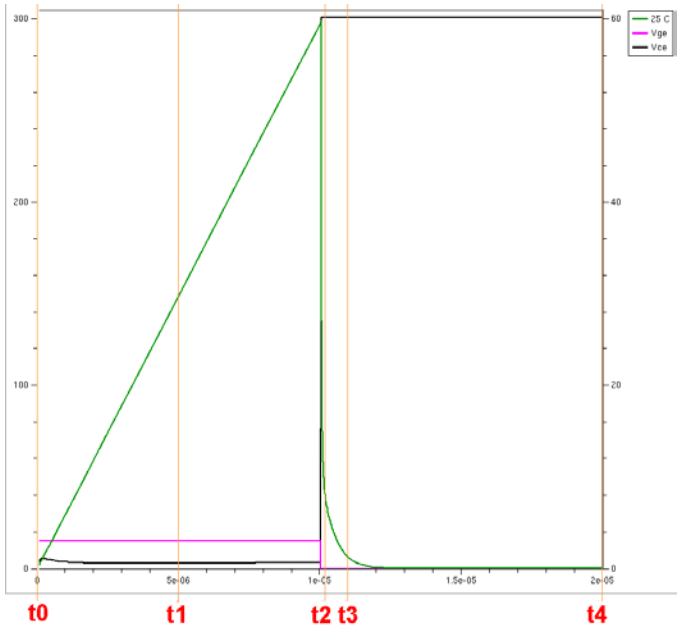


Figure 52 - Inductive load single gate pulse switching test circuit (in grey the 2D IGBT structure)

During the pulse gate duration (from t0 to t2) which determines the maximum current in the load and also in the device, the current runs linearly through the device. This shape is imposed by the inductor as indicated by the following basic equation:

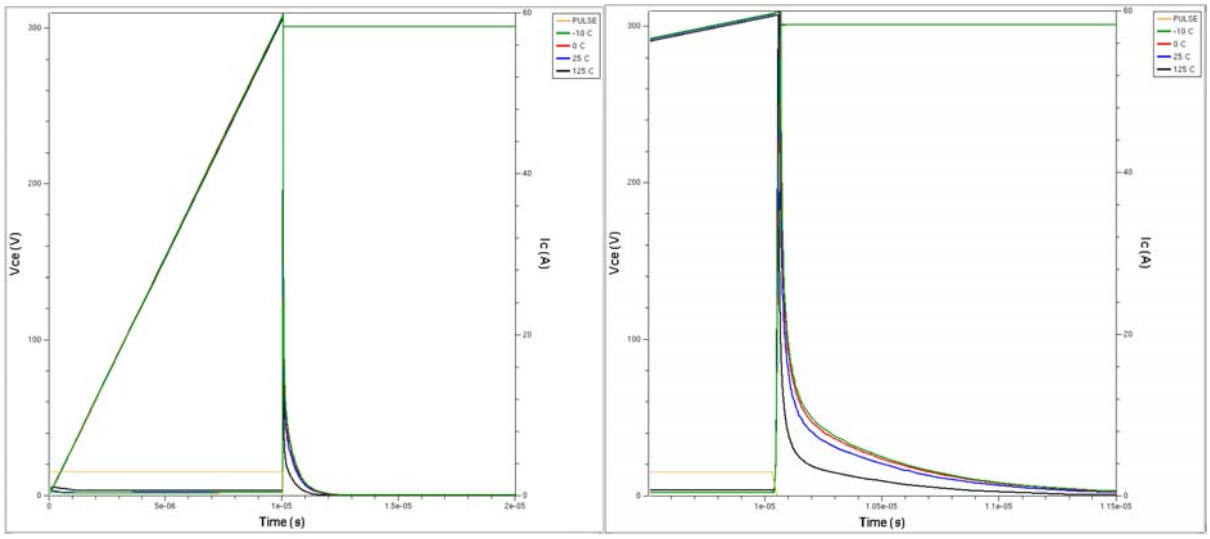
$$I(t) = (E/L) * t$$

When the device is turned off, the current stops running through the IGBT and continues flowing through the freewheeling diode. Just after time t2, the current in the device is strongly reduced since the gate pulse is also decreased to zero, and the collector emitter voltage reaches the voltage bus due to the clamping effect from the diode. The IGBT exhibits a current tail (at t3) until the minority carriers are removed by recombination from the drift region (at t4).

Table 12 illustrates the characteristics at different instants. In the last column, the collector current value is given as well as the value of the simulation temperature. It can be noticed that the current variation is very strange since when the temperature decreases the current tail is longer and the minority carriers stored in the drift region is higher at high temperature than at low temperature. This is also clearly illustrated in figure 53(b). These simulations have been made many times to check if the same results were found. We could see the validation of the present results. We did not find the reason why the results are in opposite to the real behavior of the device.

	Vce (V)	Ic (A)
t0	300	~ 0
t1	~ 2	29.6
t2	300	T = -10°C / Ic = 11.6
		T = 0°C / Ic = 11
		T = 25°C / Ic = 9.5
		T = 125°C / Ic = 4.5
t3	300	T = -10°C / Ic = 1.6
		T = 0°C / Ic = 1.5
		T = 25°C / Ic = 1.2
		T = 125°C / Ic = 0.47
t4	300	~0

Table 12 – Internal dynamics analysis simulation instants



(a) *(b)*

Figure 53 - "Strange" turn-off at various temperature (a) full waveforms (b) zoom on turn-off

6.4.6 Discussion - Troubles

The behavior of the device seems to be strange since we do not have the expected waveforms for the collector current according to the temperature. It behaves in the opposite way. The current tail is reduced when the temperature is increased. We did the internal dynamics analysis but as for the external current and voltage waveforms, we found that the electrons and holes concentrations, the electric field distribution and so on were very unusual. For instance in figure 54, it is possible to see that hole concentration in the drift region for +125°C is lower than for the other temperature, whereas the gain of the bipolar component should be increased when the temperature rises inducing an increase of the holes concentration.

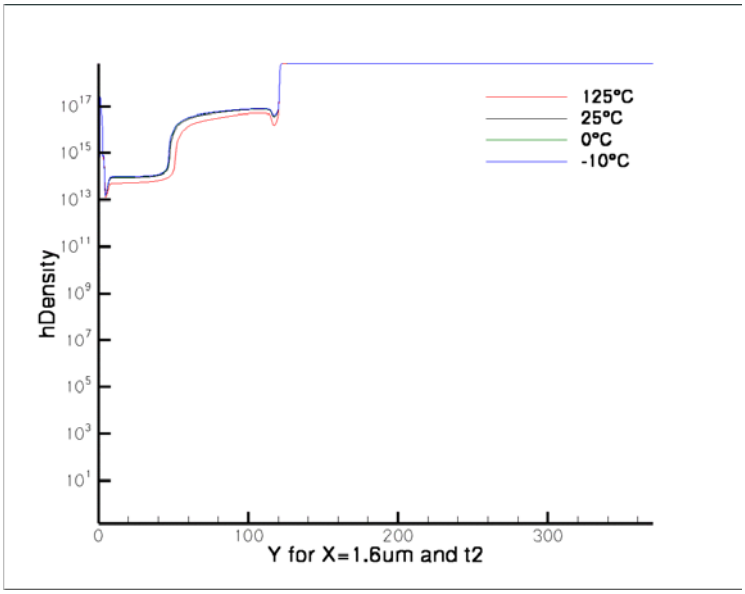


Figure 54 - Holes concentration at time t2 for different temperature values

For these reasons and as we did not have enough time to investigate more on that troubles, we did not present the internal device data in this report. Also as it was summed up in table 12, we could not achieve the full simulation for temperature lower than -10°C. We tried many set up for the thermodynamic option but each time the simulation did not converge.

6.4.7 Trial for improving the convergence

In order to try to obtain the convergence for low temperature (lower than -10°C), we tried to investigate many options:

- Use of two or one *THERMODE* command to see if the convergence can be achieved: no result.
- Use of *PLUGIN* option in the mathematical section: we had coherent results in the same domains as for the converge domains in the case of a coupled solve. The simulations converge but we had some incoherent results at low temperature simulations since the gate pulse has no effect on the device behavior. This means that the device did not switch and the collector emitter voltage kept a constant value (figure 55).
- Add of *INCOMPLETE IONIZATION* model: this model is required for low temperature simulation since the impurity may not be all ionized. The non convergence was not affected by this model.
- Change of some physical models since we do not know the temperature model validity: no effect.
- To reduce time step, this may be critical in the case of non isothermal simulations: no result.

The other points we could not investigate due to the time:

- The troubles which can come from the simulator version ?
- The effect of the mesh on the convergence ?

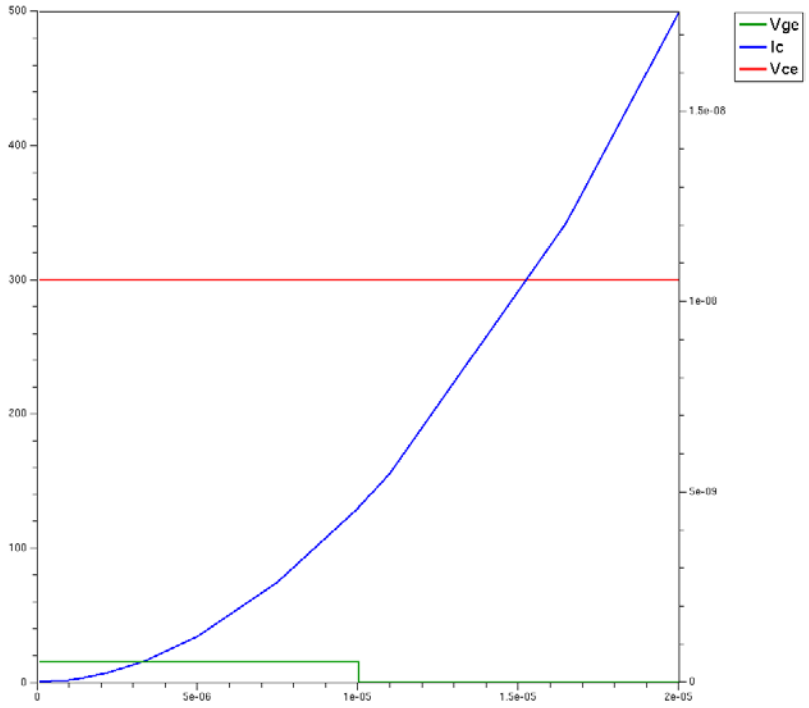


Figure 55 – Use of plugin: the simulation converge but the device does not switch

6.5 *Switching mode with inductive load: improvement of the circuit*

6.5.1 Configuration

For the experiments, we have decided to use a special double gate pulse configuration by keeping the same test circuit (figure 56) which allows to investigate both the turn-on and the turn-off. The simulation was not investigated with this configuration to reduce the simulation time, but it confirms the good waveform shape.

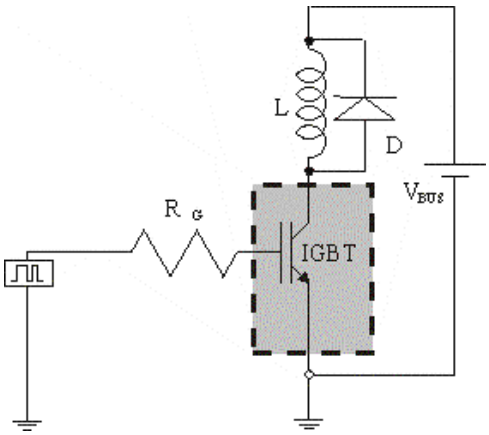


Figure 56 - Inductive load double gate pulse switching test circuit (in grey the 2D IGBT structure)

6.5.2 Simulation file

In order to simulate the IGBT commutation with two pulses, we did some modifications on the ***Solve section*** and on the ***short.pwl*** file :

```
Solve {
        coupled { hole electron poisson contact }
        coupled { hole electron poisson contact circuit}
        # increase Digits to get more accurate currents
        coupled ( Digits=12 Iterations=20 )
                { hole electron poisson contact circuit
                 temperature
                 }
  ##NewCurrentFile=""
        Transient ( InitialStep=2.0e-9 MaxStep=1e-5
                    InitialTime=0 FinalTime=2e-5
                    Increment=1.5 Decrement=2.0
                  )
        {
        coupled { hole electron poisson contact circuit
         temperature
}
        Plot (FilePrefix="n@node@" time=(1.1e-8;5e-6;1.0156e-5;1.1e-5 ) NoOverwrite)
        }

##  System("rm tmp_n@node@_des.plt")

}
#endif
```

We have added 10µs to the simulation:

We have added some times to analyse the structure during the second pulse:

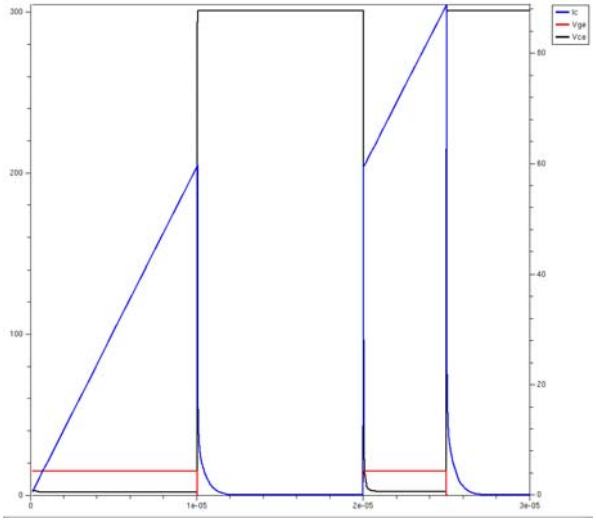
We did some modifications on the ***short.pwl*** file to define the two pulses:

0	**0**
1e-9	**0**
30e-9	**15**
10.03e-6	**15**
10.05e-6	**0**
20e-6	**0**

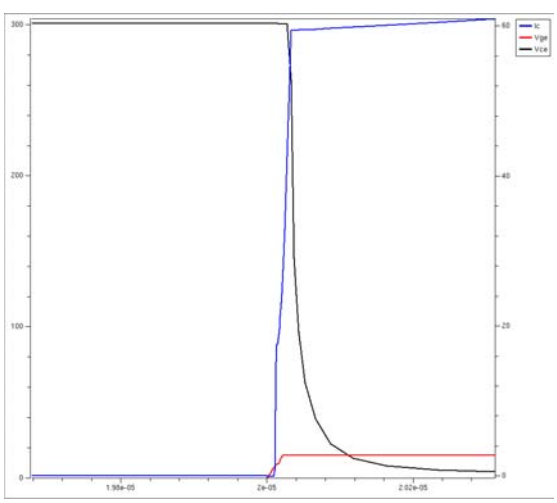
0	0
1e-9	0
30e-9	15
10.03e-6	15
10.05e-6	0
20e-6	0
20.02e-6	15

6.5.3 Results and discussion

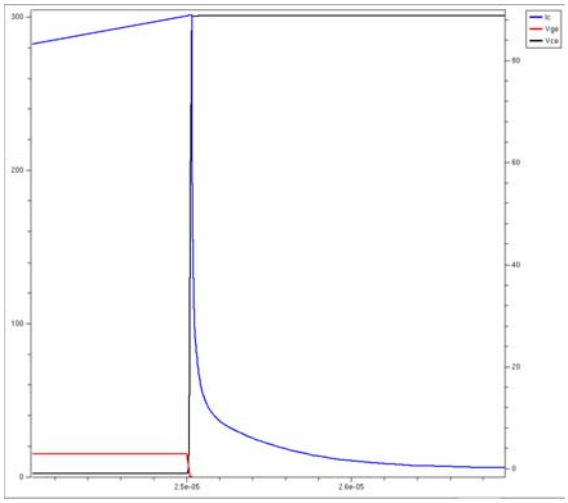
To illustrate, we propose the figures 57 (a), (b) and (c) confirming that this configuration gives an opportunity to focus on the two transients. Also it must be added that the dead time which corresponds to the time between the two pulses must be shortened to try to keep the same current level.



(a)



(b)



(c)

Figure 57 - Double gate pulse configuration (a) full waveforms (b) turn-on and (c) turn-off

6.5.4 *Observations*

No specific observation.

7 Global Discussion

7.1 About the results

For the experiments, it has been highlighted that the device behavior has been disturbed by the decoupling capacitor and the connection of the power module to the external components (inductance, capacitor, connection to the DC voltage …). The design of a specific test circuit for low temperature operation is not so simple since many additional devices have to be used with specific properties especially regarding to the temperature operating range. The limitation of the current within the device under test for the switching operation was on purpose and not due to a lack of equipment (high current probe or inductance). In fact, the low temperature configuration involves specific test conditions which were not so obvious to manage by the short duration of the project.

For the simulation, the non convergence of some simulations at low temperature could not be solved whereas at Toyota CRLD these simulations seem to give correct results. Nowadays, we are still trying to focus on that point by contacting ISE support software center.

7.2 About the project organization

The six months collaboration between Toyota CRDL and IXL Laboratory was a good experience to see how such kind of project has to be managed. Due the hard schedule of each partner, it was not so obvious to communicate even if email and video conference provide good opportunities for that.

The main point which has to be considered in the organization is the exact definition of the objectives of the project. When the DNA was written, the project was determined only by a sentence which was too wide regarding the goal. We had to manage to see how we could bring our knowledge for the simulations and the experiments according to the request of Toyota CRDL.

For the future project, we guess that the definition and the objectives of the study have to be well detailed. Furthermore, monthly reports and regular contact by video conference or even meeting have to be scheduled.

8 Conclusion

The objectives of this project could not be completely reached due to the non convergence of some simulations. Also the experiments were carried out with the available equipments and in some case it could not be possible to achieve the real operating conditions. Also we missed some internal device analysis to explain in a better way the device behavior at -40°C.

However, during the six months project, some trends were highlighted to answer the question: what can be the behavior of Trench IGBT at low temperature?

On one hand, the static mode operation has shown that:

- The gate threshold voltage increases when the temperature decreases due to an increase of the intrinsic concentration n_i.
- For the chosen gate emitter voltage, the saturation current decreases when the temperature decreases. This effect strongly depends on the chosen current load. In our case, the electron current from the MOSFET component is not dominant. The gain of the bipolar component of the IGBT is reduced but is still more dominant than the electron current.
- The rise of the on-state voltage drop, for the fixed load current is also linked to the reduction of the minority carriers concentration due to the reduction of the gain of the bipolar component.
- The breakdown voltage, as well as, the leakage current are reduced when the temperature decreases.

On another hand, the switching mode operation has shown that:

- During turn-on, the temperature has not a strong influence on the Trench IGBT since the MOSFET component is the main active part of the Trench IGBT for turn-on. The di/dt and the dv/dt are almost the same for each temperature. The effect of the gate resistance variation is to delay the turn-on of the device but also changes slightly the di/dt.
- During the on-state, the collector current is reduced as it was observed for the static operation.
- During the turn-off, it is possible to see that the temperature has an direct effect on the current tail of the Trench IGBT. However, at low temperature, the gain of the bipolar component is already low, and the reduction of the temperature does not involve a dramatic reduction of the current tail. The di/dt is not change whereas the dv/dt seems to be a little bit

modified by the reduction of the temperature. The gate resistance delays the turn-off transient but also has a little effect on the dv/dt. It must also be noted that the current tail of the tested Trench IGBT is not so typical as for the conventional planar device. It is can observed that the current decreases strongly and after there is a little bump, which is more typical from a zero voltage turn-off switching.

- The graphs of the power losses indicate clearly that when the temperature decreases the peak power losses during both the turn-on and the turn-off transients are reduced. The gate resistance also influences theses losses and a low gate resistance value induces a reduction of the instantaneous peak power.

9 References

[1] J.P. Russel, A.M. Goodman, L.A. Goodman, J.M. Neilson, "The COMFET - A New High Conductance MOS-Gated Device", IEEE Electron Devices Letters, vol.4, March, pp.63-65, 1983.

[2] B.J. Baliga, M.S. Adler, R.P. Love, P.V. Gray, N. Zommer, "The Insulated Gate Transistor: A New Three-Terminal MOS Controlled Bipolar Power Device", IEEE Trans. on Electron Devices, vol.31, no.6, June, pp.821-828, 1984.

[3] M. Trivedi, K. Shenai, "Trade-Off in IGBT Safe Operating Area and Performance Parameters", Proc. of the IEEE IAS 1997, pp.949-954.

[4] C.V. Godbold, J.L. Hudgins, C. Braun, W.M. Portnoy, "Temperature variation effects in MCTs, IGBTs, and BMFETs", Power Electronics Specialists Conference, 1993, 20-24 June 1993, pp.93-98

[5] T.P.Chow, K.C.So, D.Lau. "Operation of IGBT's at low temperatures" Proc. of the IEEE International Symposium on Power Semiconductor Devices and ICs, April 1992, pp.226-228

[6] J.L Hudgins, S.Menhart, W.M Portnoy, V.A Sankaran "Temperature variation effects on the switching characteristics of MOS-Gate devices", Proc. EPE-MAPED Conf. Rec, September 1991, pp.262-266

[7] E. Santi, X. Kang, A. Caiafa, J.L. Hudgins, P.R. Palmer, D.Q. Goodwine, "Temperature Effects on Trench-Gate Punch-Through IGBTs" IEEE Transactions on Industry Applications, vol.40, no2, March-April 2004, pp.472- 482

[8] S. Azzopardi, E. Woirgard, JM. Vinassa, O. Briat, C. Zardini, A Systematic "Performances Evaluation of New 1200V Punch-Through IGBTs Structures Using Local Lifetime Control under Hard- and Soft-Switching at High Temperature", IEEE Transactions on Power Electronics, vol.19, no.1, January 2004, pp.231-241.

10 Annexes

10.1 Annex 1: Mitsubishi Power Module data sheet CM150DY-24NF

CM150DY-24NF

HIGH POWER SWITCHING USE

CM150DY-24NF

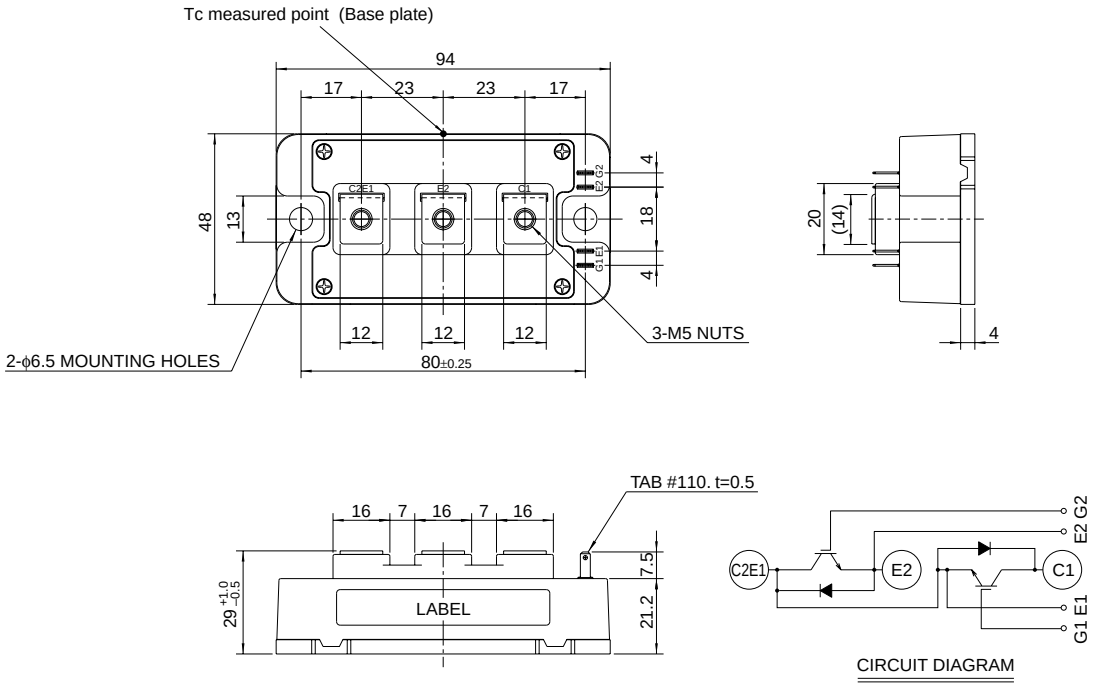
- I_C 150A
- V_{CES} 1200V
- Insulated Type
- 2-elements in a pack

APPLICATION

General purpose inverters & Servo controls, etc

OUTLINE DRAWING & CIRCUIT DIAGRAM

Dimensions in mm



MITSUBISHI ELECTRIC

CM150DY-24NF

HIGH POWER SWITCHING USE

MAXIMUM RATINGS (Tj = 25°C)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CES}	Collector-emitter voltage	G-E Short	1200	V
V_{GES}	Gate-emitter voltage	C-E Short	±20	V
I_C	Collector current	DC, T_C' = 110°C*3	150	A
I_{CM}		Pulse (Note 2)	300	A
I_E (Note 1)	Emitter current		150	A
I_{EM} (Note 1)		Pulse (Note 2)	300	A
P_C (Note 3)	Maximum collector dissipation	T_C = 25°C	780	W
T_j	Junction temperature		–40 ~ +150	°C
T_{stg}	Storage temperature		–40 ~ +125	°C
V_{iso}	Isolation voltage	Main Terminal to base plate, AC 1 min.	2500	V
—	Torque strength	Main Terminal M5	2.5 ~ 3.5	N • m
—		Mounting holes M6	3.5 ~ 4.5	N • m
—	Weight	Typical value	310	g

ELECTRICAL CHARACTERISTICS (Tj = 25°C)

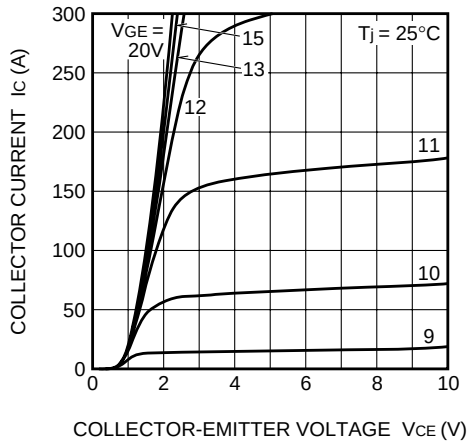
Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CES}	Collector cutoff current	V_{CE} = V_{CES}, V_{GE} = 0V		—	—	1	mA
$V_{GE(th)}$	Gate-emitter threshold voltage	I_C = 15mA, V_{CE} = 10V		6	7	8	V
I_{GES}	Gate leakage current	V_{GE} = V_{GES}, V_{CE} = 0V		—	—	0.5	µA
$V_{CE(sat)}$	Collector-emitter saturation voltage	T_j = 25°C	I_C = 150A, V_{GE} = 15V	—	1.8	2.5	V
		T_j = 125°C		—	2.0	—	
C_{ies}	Input capacitance	V_{CE} = 10V, V_{GE} = 0V		—	—	35	nF
C_{oes}	Output capacitance			—	—	3	nF
C_{res}	Reverse transfer capacitance			—	—	0.68	nF
Q_G	Total gate charge	V_{CC} = 600V, I_C = 150A, V_{GE} = 15V		—	1000	—	nC
$t_{d(on)}$	Turn-on delay time	V_{CC} = 600V, I_C = 150A, V_{GE1} = V_{GE2} = 15V, R_G = 2.1Ω, Inductive load switching operation, I_E = 150A		—	—	120	ns
t_r	Turn-on rise time			—	—	80	ns
$t_{d(off)}$	Turn-off delay time			—	—	450	ns
t_f	Turn-off fall time			—	—	350	ns
t_{rr} (Note 1)	Reverse recovery time			—	—	150	ns
Q_{rr} (Note 1)	Reverse recovery charge			—	7.5	—	µC
V_{EC}(Note 1)	Emitter-collector voltage	I_E = 150A, V_{GE} = 0V		—	—	3.2	V
$R_{th(j-c)Q}$	Thermal resistance*1	IGBT part (1/2 module)		—	—	0.16	°C/W
$R_{th(j-c)R}$		FWDi part (1/2 module)		—	—	0.25	°C/W
$R_{th(c-f)}$	Contact thermal resistance	Case to fin, Thermal compound Applied*2 (1/2 module)		—	0.07	—	°C/W
$R_{th(j-c')Q}$	Thermal resistance	Tc measured point is just under the chips		—	—	0.093*3	°C/W
R_G	External gate resistance			2.1	—	21	Ω

*1 : Tc measured point is shown in page OUTLINE DRAWING.
*2 : Typical value is measured by using Shin-etsu Silicone "G-746".
*3 : Tc' measured point is just under the chips.
If you use this value, $R_{th(f-a)}$ should be measured just under the chips.

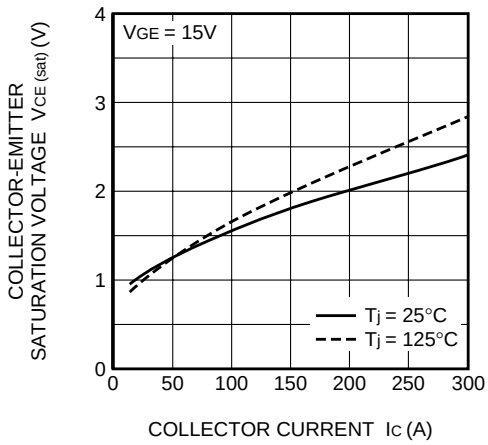
Note 1. I_E, V_{EC}, t_{rr} & Q_{rr} represent characteristics of the anti-parallel, emitter to collector free-wheel diode (FWDi).
2. Pulse width and repetition rate should be such that the device junction temp. (T_j) does not exceed T_{jmax} rating.
3. Junction temperature (T_j) should not increase beyond 150°C.

PERFORMANCE CURVES

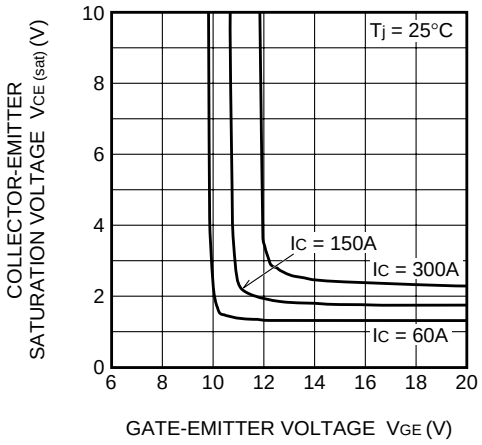
OUTPUT CHARACTERISTICS (TYPICAL)



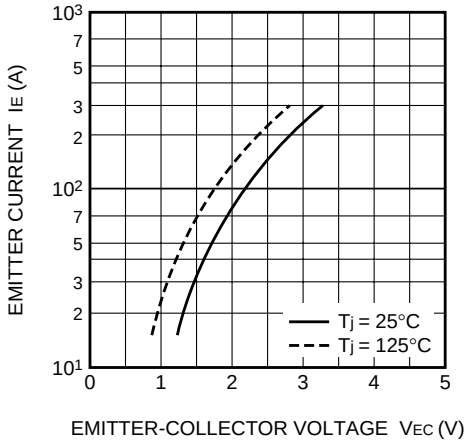
COLLECTOR-EMITTER SATURATION VOLTAGE CHARACTERISTICS (TYPICAL)



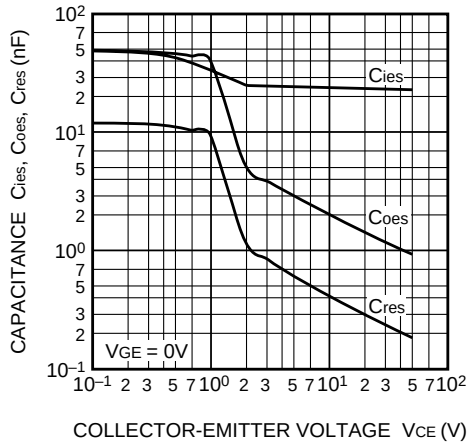
COLLECTOR-EMITTER SATURATION VOLTAGE CHARACTERISTICS (TYPICAL)



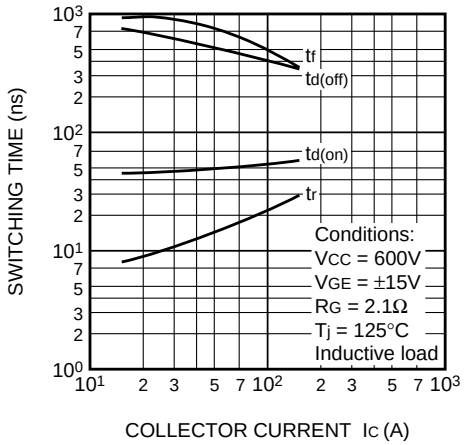
FREE-WHEEL DIODE FORWARD CHARACTERISTICS (TYPICAL)



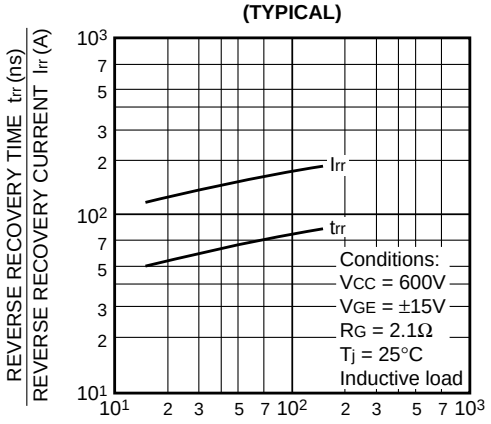
CAPACITANCE–VCE CHARACTERISTICS (TYPICAL)



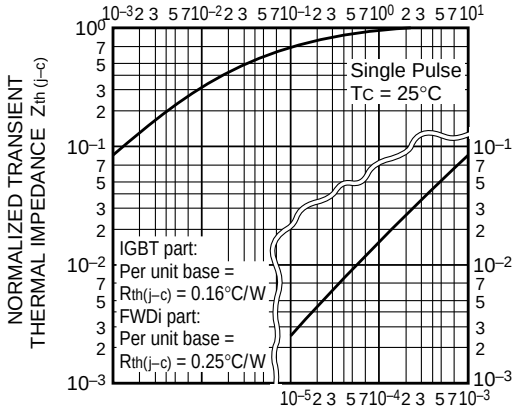
HALF-BRIDGE SWITCHING CHARACTERISTICS (TYPICAL)



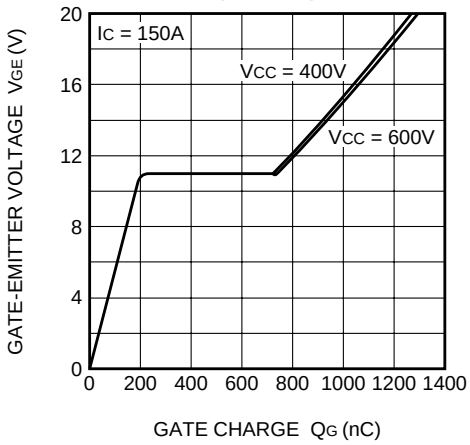
REVERSE RECOVERY CHARACTERISTICS OF FREE-WHEEL DIODE (TYPICAL)



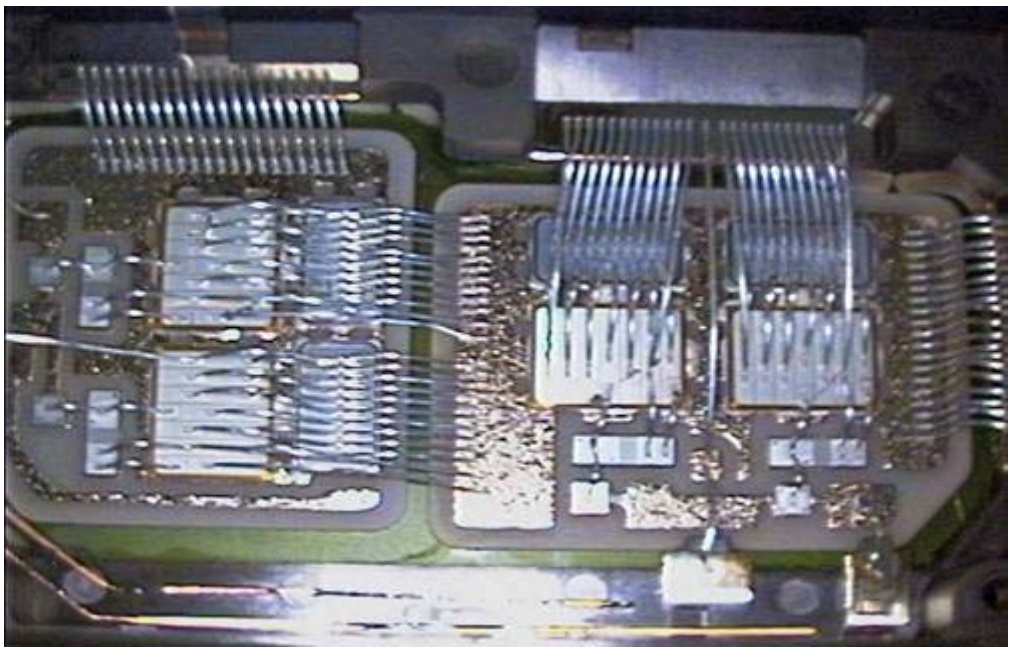
TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (IGBT part & FWDi part)

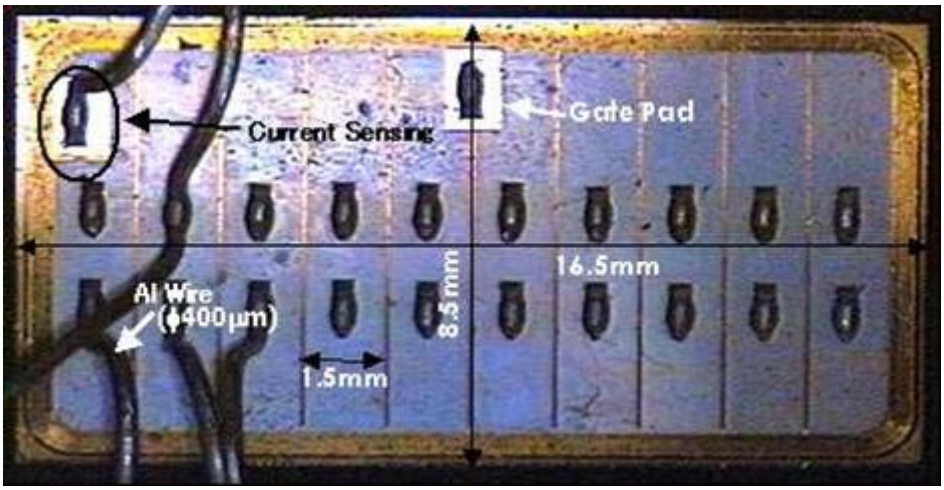


GATE CHARGE CHARACTERISTICS (TYPICAL)

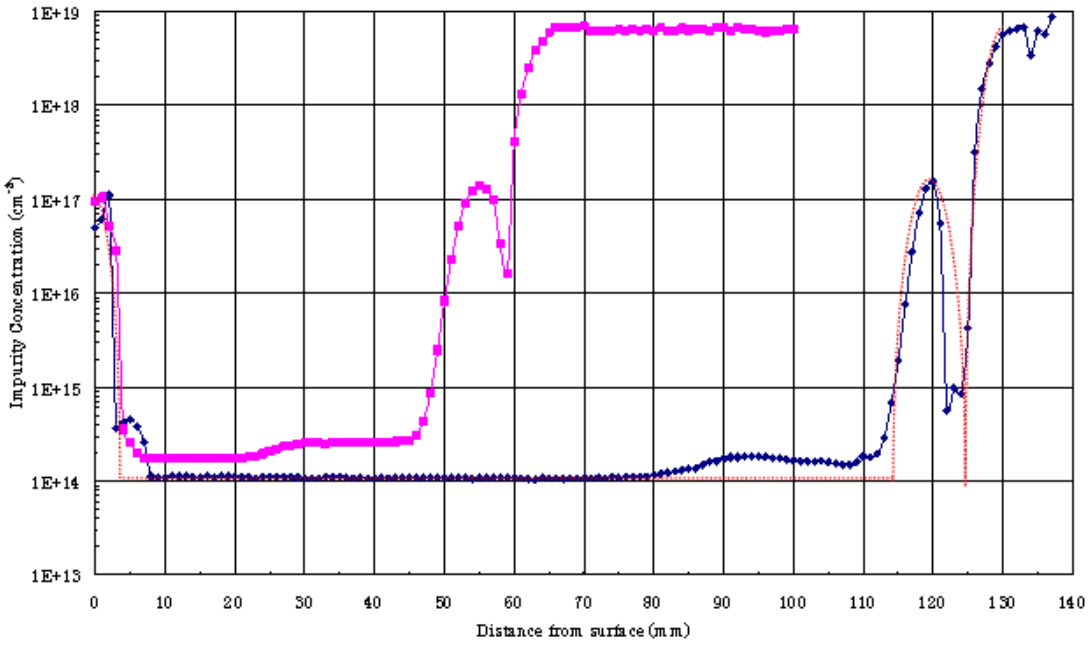


10.2 Annex 2: Power module photography

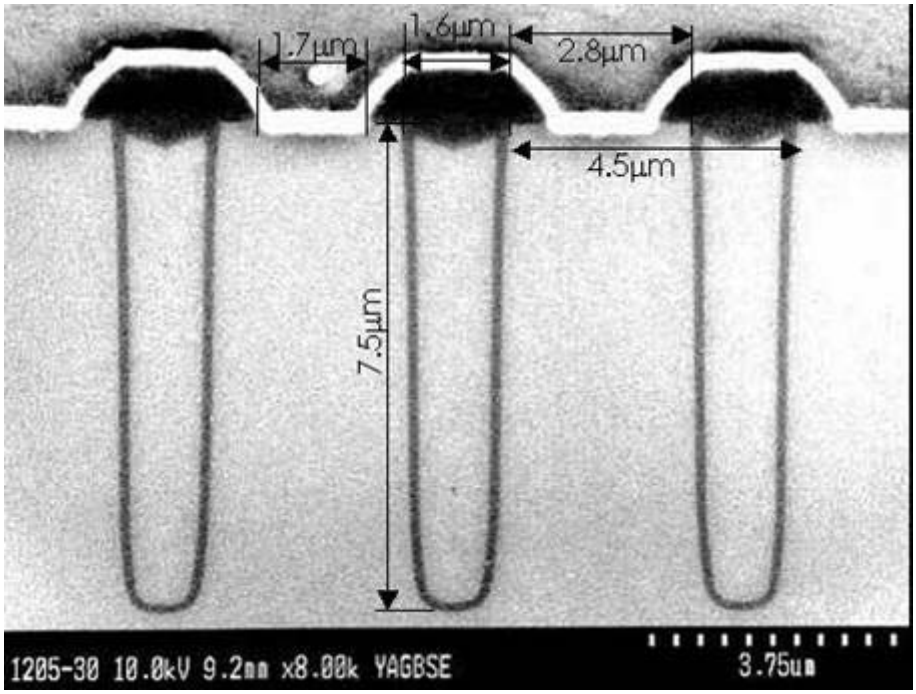




10.3 Annex 3: Concentration profile of CM300DU-12F and CM200DU-24F

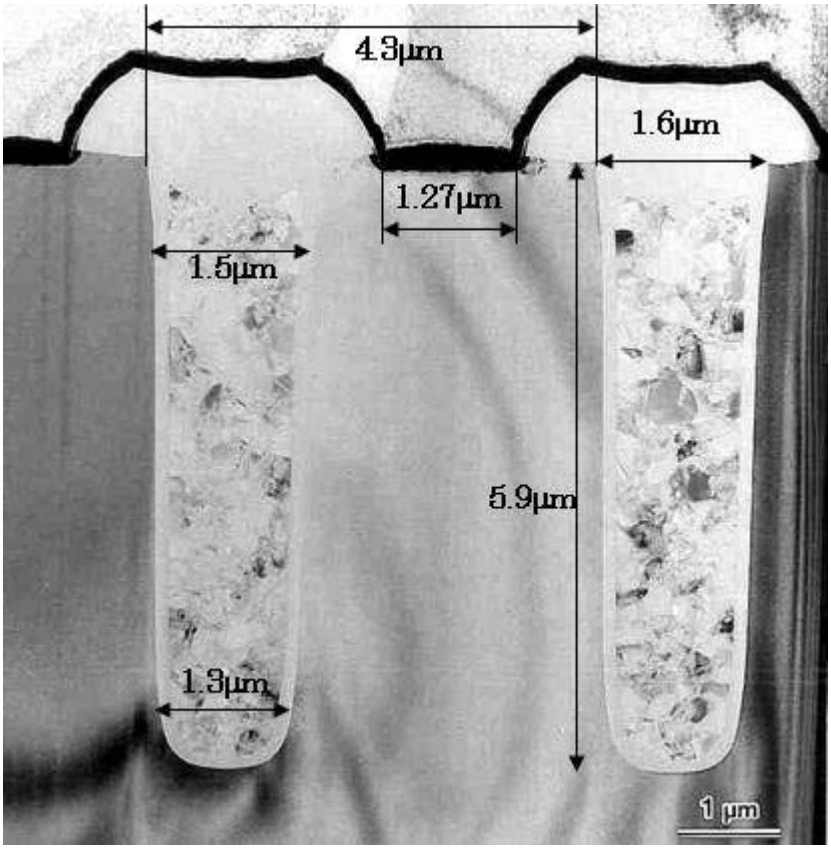


10.4 Annex 4: SEM and TEM Analysis

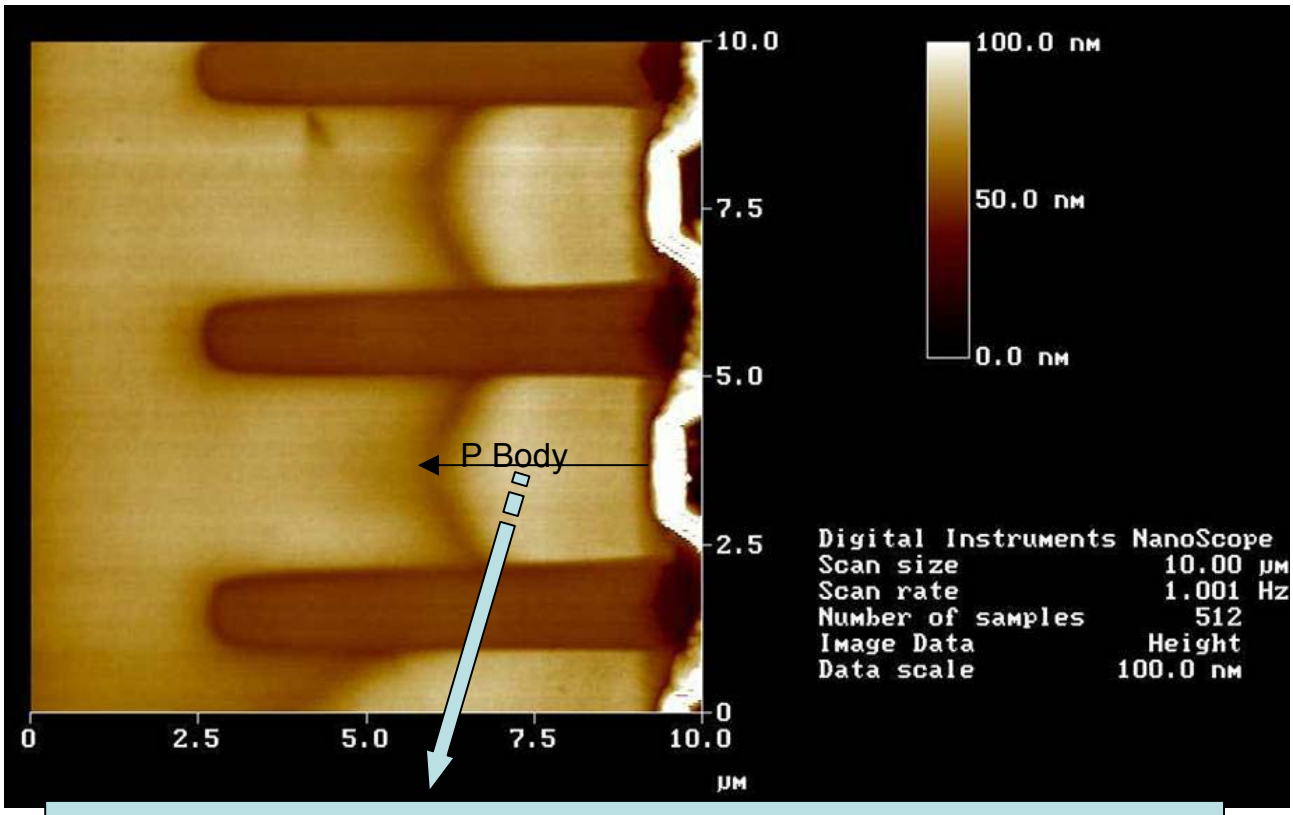


SEM Image

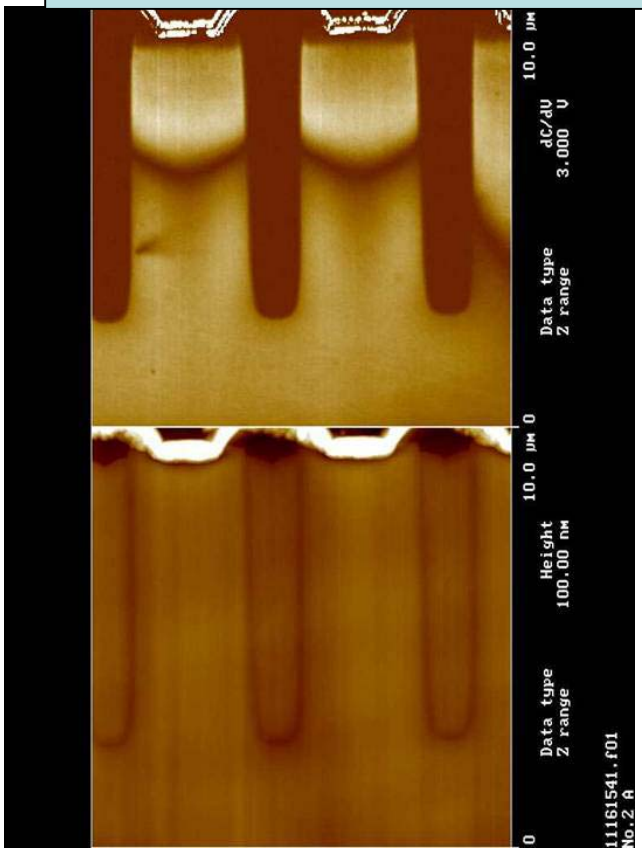
TEM Image



Trench depth might be 6 to 6.5µm.



P body junction might be deeper than this because of the deep graded junction.



10.5 Annex 5: Paper 1 submitted to IPEC 05

A very simple and low cost test circuit for hard- and soft-switching IGBT characterization

S. Azzopardi[1], M. Ishiko[2], A. Benmansour[1], R. Roy-Pelat[1], C. Zardini[1]

[1] IXL – CNRS UMR5818 - University of Bordeaux 1
351, cours de la Libération
33405 Talence Cédex FRANCE
azzo@ixl.u-bordeaux.fr

[2] TOYOTA CENTRAL R&D LABS., INC.
Nagakute, Aichi
480-1192, JAPAN
ishiko@mosk.tytlabs.co.jp

***Topic 1*: Power semiconductor devices**

Abstract - The use of IGBT power module designing as single-leg inverter is more and more popular for customers. It is always useful to characterize such device under various operating modes. In that purpose, this power module has been considered to develop a very simple and low cost experimental test circuit for IGBT characterization. Both hard- and soft-switching operations (by the mean of zero-current switching turn-on and zero-voltage switching turn-off) can be investigated with the same pulse gate configuration and by adding some external additional passive components. Each parameter (temperature, voltage, current, gate resistance) can be adjusted independently to have a full device characterization. The circuit is described and some results are presented and commented.

1. Introduction

Research in the field of power semiconductor technology allows to improve continuously power devices. The goal of power semiconductor devices manufacturers is to find the ideal device: high switching frequency, no loss, easy drive, and so on. Since its first description in the early 80s, the Insulated Gate Bipolar Transistor (IGBT) has considerably been evolved and has gained wide acceptance in switched mode power converters and inverters. Widely used for medium voltage and medium current applications range (300-2500V / 50-200A), it allows a good trade-off between the switching speed, the on-state voltage drop and the ruggedness.

Power semiconductor devices can operate under two main switching configurations: hard-switching and soft-switching techniques. In order to verify the appropriate behavior of the device according to the application, most of the time users need to characterize each power transistor. Usually IGBT can be found in a power module as a single-leg inverter unit including two IGBTs and two freewheeling diodes. Some tests circuits can be found in the literature [1-5], but the structure or the pulse gate configuration is not so simple.

In this paper, we propose the design of a very simple and low cost test circuit for IGBT characterization. The use of a specific pulse configuration allows to investigate not only hard-switching turn-on and turn-off but also soft-switching such as zero-voltage switching turn-off and zero-current switching turn-on. Some experimental results are presented allowing to validate the test circuit design.

2. Hard and soft switching modes

Hard-switching: This operating mode is widely used in motor control, where devices require to turn-on and turn-off the entire load current during each switching phase. As the overlap between the voltage and the current of power semiconductor devices is quiet important, during turn-on and turn-off, devices are subjecting to high switching stresses and high switching power losses.

Soft-switching*:* The aim of the soft-switching is to reduce the overlap between the voltage and the current of power semiconductor devices. It involves to turn devices on or off with minimal switching stress. Therefore, it is possible to reduce switching losses, dv/dt, EMI, noise and to improve the switching frequency, as well as the size reduction of converters. Two main techniques are used for soft-switching: Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS). ZVS allows switching on and off the device when the voltage across the device is effectively zero, and ZCS allows switching the device when the current conducted by the device is zero.

3. Power module description

This study focuses on IGBT dice attached to power modules as described below. However, it is possible to use single IGBT chip package to perform the same test circuit configuration. The power modules which will be used to design this test circuit can be observed on the figure 1.

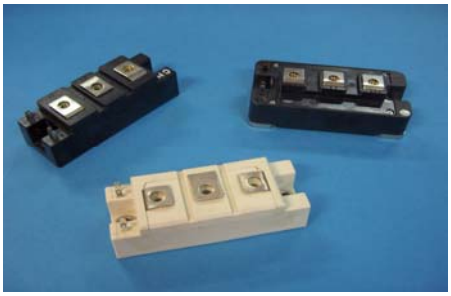


Fig.1 – Single-leg inverter power module external view

Nowadays many manufacturers propose such power module arrangement including two IGBTs and two freewheeling diodes as shown in figure 2. The main advantages come from the reduction of the stray

inductance and also the possibility to change in once a full single-leg inverter. The main drawback is that in case of one device fails (diode or IGBT), it is necessary to change the complete module unit.

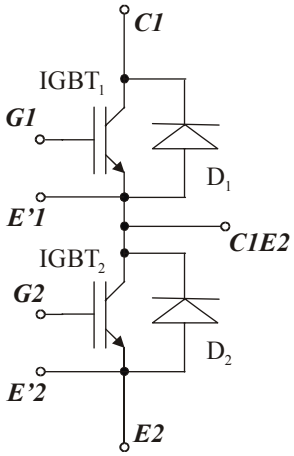


Fig.2 – Single-leg inverter power module arrangement

4. Test circuit design

Power circuit: Based on the power module described in figure 2, and by considering the power devices $IGBT_2$ and D_1, and adding some external passive components, it is possible to obtain a first version of the test circuit as depicted in figure 3.

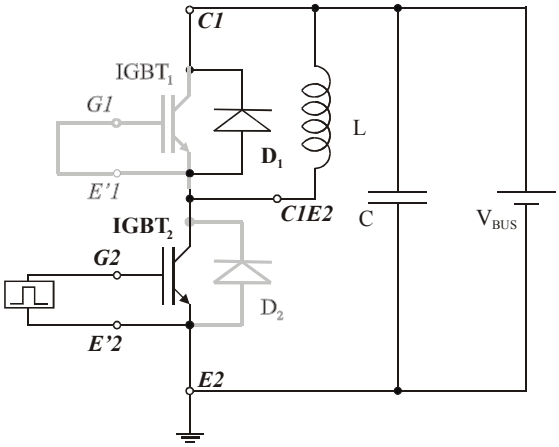


Fig.3 – First version of the test circuit

It can be easy to notice that if this test circuit is used, the measure of the collector current of $IGBT_2$, which is the Device Under Test (DUT), will not be possible since the current of the available connection C1E2 corresponds to the current passing through the inductor.
This current will be equal to the collector current when the device has been switched on, but it will be equal to the current of the freewheeling diode when the device has been switched off. Then, the characterization of the DUT will not be fully efficient for turn-on and turn-off. This is the main drawback of using such kind of power module to characterize a power transistor.
In order to obtain the full current waveform of the DUT, it is necessary to add an external diode (D_{ext}) as shown in figure 4. In order to reduce the influence of the reverse recovery phenomenon of the diode, it is highly recommended to use a Schottky diode.

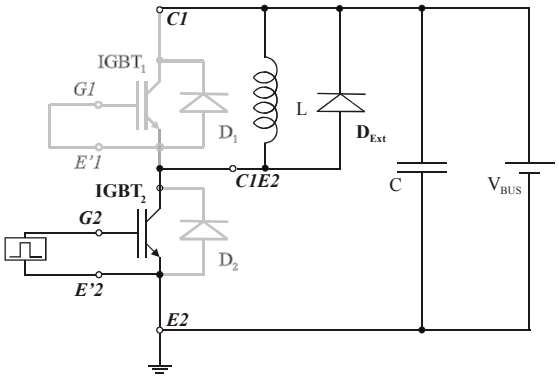


Fig.4 – Influence of the temperature on the turn-off losses

Finally, figure 5 illustrates the test circuit design: very simple and does not need so many external devices.

Fig.5 – Power test circuit

Command circuit: The command circuit has been developed with the help of a PIC microcontroller. More details will be presented in the full paper. It is easy to set up the various pulse durations thanks to a keyboard as shown in figure 5.

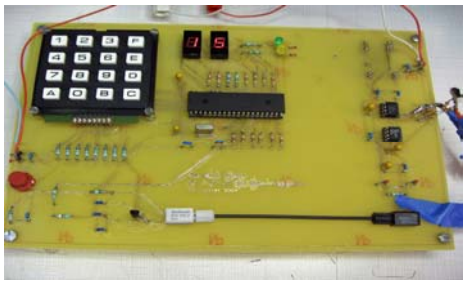


Fig.5 – Command board

Also as it can be seen in figures 6 and 7, two kinds of pulse configurations can be selected.

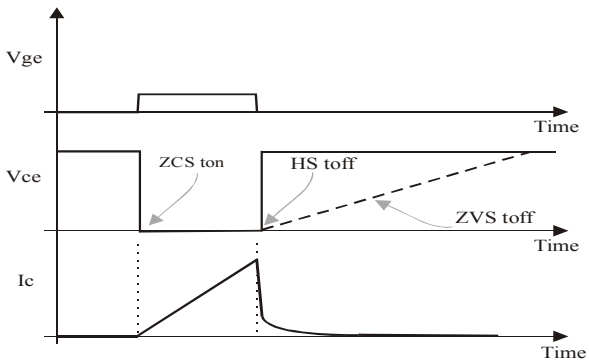


Fig.6 – Single-pulse configuration

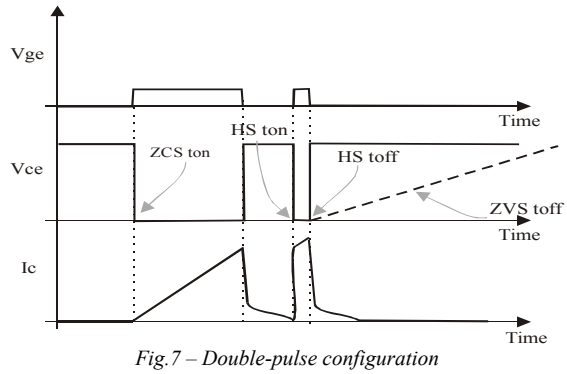


Fig.7 – Double-pulse configuration

The first one allows to switch the device on and off under a single or repetitive pulse based on a specific period. The main drawback is that only the hard switching turn-off, the zero-voltage switching turn-off by adding an external capacitor to the test circuit and the zero-current switching turn-on can be studied. It is not possible to focus on the hard-switching turn-on.
The second configuration permits to have a second pulse applied to the gate electrode which can afford a study of all previous switching modes but also the hard switching turn-on. It has to be noticed that the second pulse should be as short as possible if the user wants to keep a constant current for turn-on and turn-off.

5. Test conditions and instrumentation

The input voltage V_{BUS} can be adjusted by using external power supply. The input capacitor C allows to supply high instantaneous peak current. The inductive load L has been built by using an E65/32/27-3F3 core. The freewheeling diode is a 50HQO45 Schottky diode. The gate driver of the IGBTs is a TC4420.
The experimental collector-emitter voltage and collector current waveforms of the DUT have been measured with the high voltage probe TEKTRONIX model 2.5kV and the current probe TEKTRONIX TCP220. For the switching power loss measurements, the use of the TEKTRONIX oscilloscope model TDS5054 allowed to compensate the delay between the voltage and the current probes using a calibration source.

6. Experimental validation

The double-pulse configuration for an inductive load is illustrated in figure 8. The current has been set up to 20A and V_{BUS} to 50V. The test has been performed on $IGBT_2$.

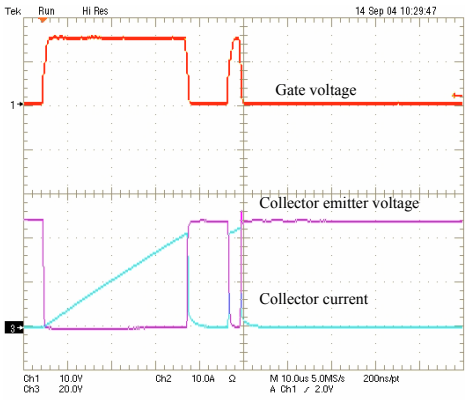


Fig.8 – Full double-pulse configuration

A zoom on each specific part of figure 8 are then shown in the following figures.
Figure 9 proposes the turn-on under zero-current switching operating mode. It is important to note that even if this circuit is not a resonant converter, when the pulse on the gate reach the threshold voltage, the device is turn-on with zero current whereas the collector-emitter voltage is equal to V_{BUS}.

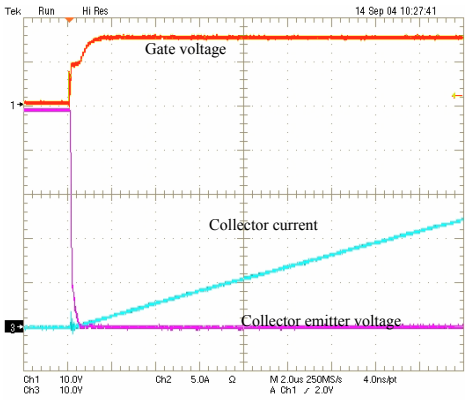


Fig.9 – Zero-current switching turn-on

The hard-switching turn-on is depicted in figure 10. The oscillations are due to the stray inductance from the external circuit. The freewheeling diode effect can be observed on the current waveform, but it has been reduce by the use of a Schottky diode.

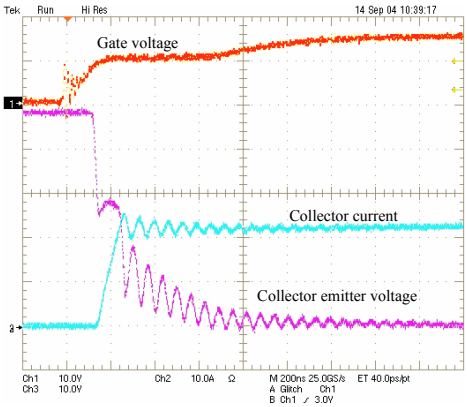


Fig.10 – Hard-switching turn-on

Finally, figure 11 and 12 plot the turn-off under hard-switching and soft-switching by the mean of zero voltage switching. As well know, the value of the external capacitor will have a direct effect on the dv/dt.

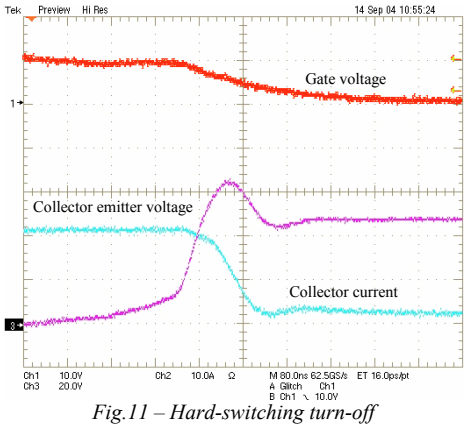


Fig.11 – Hard-switching turn-off

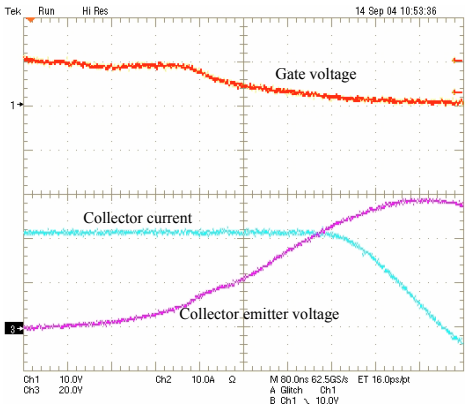


Fig.12 – Zero-voltage switching turn-off

7. Conclusion

Based on simple considerations, a very simple and low cost test circuit to characterize power semiconductor devices under hard-switching and soft-switching operating modes has been investigated.

The use of a specific pulse-gate command allows to analyze hard-switching turn-on and turn-off, zero-voltage-current turn-on switching and zero-voltage switching turn-off. The results show good agreement with theoretical waveforms.

One of the merits of such circuit is that it is possible to adjust external parameters independently such as temperature, gate resistance, load type, voltage and current. It can also be possible to study the interaction between the freewheeling diode and the IGBT. The circuit can also be improved by considering a better connection between each part in order to reduce parasitic elements.

References

[1] B.M. Song, H. Zhu, J-S. Lai, A.R. Hefner "Switchng Characteristics of NPT- and PT-IGBTs under Zero-Voltage Switching Conditions" in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1995, pp. 1055-1060.

[2] S. Pendharkar, C. Winterhalter, M. Trivedi, H. H. Li, A. Kurnia, D. Divan, and K. Shenai, "Test Circuits for Verification of Power Device Models," in *Dig. IEEE Industrial Applications Society (IAS) Ann. Mtg.*, 1995, pp. 1055-1060.

[3] M. Trivedi, R. Evazians, and K. Shenai, "Test Circuits for Characterizing Power Transistors in ZVS and ZCS Circuits," in *Proc. IEEE Instrumentation and Measurement Technology Conf. (IMTC)*, 1998, pp. 515-518.

[4] A. Claudio, M. Cotorogea, J. Aguayo, L.G. Vela "Experimenental and Simulation of the PT-IGBT under ZCS Operation in a Special Test Circuit", in *Proc. COBEP 1999, pp.56-61*.

[5] S. Azzopardi, J.M. Vinassa, E. Woirgard, C. Zardini, O. Briat, "A Systematic Hard- And Soft-Switching Performances Evaluation Of 1200v Punch-Through IGBT Structures ", in *IEEE Transactions On Power Electronics*, Vol. 19, No. 1, Pp.231- 241, 2004.

10.6 Annex 6: Paper 2 submitted to IPEC 05

Low temperature Trench IGBT characterization under static and dynamic operations

S. Azzopardi[1], M. Ishiko[2], A. Benmansour[1], R. Roy-Pelat[1], C. Zardini[1]

[1] IXL – CNRS UMR5818 - University of Bordeaux 1
351, cours de la Libération
33405 Talence Cédex FRANCE
azzo@ixl.u-bordeaux.fr

[2] TOYOTA CENTRAL R&D LABS., INC.
Nagakute, Aichi
480-1192, JAPAN
ishiko@mosk.tytlabs.co.jp

***Topic 1*: Power semiconductor devices**

Abstract – The purpose of this study is to focus on the low temperature Trench IGBT characterization under static and dynamic operations by the aim of intensive measurements. The analysis of the Trench IGBT behavior in these conditions is dedicated to the HEV applications. One question can be raised in case of the use of HEV in countries where during winter the temperature drops down -40°C or less: are Trench IGBT strongly affected by the low temperature environment? In this paper, we present some experimental results as well as a methodology to allow low temperature switching measurements by using conventional equipments.

1. Introduction

Technical progress in power electronics depends on the development in the fields of power circuit topologies, power devices technologies and control techniques. Since the 80's, significant new developments have been made in the area of power electronics devices, more precisely for the Insulated Gate Bipolar Transistor (IGBT) [1-2]. Widely used for the medium voltage and medium current application ranges (300-1500V/50-300A), for instance motors drives, DC/DC converters, it allows a good trade-off between the switching speed, the on-state voltage drop and the ruggedness [3].

More recently, HEV like PRIUS started becoming very popular in Japan and US. However, for some countries such as Canada, Russia and even from north European such kind of cars will be submitted to low temperature environment. This condition will be stressful for the power hybrid assembly but it is also necessary to wonder what can happen to the power semiconductor devices. It is well known that the switched power becomes higher and higher and IGBTs used in converters are submitted to high temperature changes, which disturb physical parameters of silicon, and change their behavior. In the other way, what can be the behavior of IGBT submitted to low temperature down to -40°C or -50°C?

In the literature it is possible to find some data related to cryogenic operations on power semiconductor devices [4-5-6], but it needs some very specific and quiet expensive equipment. Furthermore, only very few data are available regarding the low temperature operations of Trench-IGBT [7]. In this paper, we propose to investigate the behavior of Trench IGBT at low temperature from 25°C down to -40°C or -50°C using a very simple and low cost test circuit but also by using conventional equipments. A methodology to realize low temperature experiments is described and some results are presented for the static mode and also turn-on and turn-off under hard switching inductive load.

2. Device structure

The device used is the Trench IGBT CM150DY-24F, 1200V-150A from Mitsubishi Power Semiconductor. Using a punch-through structure (Fig.1), the gate oxide and the conductive poly-silicon gate electrode of the Trench IGBT are formed in a deep narrow trench bellow the chip surface. This structure allows a reduction of the on-state voltage drop by suppressing the JFET resistance, which results from the constriction of the current flow in the region between adjacent cells in the planar structure. Furthermore, the vertical channel requires less chip area and permits an increase in cell density. A local lifetime control, using heavy ion irradiation process, allows to keep a low on-state voltage drop as well as to improve the control of the storage charges in the drift region

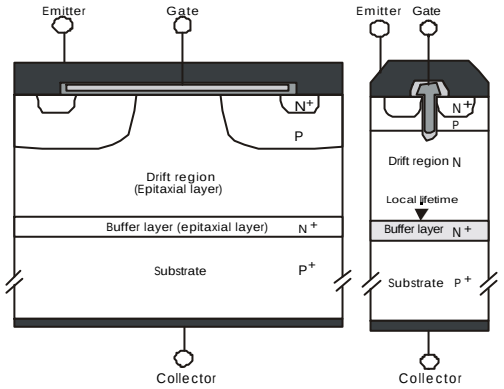


Fig.1 – Structure of the Planar and Trench punch through IGBTs

3. Experimental test bench

Temperature set up equipment: The temperature is controlled by a climatic chamber which allows to set up easily the temperature from +150°C down to -60°C. Thermocouples are used to check the temperature within the device. To be sure that the device temperature is well established, the module is stored to a defined temperature for 40min before obtaining a specific waveform in a specific operating mode.

Static mode: The main part of the static operating mode is based on the use of the curve tracer TEKTRONIX 371A and the design of a specific cable as shown in figure 2. This cable allows to insert the device connector inside the climatic chamber. Measurements comparison with and

without this cable have been made and the characteristics obtained were the same. This allows to validate the use of such cable extension. Thanks to that equipment, the measure of Ic-Vce, Ic-Vge and BVCEO characteristics are possible.

Fig.2 – Specific cable design for TEKTRONIX 371A for low and high temperature operations

Dynamic mode: A very simple and low cost hard-switching test circuit has been used for this study and is given in detail in [8]. It is based on the use of single-leg inverter power module as shown in figures 3 and 4.

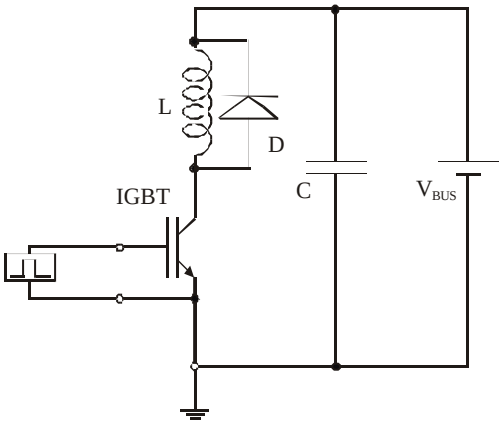


Fig.3 – Hard-switching test circuit [8]

Fig.4 – View of the hard-switching test circuit [8]

Fig.5 – Hard-switching test bench at low temperature

The experimental collector-emitter voltage and collector current waveforms of the DUT have been measured with the high voltage probe TEKTRONIX model 2.5kV and the current probe TEKTRONIX TCP220. For the switching power loss measurements, the use of the TEKTRONIX oscilloscope model TDS5054 allowed to compensate the delay between the voltage and the current probes using a calibration source. The full hard-switching test bench is presented in figure 5.

4. Methodologies

Static mode: Under this operating mode, there is not difficulty to get each static curve. The use of a dedicated software and a computer connected to the curve tracer thanks to a IEEE-GPIB connection allow to obtain static characteristics very easily.

Dynamic mode: Since the test circuit is inserted in a climatic chamber, all the external components, and especially the capacitor, have to withstand the lowest temperature. In our case, a -40°C low temperature limit capacitor has been used. Furthermore, during the switching measurements, it could not be possible to leave the current and voltage probes inside the climatic chamber since it is not recommended to use them under 0°C. As a consequence, to obtain experimental waveforms, it was necessary to open the window of the climatic chamber, to connect the probes and to send the pulse as quick as possible. Then the probes could be removed until the next measurement.

5. Experimental test conditions

Static mode: The temperature was the only parameter and it was decided to perform static experiments from 25°C down to -50°C.

Dynamic mode: Many parameters could be taken into account for the switching operation. Table 1 allows to sum up the chosen values for the experiments.

Temperature	Gate Resistance	Current	Load type
25°C, 0°C, -10°C, -20°C, -30°C, -40°C	**2.2**Ω, 4.7Ω	5A, 10A, 15A, **20A**	resistive **inductive**

Table.1 – Experimental conditions (in bold for the digest)

For technical reason, the load current has been limited to 20A, and the voltage to 50V. More specific test circuit should be used to operate under high current and voltage values.

6. Some results and discussion

Static mode: As it can be observed in figure 6, the dynamic breakdown voltage of the Trench IGBT decreases from 1400V down to 1280V, when the temperature decreases. This phenomenon induces a reduction of the maximum value of the electric field within the structure, as well as the reduction of the depletion region extension. Furthermore, and it can not be possible to see it on this curve, the reverse current also decreases as the intrinsic carrier concentration n_i is reduced. Note

that this breakdown voltage variation is also very important for high temperature values.

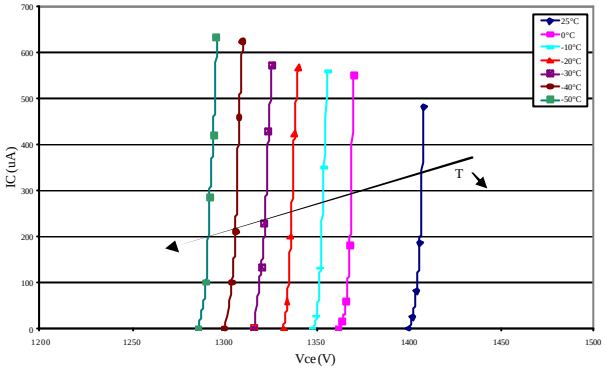


Fig.6 – BVCEO characteristics for T = [25°C down to -50°]

As depicted in figure 7, it is important to see that a low temperature induces an increase of the threshold voltage as reminded in [7]. This is directly linked to the reduction of the intrinsic carrier concentration n_i when the temperature decreases.

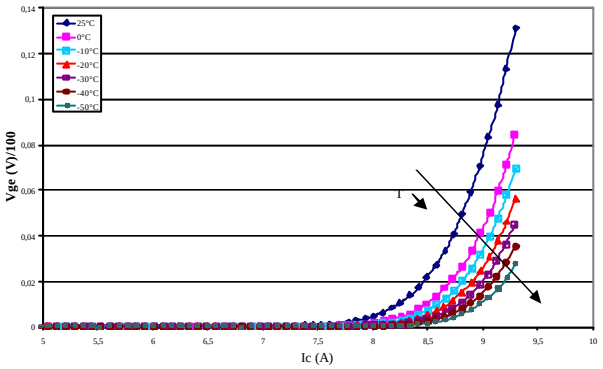


Fig.7 – Ic- Vge characteristics for T = [25°C down to -50°]

One of the most important effects of the temperature reduction can be analyzed in figure 8 where the gate voltage was about 9.55V. For the given current value, it increases the on-state voltage drop because of the reduction of the current gain of the bipolar part of the IGBT, lowering the minority carrier injection. As a consequence, the conductivity modulation is less effective leading to an increase of the on-state power losses.

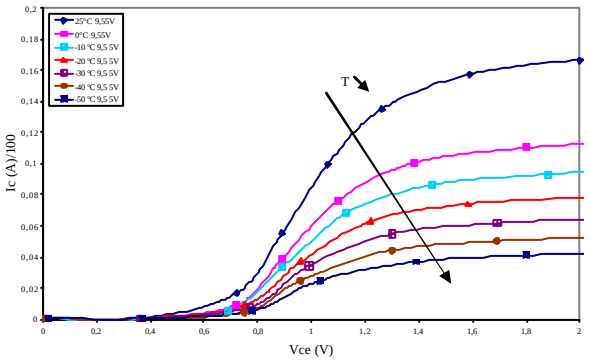


Fig.8 – Ic- Vce characteristics for T = [25°C down to -50°]

Furthermore, when the temperature decreases, the collector current decreases too. For low doping levels, the carrier mobility in silicon increases with the reduction of the temperature which induces an increase of the saturation current level. However, for the given current level the saturation current is reduced. Then it is possible to say that the electron current from the MOS component is not a dominant factor. The decrease of the electron current from the MOS component is higher than the decrease of the current gain of the bipolar part of the Trench IGBT. Furthermore, we may also consider that the gate voltage value is not so high compare to the threshold voltage value and this will have an effect on the device behavior as explained in [5].

Dynamic mode: The whole hard-switching transient will be divided in three parts: turn-on, on-state and turn-off phases. The gate resistance has been set up to 2.2Ω.
Since saturation velocity of carriers and their mobility are increased at low temperature, the switching behavior of the IGBT will be changed.
As it is possible to observe in figure 9 depicting the turn-on, the collector emitter voltage does not change at all when the temperature decreases. As well as the collector-emitter voltage, the collector current is not affected by the temperature decrease. In fact, as the turn-on phase mainly depends on the MOSFET part of the IGBT which is not influenced by the temperature variation, then the IGBT turn-on does not change at all. The oscillations are due to the stray inductance. The collector current overshot comes from the reverse recovery phenomenon of the external freewheeling diode.

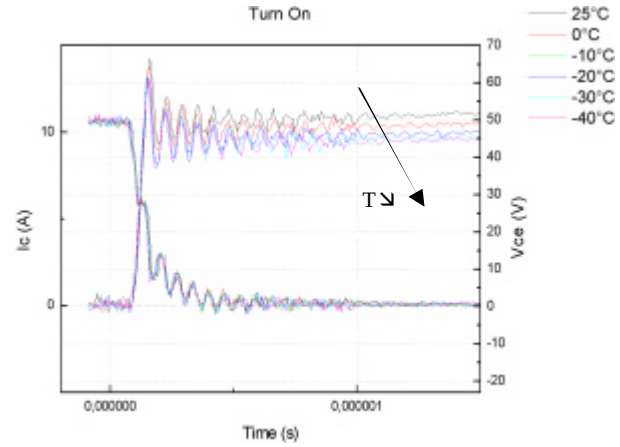


Fig.9 – Hard-switching turn-on for T = [25°C down to -40°]

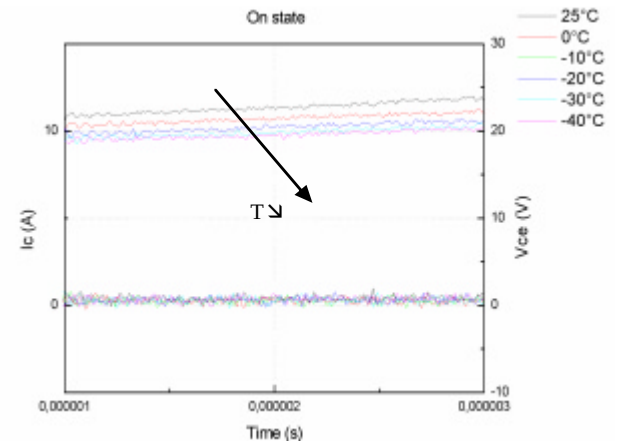


Fig.10 – Hard-switching on-state for T = [25°C down to -40°]

The collector-emitter voltage during the on-state phase, as illustrated in figure 10, does not vary so much since this variation depends also on the collector current level. This current level is lower than for the static mode and in that case, the Trench IGBT on-state voltage drop is not sensitive to low temperature values.

As regarding the collector current, and as it was already mentioned in figure 8, the decrease of the temperature induces a decrease of the collector current for a given gate-emitter voltage. This is again clearly illustrated in figure 10.

When the temperature decreases the overlap between the collector current and the collector-emitter voltage during turn-off is reduced as shown in figure 11.

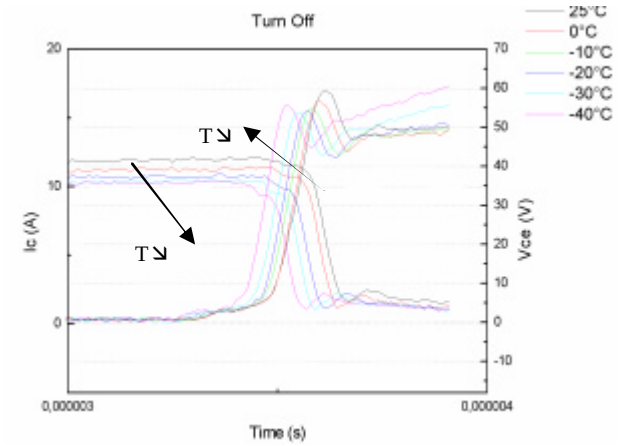


Fig.11 – Hard-switching turn-off for T = [25°C down to -40°]

This is mainly due to the reduction of the collector current value. When we focus on the current tail, which is a typical characteristic of IGBT due to minority carriers responsible for a stored charge in the drift region, it is obvious to notice that the tail is not so much influenced by the temperature variation for the chosen load current. The effect of the temperature is stronger when the temperature rises, since the bipolar part is strongly sensitive to high temperature value.

The power switching losses and the effect of the gate resistance is not presented in the digest.

7. Conclusion

The Trench IGBT characterization at low temperatures has been investigated with the help of intensive measurements under static and dynamic operating modes. Specific test benches have been design to perform these experiments by using conventional equipments.

It has been shown that the low temperature has also a strong effect on the IGBT behavior as well as the high temperature. The properties of the silicon are changed which has a main effect on the device current and voltage waveforms.

More investigations are in progress to consider the device structure at low temperature by the help of the physically-based bi-dimensional device structure simulator.

References

[1] J.P. Russel, A.M. Goodman, L.A. Goodman, J.M. Neilson, "The COMFET - A New High Conductance MOS-Gated Device", IEEE Electron Devices Letters, vol.4, March, pp.63-65, 1983.

[2] B.J. Baliga, M.S. Adler, R.P. Love, P.V. Gray, N. Zommer, "The Insulated Gate Transistor: A New Three-Terminal MOS Controlled Bipolar Power Device", IEEE Trans. on Electron Devices, vol.31, no.6, June, pp.821-828, 1984.

[3] M. Trivedi, K. Shenai, "Trade-Off in IGBT Safe Operating Area and Performance Parameters", Proc. of the IEEE IAS 1997, pp.949-954.

[4] C.V. Godbold, J.L. Hudgins, C. Braun, W.M. Portnoy, "Temperature variation effects in MCTs, IGBTs, and BMFETs", Power Electronics Specialists Conference, 1993, 20-24 June 1993, pp.93-98

[5] T.P.Chow, K.C.So, D.Lau. "Operation of IGBT's at low temperatures" Proc. of the IEEE International Symposium on Power Semiconductor Devices and ICs, April 1992, pp.226-228

[6] J.L Hudgins, S.Menhart, W.M Portnoy, V.A Sankaran "Temperature variation effects on the switching characteristics of MOS-Gate devices", Proc. EPE-MAPED Conf. Rec, September 1991, pp.262-266

[7] E. Santi, X. Kang, A. Caiafa, J.L. Hudgins, P.R. Palmer, D.Q. Goodwine, "Temperature Effects on Trench-Gate Punch-Through IGBTs" IEEE Transactions on Industry Applications, vol.40, no2, March-April 2004, pp.472- 482

[8] S. Azzopardi, M. Ishiko, A. Benmansour, R. Roy-Pelat, C. Zardini "A very simple and low cost test circuit for IGBT characterisation under hard- and soft-switching", submitted to IPEC'05, Niigata, Japan, April 4-8.