Study of the CLIC module front-end acquisition and evaluation electronics

J.M. Nappa, J. Tassan, L. Soby, S. Vilalte

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STUDY OF THE CLIC MODULE FRONT-END ACQUISITION AND EVALUATION ELECTRONICS.

Jean-Marc Nappa, Jean Tassan,
Lars Soby (CERN), Sébastien Vilalte.

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Laboratoire d'Annecy le Vieux de Physique des Particules
B.P. 110 74941 ANNECY-LE-VIEUX CEDEX France.
Phone : 33 4 50 09 16 00
Fax : 33 4 50 25 94 95
e-mail : vilalte@lapp.in2p3.fr

Abstract: since 2005, LAPP is involved in developments for a new system of BPMs intensity and deviations read-out for the CTF3 (CLIC Test Facility 3) collaboration.
A first system has been developed from 2005 to 2009.
The aim of this system was to perform the analog to digital conversion of CTF3 inductive pick-ups signals the closer as possible to the beam in order to reduce the cost of the expensive existing acquisition (analog signals cables and digitizers in VME crates). The system included the full chain from pre-amplification to data processing: analog pre-amplification module, analog transmission, digitalization board, network and data processing/display software in CERN framework.
From 2006 to 2009, 50 read-out chains have been installed in several beam lines of the CTF3 accelerator. Unfortunately the unforeseen total radiation doses destroyed some digital parts. Initially the idea was to make evolve this acquisition to a new system suitable for the CLIC module.
By consequence, the decision has been taken to start a new development based on the final CLIC module specifications.
Before a full CLIC module crate study, according to the CLIC collaboration we fixed CLIC module specifications in term of crate architecture. Then, as a first step, we decided to develop an evaluation system for this crate and its associated network.
LAPP is also involved in future module subsystems developments: generic acquisition system and more specifically, beam position monitor subsystem.
This document describes the developments on global architecture, proposed solutions and first developments for evaluation.

Summary:

1- CLIC module specifications and proposal of a future architecture.
   1-1 Acquisition and control channels.
   1-2 Module acquisition architecture.

2- Evaluation boards for CLIC module read-out.
   2-1 Evaluation board.
   2-2 PCIe board.
   2-3 Foreseen tests and preliminary results.

3- Conclusions and perspectives.

1- CLIC module specifications and proposal of a future architecture.

As CLIC tunnels will allow very rare accesses (every ~900m), it became obvious to implement a local acquisition and control system for the module. This choice is mandatory for technical and financial reasons (cabling, signal attenuation…). As the 2m long CLIC module is a construction "brick" of the accelerator, the acquisition and control system should be designed to fit the module's specifications and should be a part of it with a minimum number of connections with the final collection system. One of the main issues is the radiation environment in which the system has to work with high reliability.

Ideally, the back-end connections of the module should be reduced to power supplies and network. Due to losses of low voltages power supplies on long distances, the system should be supplied by a local 230V service line. Concerning the network, a synchronous and rad-hard optical link should be the best choice: the network has to be able to transmit a clock referenced to the machine, needed for some subsystems. An optical link allows the lower attenuation and the lower susceptibility to the harsh environment.

Each module includes 100 to 200 acquisition and control channels for the different subsystems. As each subsystem has different specifications and can evolve, or just can be present or not in the module, the more versatile solution is to implement a generic digital mother board able to receive mezzanines dedicated to subsystems.

1-1 Acquisition and control channels.

The CLIC note *CLIC FRONT END ACQUISITION SYSTEM SPECIFICATION* describes more in detail this part. We can summarize the needed channels for the different subsystems as follows. Full specifications are also now available in the *CLIC CDR* document, *Accelerator control part* [1]:

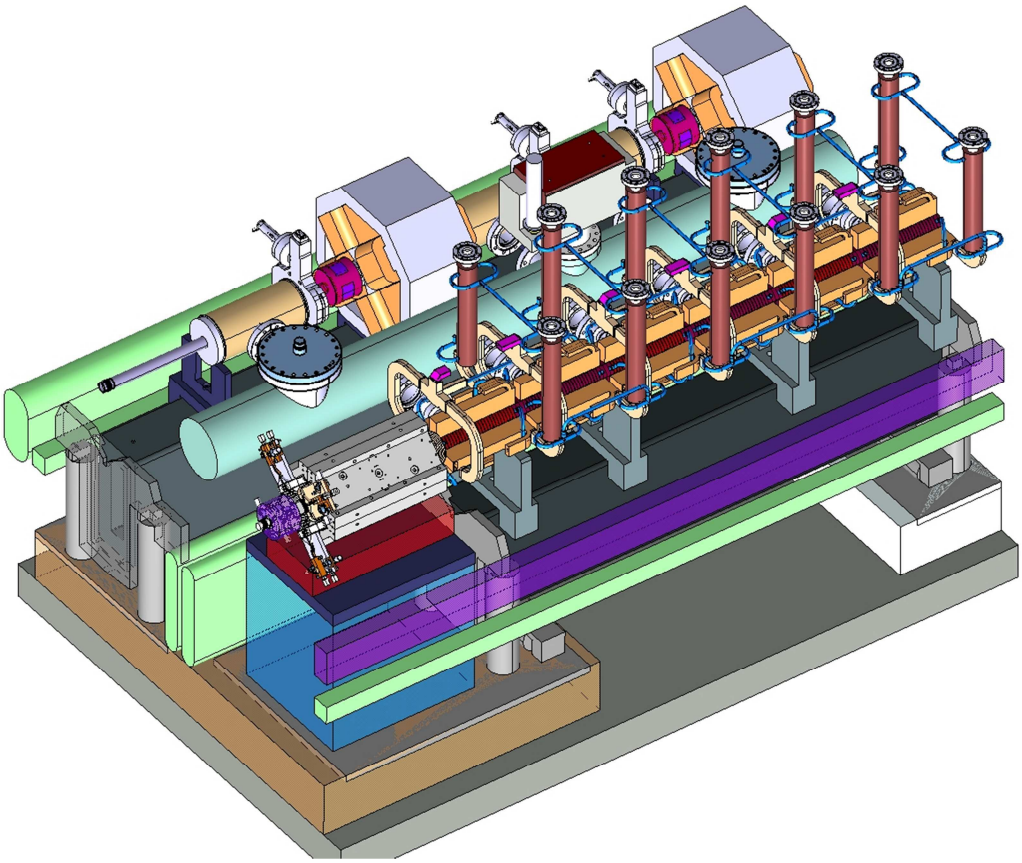
	Analogue				**Digital**	**Update rate**
	Number of signals	Frequency	Sampling frequency	Resolution	Number of signals	
Beam instrumentation	17	50MHz	160MS	16 bits	4 bytes	50Hz
RF instrumentation	8	50MHz	100Ms	8 bits	1 byte	50Hz
Cooling	12	DC	1kS	12 bits	6 bytes	1Hz
Alignment	22	10-100Hz	1kS	24 bits	48 bytes	1Hz
Stabilisation	10	1kHz	10kS	18 bits	-	1kHz
Vacuum	12	10-100Hz	1kS	16 bits	1 byte	1Hz
Power	2	100Hz	1kS	18 bits	-	100Hz

Table 1: Front-end acquisition channels

	Analogue				Digital	Update rate
	Number of signals	Frequency	Sampling frequency	Resolution	Number of signals	
Beam instrumentation	-	-	-	-	4 bytes	50Hz
RF instrumentation	-	-	-	-	3 bits	50Hz
Cooling	-	-	-	-	6 bytes	1Hz
Alignment	-	-	-	-	44 bytes	1Hz
Stabilisation	4	1kHz	10kS	18 bit	-	1kHz
Vacuum	12	10-100Hz	?		1 byte	1Hz
Power	2	100Hz	1kS	18 bit	-	100Hz

Table 2:Front-end control channels

Figure 1: Type 1 CLIC module



1-2 Module acquisition architecture.

The local electronics has to be able to process the analog signals from the different subsystems, to digitize these processed signals, to manage their digital processing, their concentration and to transmit them to the surface/alcove collection system according to a standard protocol.
The number of the motherboards should depend on the number of needed mezzanines. These motherboards should be installed in a standard crate.
The motherboard should also be a form factor standard to allow the use of others standardized boards for sub-systems that cannot be implemented on mezzanines.

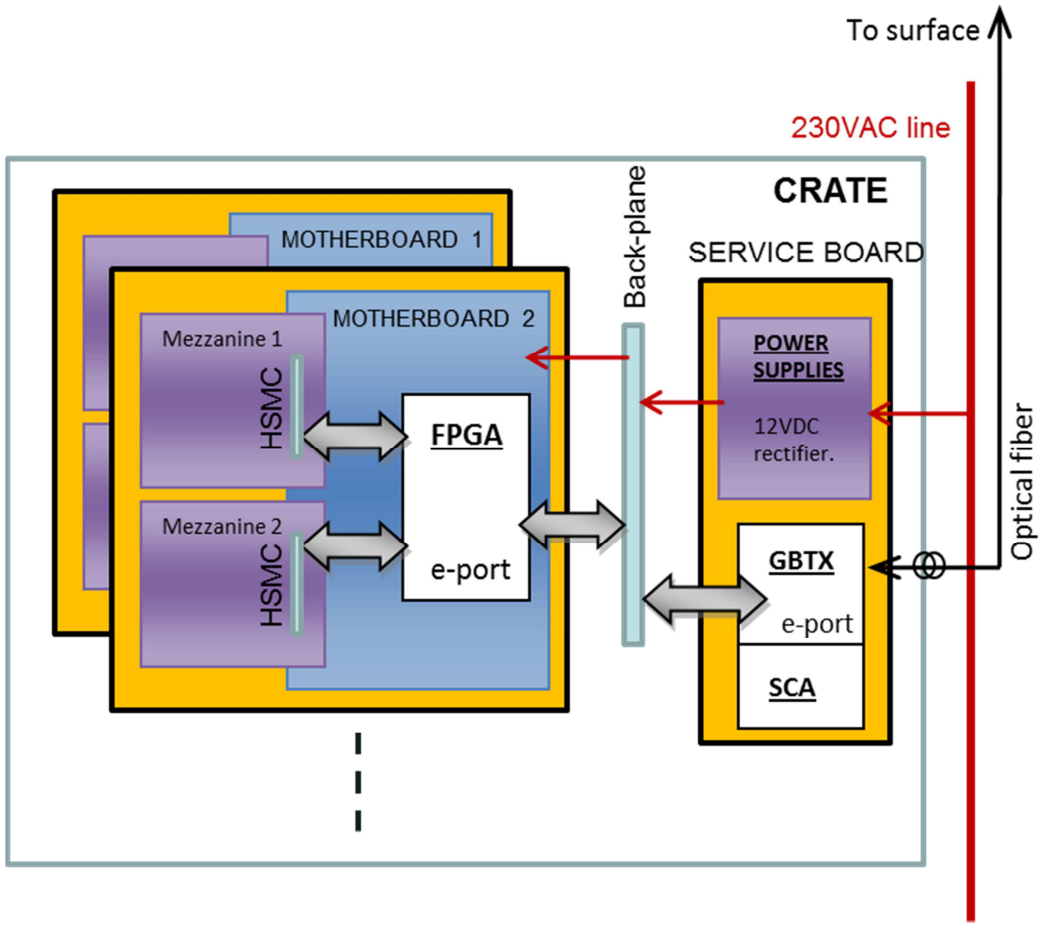
- Network:
  The network has to take in charge the ascending acquired data with a rate that can be important in some configurations (>100Mbps). It has also to take in charge the descending controls and clocks/timings synchronized with the machine.
  In some cases, synchronization is needed to avoid jitter on digitalization.
  In a 2009 study we compared several possible networks as PLC, WiFi, Ethernet… We think that the rad-hard network GBT [2], developed at CERN, is the network that corresponds to the CLIC requirements. GBT is also the future LHC front-end standard network.

  → 4.8Gb/s optical link.
  → up to 40 local chip-to-chip links, ser-des (data concentration).
  → Radhard design (~100Mrad).
  → multiple synchronous clocks management.
  → final version will include slow control features (ADCs, DACs, JTAG, I2C, alarm, monitoring…).

The aim is to have only one optical link between the crate and the collection (surface, alcove…). All the motherboards will be connected to a backplane and use one or several GBT chip to chip links (e-link).
The GBT chip should be implemented on a “Service Board” and this Service Board should perform the different power supplies from the AC 230V line. More than a simple SerDes, the GBT chip will include a lot of functionalities as ADCs and DACs that will allow to control and to monitor the crate. Another advantage is the development of HDL code for FPGAs in the collaboration.
As network, power supplies are very sensitive to radiation. CERN microelectronics group is also developing voltage adjustable rad-hard DC-DC converters (12VDC input).

The choice to use mezzanines for subsystems results in a limited number of links on the connector and so to the choice of high speed links. We chose HSMC connectors that allows up to 10Gb/s serial links. One of the consequences is to choose high speed serial output components for the mezzanine: i.e. ADCs. This choice is coherent because technologies for data transmission are evolving this way.

The central component of the mother board will be a FPGA. In one hand its role is to manage the mezzanines: controls and back-up of the data. In another hand its role is to concentrate the data of the mezzanines and to transmit them to the GBT chip via the backplane. It will recover the descending clocks and controls via GBT.



Crate architecture.

- *Radiation hardness:*

  Simulations from S. Mallows and T. Otto have shown that the total dose, close to the module, can exceed 1 kGy/year. For a 15 years period the total dose should exceed 15kGy. The electronics has to resist to such a dose.
  Rad-hardened components should be chosen each time it is possible and shielding is also possible.
  Some as GBT or power parts like DC-DC converters are rad-hard; others as analog parts or ADCs are not qualified but known for their hardness. As we could observe in CTF3, digital parts are the most susceptible, particularly memory points.
  Unfortunately, FPGAs are more and more rare in rad-hardened version.

Industrial standard technologies less to 90nm are more or less intrinsically total dose resistant due to annealing effects of leakage currents, at the foreseen CLIC's levels.
Latch-up (SEL) are limited by the reduced size of the pnpn thyristor structure. Currently technology is 40nm, next 28nm. Single events errors (SEE) can be prevented by TMR (triple modular redundancy).
Finally a hardcopy version, a kind of ASIC, should avoid memory points susceptibility to neutrons. In this case, the drawback is the impossibility to change the code but the FPGA role should be only to manage the sub-systems and to transmit raw data.
Whatever the choices, final qualifications will be mandatory to validate choices. Current studies on industrial FPGA are promising and we based our choices on specific studies [3].

- *Power consumption:*

  An important issue is the available power consumption. The total module budget is about 150W/m. The estimated budget for the acquisition crate is about 30-50W. Particular effort has to be made on power consumption reduction. Maximum simplification of the local electronics is a key and power cycling is to be studied (switching off the supplies when possible).

- *Mezzanines for sub-systems:*

  The use of mezzanines allows the implementation of a generic motherboard with no specific application. Mezzanines will be designed with state of the art parts and will be able to involve and so to be upgraded if needed. This choice has for consequence constraints on number of linked signals because of connectors. For sub-systems needing high speed acquisition, typically BPMs, the choice of parallel outputs should limit data rates but is incompatible with mezzanines architecture because of the large number of transmission pairs. The choice is oriented to serial output components (i.e. ADCs) but it means higher rates in data transmissions. The current trend is to use serial outputs because of involvements on high speed transmissions.
  These links are LVDS, up to 1.2Gb/s rates, and the next step should be transceivers links up to 6Gb/s. To be able to use the motherboards with next technologies, we decided to implement HSMC high speed standard for mezzanine connectors. This connector has been designed especially for ALTERA high speed FPGAs. It is able to transmit data with rates up to 6Gb/s. First tests showed rates up to 8.5Gb/s with no data errors.

- *Data collection:* PCIe board.

  The crate data will be sent to the collection system (surface, alcove…) via an optical link. First discussions and propositions mentioned the possibility to collect and concentrate data inside the tunnel using switches (according to upstream possible data rate). The aim was to limit the number of parallel fibers. This “tree” solution has been abandoned: a loss of one link could produce the loss of a large sector; it should also be more expensive and less reliable.
  A simpler and more reliable solution is to implement a point-to-point network. As the used network will be standard, several final solutions to concentrate the links are possible.
  In order to recover our prototype board data and in order to evaluate the system, we developed a PCIeX8 collection board. This board will not be necessarily the final collection board, the aim is to evaluate its performances. PCIe will be the next bus standard and its advantage is to reach high speed transfers on standard platforms as PCs.
  This board allows to recover four 4,8Gb/s GBT optical links so four GBT links from four CLIC crates.
  The PCIe board will also be able to recover external machine clocks and timings and transmit them synchronously via GBT to the crates.

2- Evaluation boards for CLIC module read-out.

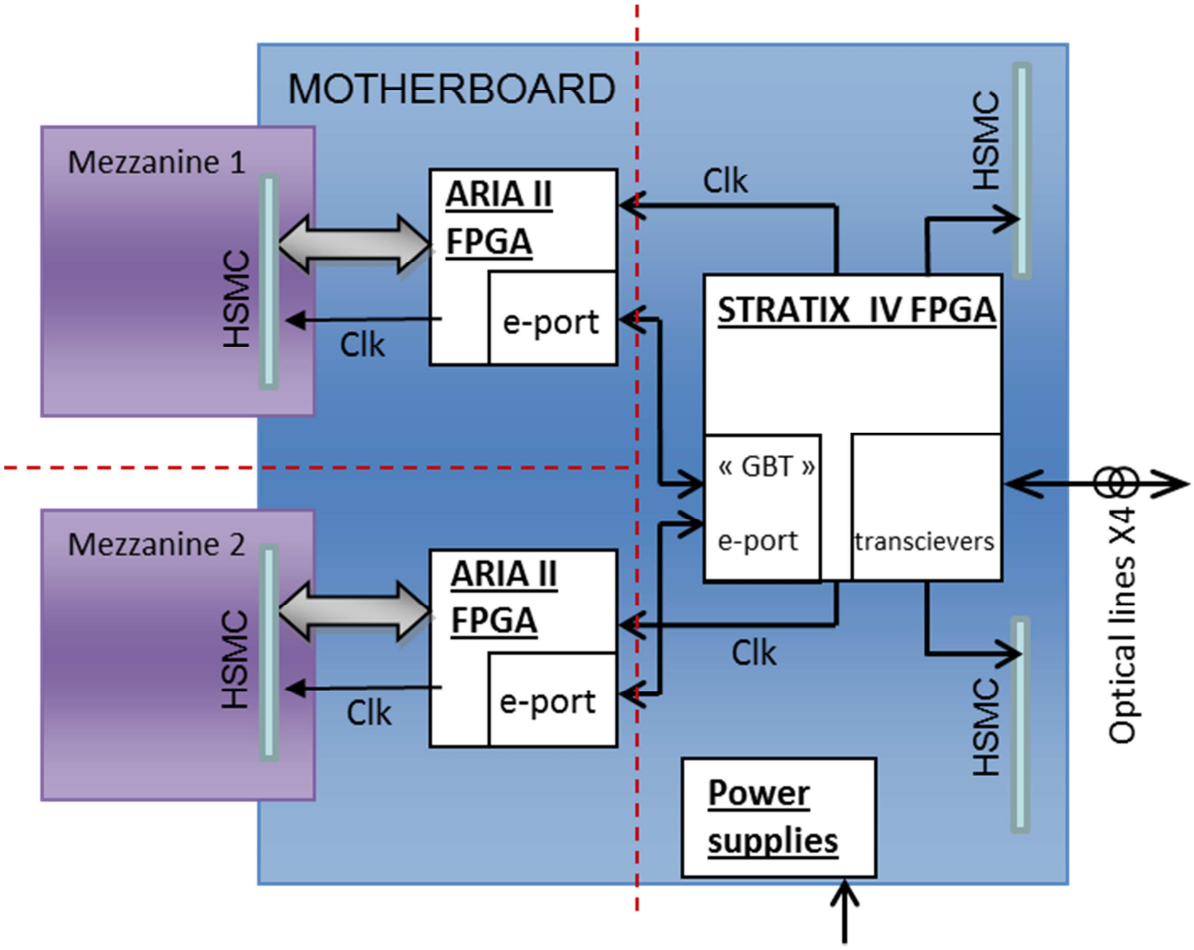
Designing at first a complete architecture is a bit early because a lot of technical solutions have to be validated. A lot of inputs from subsystems are also missing. Important choices on form factors or systems have still to be discussed with all the actors in the collaboration, especially CERN Control group. The development began fall 2009 and several specifications were not fixed.
So we decided to implement at first an evaluation board with two aims:

- Emulation of an entire crate with GBT protocol: it will allow to test the GBT with tools provided by the GBT collaboration. All GBT features can be coded in FPGAs. It will also allow to test the acquisition architecture without producing several motherboards, crate, and so limit costs.
- Second, in the future this board could be used to develop and test mezzanines.

In parallel, we developed a PCIe board to evaluate the performances of this possible data collection.

2-1 evaluation board.

The evaluation board emulates a full crate with motherboards, service board and mezzanines. We implemented two independent FPGAs corresponding to two emulated motherboards in the module crate.
GBT can concentrate up to 40 local links (80Mb/s each), called e-link. These links can be grouped to increase the rate. We implement a group of links to test transmissions and particularly synchronizations for each of the two emulated motherboards FPGAs. A third FPGA will emulate the GBT and will allow a lot of developments/tests. This Third FPGA is able to emulate 4 GBT links and so allows the emulation of 4 crates data transmissions in parallel.



Emulation board architecture.

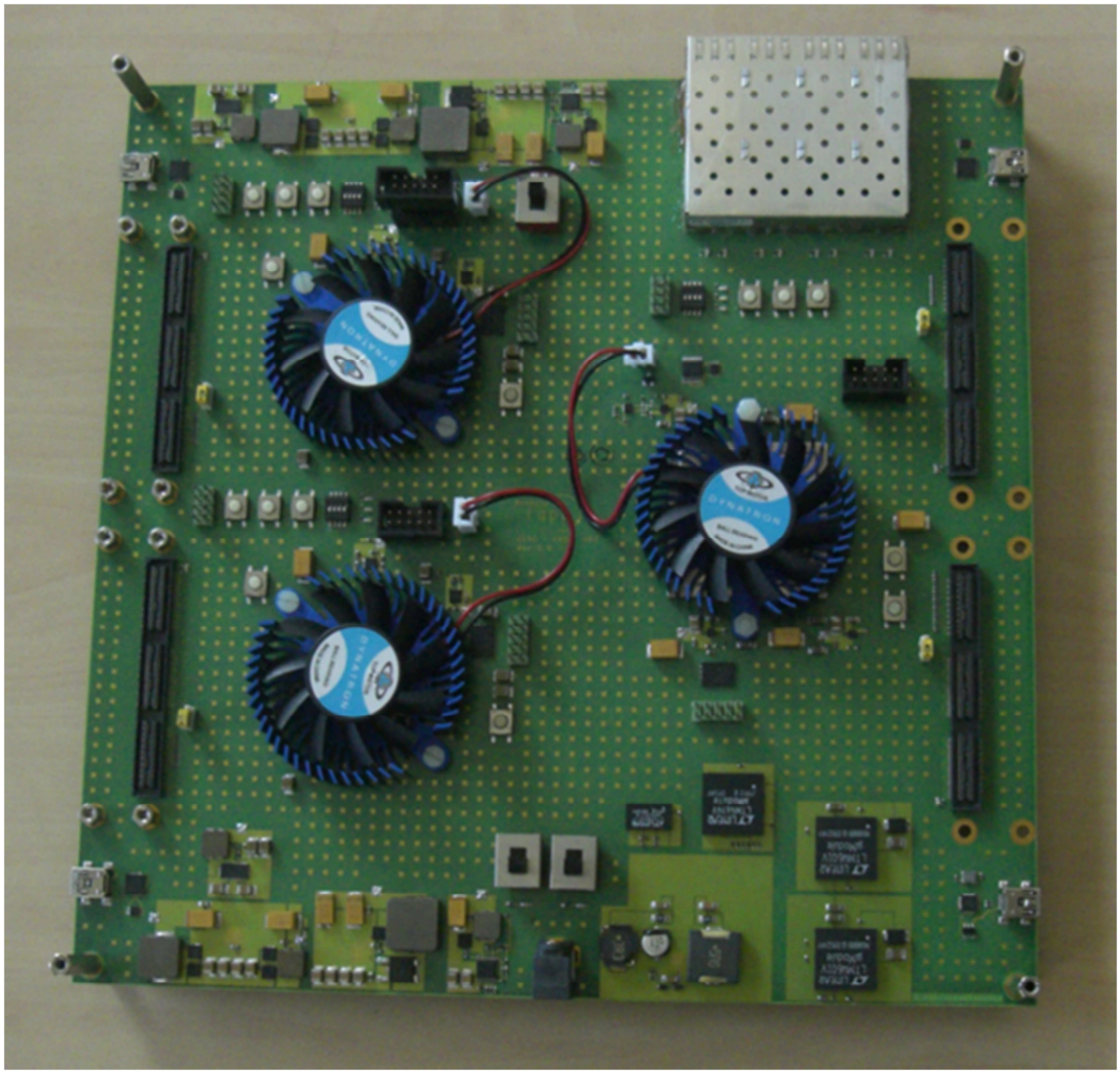
ARRIA II FPGAs and their corresponding HSMC connectors emulate the motherboards. STRATIX IV emulates the 4 parallel GBT links, so 4 crates.
As the HSMC connector used for mezzanines is a standard high speed connector, we implemented two more connectors linked with the StratixIV FPGA. They can be used for mezzanines tests and especially in the future to test the real GBT chip implemented on a dedicated mezzanine.

HSMC connector features:

- 8 transceivers links up to 8,5Gbps.
- 17 LVDS Tx, 17 LVDS Rx 1,2GBps.
- 3 reserved links for clocks.

The evaluation board has been produced beginning 2011:

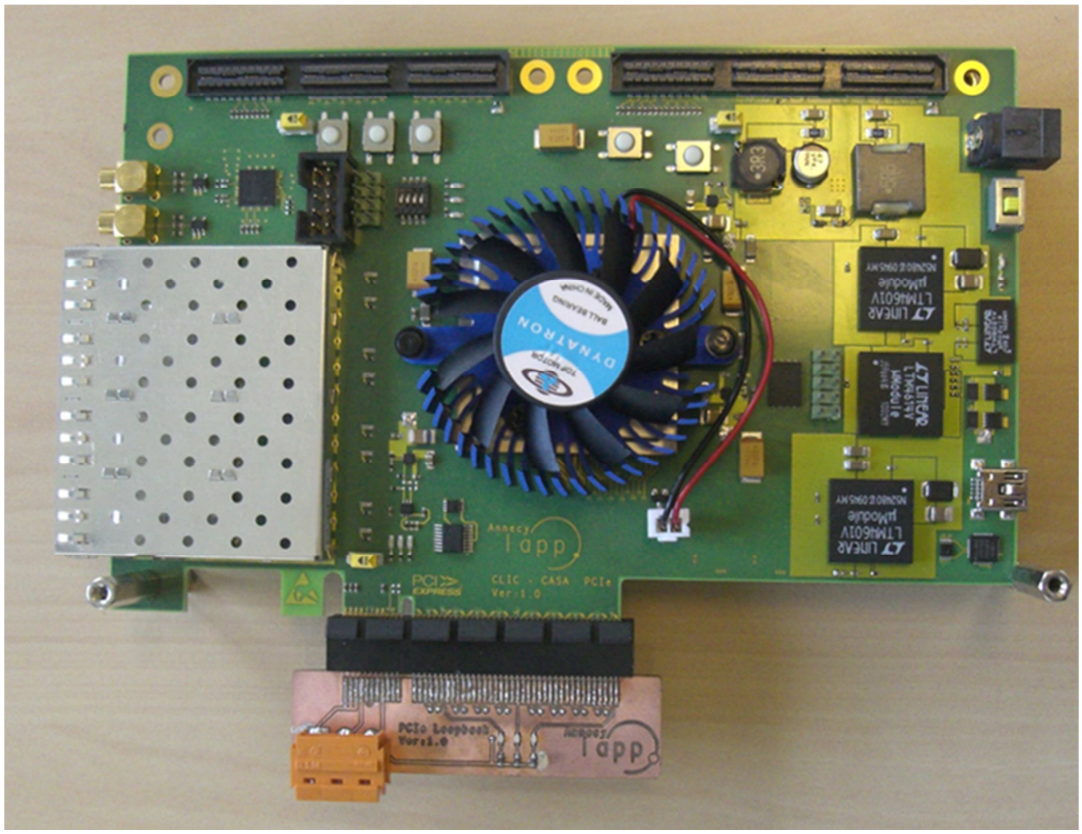
240x240mm Hitachi FX-II, 60µm class, 18 layers, ~2000 components
~900 differential pairs 1,2Gb/s, 56 transceiver pairs 8,5Gbps
4 SFP 8,5Gb/s, 3 FPGAs 1700 pins, 4 USB links, 4 mezzanines



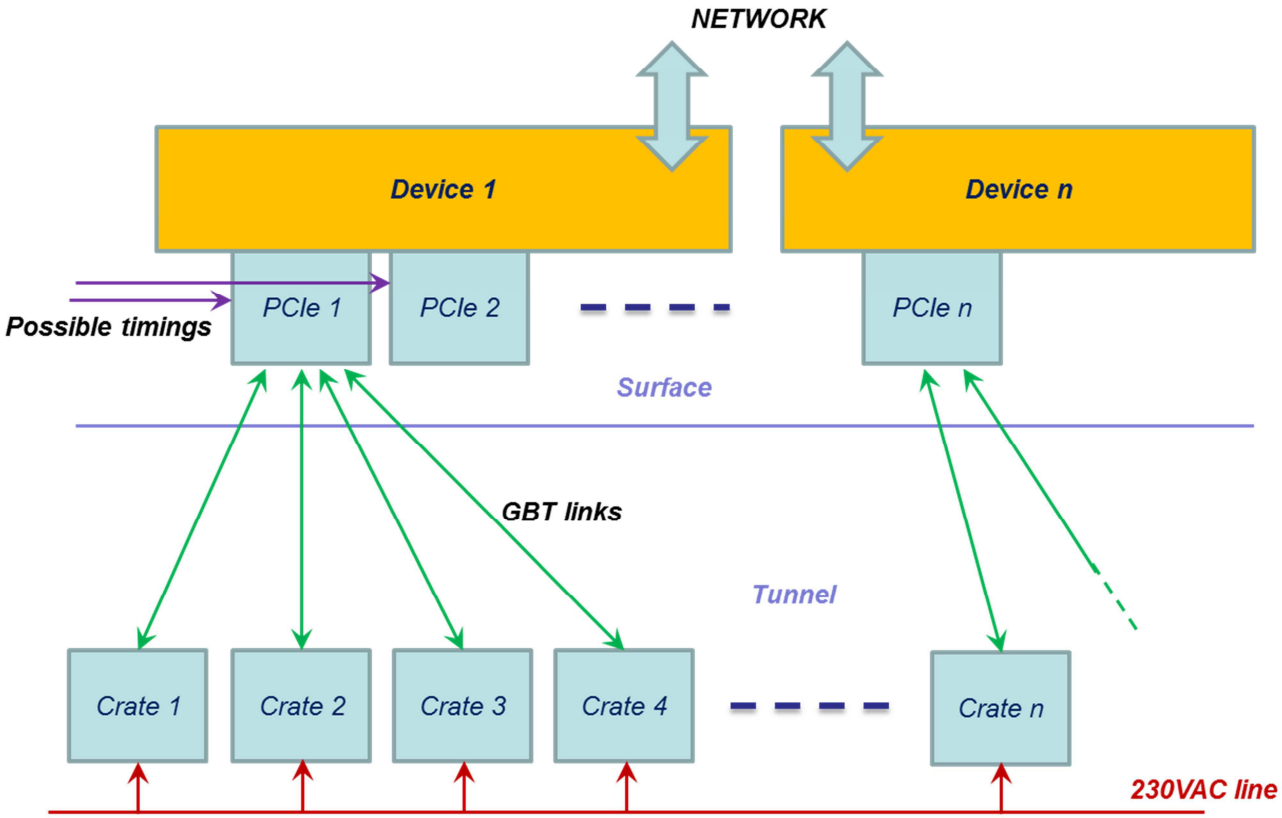
2-2 PCIe board.

The PCIe data collection board has been produced on spring 2011:

- 4 SFP+ optical links so recovers 4 crates: actual GBT rate is 4,8Gb/s.
- X8 Gen2 for high speed standard interface. The advantage to use PCIe links is to transfer the data independently of the CPU in a Direct Memory Access mode.
4 PCIe Gen2 lines (5Gb/s) should be enough to transfer the data from the 4 SFP links but the implementation of 8 lines allows to use older or cheaper chipsets with PCIe Gen1 rates (2,5Gb/s). 8 lines will also allow to use faster links or next versions of GBT with rates of 9Gb/s.
- 2 MCX inputs for external timings.
- 2 HSMC connectors: allows the connection of mezzanines locally (i.e. generic acquisition, tests…).
- 1 USB link for tests and stand-alone use.



Possible global architecture for the CLIC section:



Server CPU mother-boards are currently available with 8 PCIeX8 or 16 PCIeX4 sockets (total of 64 lines). In the future, we could imagine to plug up to 16 PCIeX4 and so to collect the data from up to 64 crates. That could reduce the number of servers to 7 for a whole ~900m long CLIC section.

2-3 Foreseen tests and preliminary results.

- Functionality tests: test of all the links with user's protocol.
- Tests on local evaluation board network, synchronizations and timings: GBT should be a future standard in the LHC for the synchronous applications with large data transfers. Although this component is not available in its final version, the code developed by the collaboration allows to emulate the GBT protocol and to evaluate it for our application.
  Even only one FPGA is enough to test the ADCs and the code of a future acquisition board, we implement two ARRIA II FPGAs with two different acquisition chains and a central Stratix IV. It will allow to test the *e-link* interfacing local link of the GBT and its protocol and also the timing distribution from PCIe board timings inputs to mezzanines components as ADCs.

- Test on the global network: full chain from PCIe board to mezzanine plugged on the evaluation board. Test of the data transmission, data rates. Tests of the timings transmission, synchronisations.

- Tests on FPGA code: the evaluation board will allow to test the specific code for the mezzanines architecture, the GBT interfacing code and specific technics as TMR for radiation issues.

- Thanks to mezzanines, independent power supplies will be able to be connected to test future solutions for the service board and their compatibility with the acquisition (power, PSRR, noise…).

- Tests on radiations: the architecture will allow to deport the mezzanines in a radiation area for radiation qualification. Different parts should be qualified: mezzanines for sub-systems, mezzanines designed especially for specific tests (power supplies, FPGAs…).

  This tests list is not exhaustive.

Preliminary results:

- Functionality tests:

These hardware tests are the first steps to verify that the cabling and all the links are working as foreseen. Then applications tests will be done.
All the links have been controlled with BER pseudo-random test patterns (bit error rate). Tests have been performed on the evaluation board: links between the three FPGAs, links between FPGAs and HSMC connectors.
Tests have also been performed via the optical link between the evaluation board and PCIe board.
Tests on several hours have shown no error on transmission and no cross-talk error.
Rates of 1,2GB/s have been verified on LVDS pairs, up to 11GB/s on high speed HSMC transceiver links, all links transmitting data at the same time. Rates of 9GB/s have been checked on the optical link with no errors.
HSMC interface test has been performed using multiple high-speed data streams through a HSMC loop-back connector.

- Tests on synchronizations and timing:

Some subsystems as beam position need an acquisition synchronized with the machine (i.e. 96MHz for CTF3). This timing can be transmitted on the network using a carrier frequency which is a multiple of the reference frequency.
That means optical carrier frequency must be controlled accurately to bring out the clock in the crate. We tested the possibility to impose a frequency to the FPGAs and to the optical transceivers. Using the PCIe board and timing boards developed for another application, but with same architecture and components than the evaluation board, we verified the synchronisation: FPGAs and transceivers allow to impose the reconstructed frequency to PLLs. Since the PLL is locked, it ensures that the clock reconstructed is synchronous. The important issue in timing distribution is the jitter: it is the limiting factor for the acquisition dynamic range. As the clock is reconstructed thanks to the FPGA's PLL, jitters values were in compliance with the announced PLL jitters values. In sub-systems applications, as BPM acquisition, we will use jitter cleaners that reduce the clock jitter to about 150fs.
We performed these tests with two chained reception boards, so it proves that, even if intermediate boards are not foreseen, it is possible to repeat this reference frequency in a chained architecture.
These results proved that it was possible to implement a single optical link between local crate and collection.
The last foreseen test is to check the synchronisation/jitters with the full chain and ADC.

3- Conclusions and perspectives.

Even if all the tests have not been performed yet, first results are very promising. Tests have shown the large future possibilities of the architecture and its ability to adapt to future sub-system developments thanks to high speed links.
Next tests and developments will allow us to become familiar with GBT network. In parallel of these tests, we are defining the future crate architecture and mechanical form factors with the CERN Control group. After evaluations and discussions, we plan to produce prototypes of the full system: mother-board, service board and mechanical crate. This full system could be available beginning 2013. The LAPP should be committed in CLIC module crate R&D for the next TDR period.
As we are also involved in stripline BPM read-out and acquisition, we foresee to test the mezzanine in CTF3 with the evaluation board and a fiber link end 2012 in collaboration with the CERN BI-PI group.

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