Advanced ESD power clamp design for SOI FinFET CMOS technology

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***Abstract*—Two novel ESD power clamp design techniques for SOI CMOS technology is reported. First, a layout improvement technique is discussed for series gated diodes, which reduces the required area for a given ESD robustness and at the same time reduces the on-resistance of the clamp. Secondly, circuit design techniques are used to convert a standard RC-triggered active ESD clamp into a bi-directional design, thereby alleviating the need for a separate reverse protection diode.**

***Index Terms*—ElectroStatic Discharge (ESD), FinFET, Silicon On Insulator (SOI)**

I. Introduction

ELECTROSTATIC DISCHARGE (ESD) protection devices typically consume a large portion of the Integrated Circuit (IC) silicon area. Without simultaneous reduction in the required ESD robustness, as CMOS technology scaling continues, the ratio of silicon area occupied by ESD protection devices to the rest of the circuit become even larger [1]. Silicon On Insulator CMOS technologies offer significant performance advantages over bulk CMOS. However, ESD performance of SOI technologies is much inferior than bulk CMOS [2] so the ESD protection device area becomes even more of a concern. Therefore, reduction of ESD protection elements silicon area, especially for the most advanced CMOS technologies, is very critical from the cost economic point of view.

Clamping the voltage across different power rails and domains during ESD stress to the lowest possible amplitude is by far the most important step to protect the core circuitry. This paper discusses two novel approaches for ESD power clamp design in Silicon On Insulator (SOI) CMOS technologies, which result in reduced area consumption with equal or enhanced ESD robustness. These novel concepts are implemented in a SOI FinFET technology, where the ESD area efficiency is lower than planar SOI technologies [2]. A design methodology for area minimization of ESD protection devices in FinFET technology was previously reported [3], which was based on optimization of the standard device geometrical parameters. This work focuses and presents additional area optimization techniques and silicon validation of the same.

The features of the SOI FinFET technology used for the work are described in Section II. A novel layout technique for optimization of stacked-diodes as power clamp is proposed in section III. Section IV discusses a circuit technique to create a bi-directional power clamp, thereby avoiding the need for a separate reverse protection diode.

II. SOI FinFET Technology

Sub 45-nm FinFET devices are processed at imec on SOI-wafers with 65 nm fin height H_{fin} and 145 nm Buried Oxide (BOX) thickness T_{BOX}. A 2 nm HfSiON high-k gate dielectric and TiN metal gate are used on top of an interfacial 1 nm SiO_2 layer [4]. The fin width W_{fin}, the fin number N and the gate length L_g are layout parameters and can be set to 20 nm, 400, and 45 nm minimum, respectively. Fin-to-fin spacing S is fixed to 170 nm. Figure 1 shows a horizontal layout (top) and vertical cross-section (bottom) of the FinFET device, indicating the different geometrical parameters.

III. Series Diodes as Power Clamp

Often, stacked-diodes are used as ESD power clamp in advanced CMOS technologies due to the reduced power supply voltage. The number of series diodes depends on a trade-off between leakage current and clamping voltage.

In conventional bulk CMOS technologies, placing diodes in series requires the use of separate n-wells for each diode. Therefore, the distance between two diodes is determined by minimum n-well to n-well spacing. However, in SOI technology, a single n-well can be drawn as the Shallow Trench Isolation (STI) cuts down till the BOX, thereby isolating each diode. This reduces the amount of required space. In FinFET SOI technology, gated diodes are commonly used and the same layout technique can be used and no n-well is even present due to the usage of undoped body, see Figure 2 (top). The anode is connected through the metal1 layer (M1)

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and several contacts (CT) down to the P^+ active of the first diode. The cathode of the first diode is connected by CT-M1-CT to the anode of the second and so on.

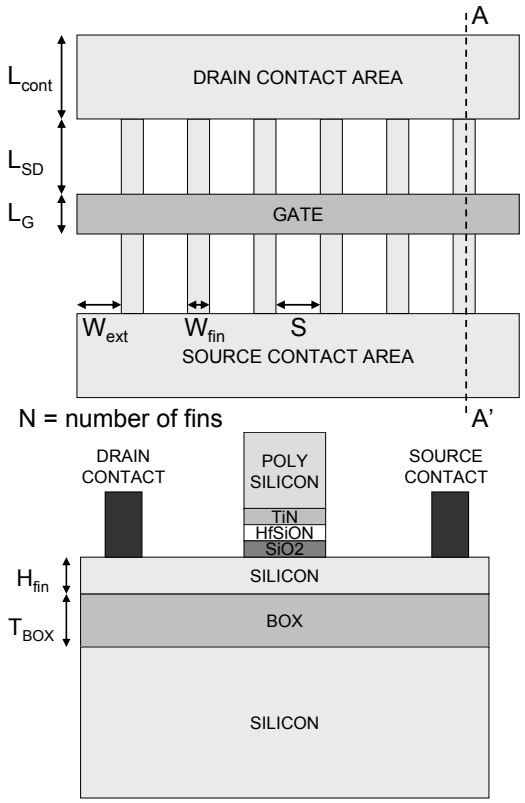

Figure 1: Horizontal (top) and vertical along cut-line A-A' (bottom) layout view of a FinFET device indicating the different geometrical parameters.

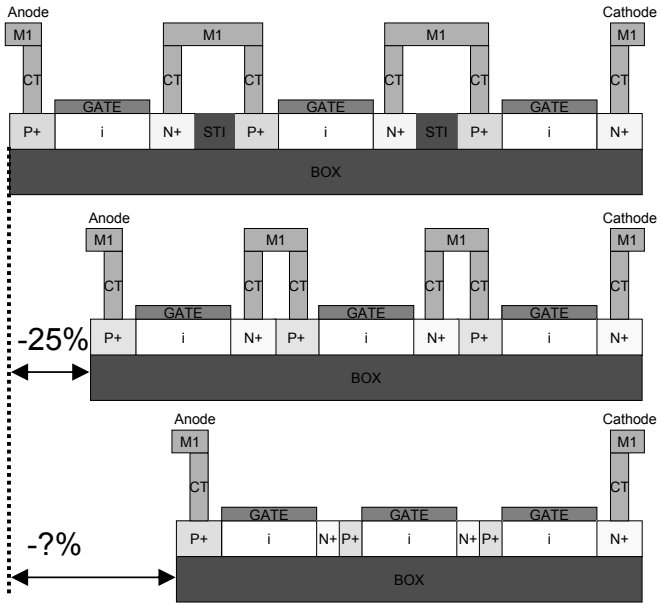

Figure 2: Cross-section of three gated diodes placed in series. The top figure shows separate devices, while in the middle the intermediate anodes and cathodes are merged into a single active area and are shorted by silicidation and the backend. By relying solely on the silicidation connection, the intermediate CTs and M1 can be removed resulting in a further layout reduction (bottom).

Another technique which further reduces the required area is by merging the cathode active region with the anode active region of the next diode, see Figure 2 (middle). The STI isolation is omitted. A good connection is formed through the silicidation process and the backend CT-M1-CT and with this approach, for this technology, 25 % reduction in area is achieved. Since the silicidation shorts the anode and cathode regions, further layout reduction is possible by omitting the intermediate CTs and M1 as in Figure 2 (bottom). Since the anode and cathode regions do not need to accommodate any contacts, they can be made significantly smaller. However, omitting the intermediate CTs and M1 might have a drastic influence on the failure current It_2 as they are responsible for part of the cooling of the device during ESD stress. More investigation is required to determine the optimal layout strategy based on the layout technique as seen in Figure 2 (bottom) and is not addressed in this paper.

The ESD performance of the first two layout techniques in Figure 2 (top and middle) is compared in Figure 3. Transmission Lin Pulse (TLP) measurements with 100 ns pulse width and 2 ns rise time were performed on three diodes in series. Each diode has 80 nm L_g and consists of 400 fins of 20 nm W_{fin}. Selective Epitaxial Growth (SEG) [5] was used to reduce the overall diode resistance. The impact of SEG has been already discussed in [2]. When omitting the STI isolation according to Figure 2 (middle), on-resistance decreases by 16% for almost the same failure current It_2. This reduced resistance is due to the reduced interconnect resistance, caused by the parallel connection of the silicide and the CT-M1-CT chain. Thus, Ron decreases by 16% with a 25 % area reduction for same It2.

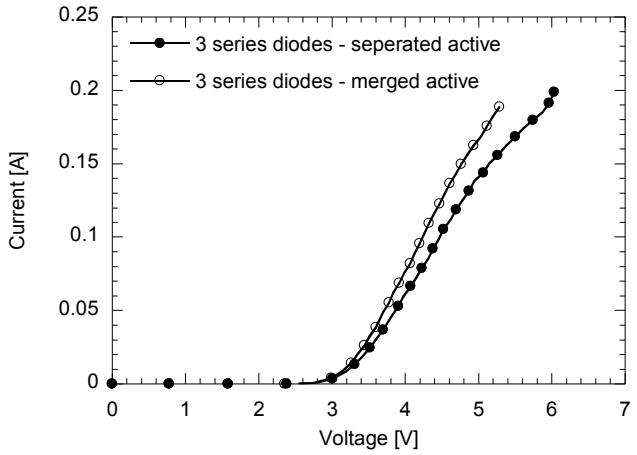

Figure 3: TLP-IV measurements for three diodes in series using different layout configurations. The diodes have 80 nm L_g and consist of 400 fins of 20 nm W_{fin}.

IV. Bidirectional Power Clamp

Typical RC-triggered power clamp [6] is shown in Figure 4. During positive ESD stress between V_{DD} and V_{SS}, the RC-circuit detects the transient ESD signal and turns on the gate of the BigNFET transistor via an inverter chain with feedback. Hence, the BigNFET discharges the ESD current while operating in active MOS mode. For negative stress between V_{DD} and V_{SS}, the current is flowing through the diode D_1

placed parallel to the BigNFET. The addition of the dedicated diode for the negative stress polarity requires additional silicon area.

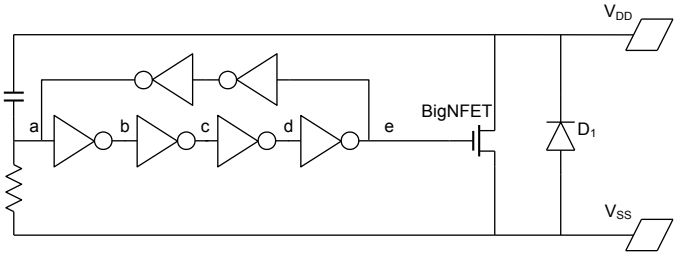

Figure 4: Schematic of RC-triggered power clamp. The addition of inverters and feedback relaxes the constraint on the RC-network.

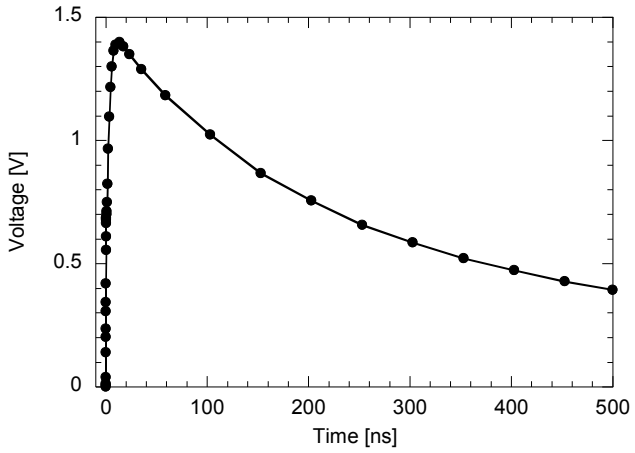

Figure 5: 1 kV HBM simulations of the circuit in Figure 4. HBM stress was applied positive between V_{DD} and V_{SS}.

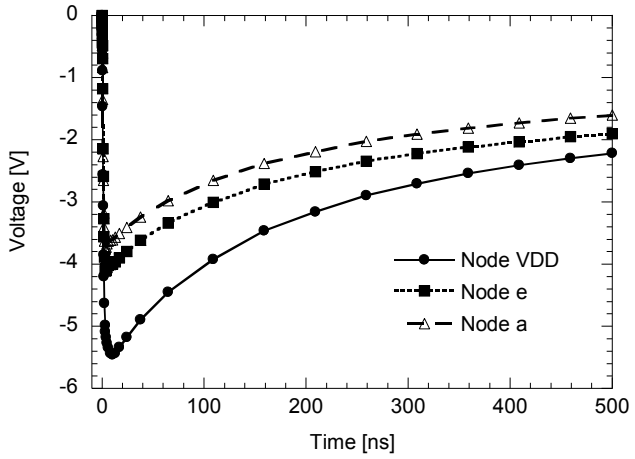

Figure 6: 1 kV HBM simulations of the circuit in Figure 4 without reverse diode D_1. HBM stress was applied negative between V_{DD} and V_{SS}.

However, since a non-tied-body SOI transistor has no body contact, it is a fully symmetric device (meaning that source and drain can be interchanged). We can exploit this symmetry by making the BigNFET operate in active mode during both positive and negative stress polarities, thereby avoiding the need for an additional diode, D1 in Figure 4. 1 kV HBM simulations have been performed on the circuit shown in Figure 4 for both polarities. In Figure 5, the active clamp is operating as expected, clamping the voltage to 1.4 V. However, during negative stress events, simulated in absence of diode D_1, the inverters are not inverting anymore, but are acting as buffers, meaning that their output follows their input, but the signal is degraded. As V_{DD} goes negative, this signal is coupled onto node 'a', and all other nodes ('b'-'e') follow this signal. As a result, the gate voltage V_{GS} of the BigNFET is zero, and hence the BigNFET remains off. Simulations show in Figure 6 that since node 'e' does not follow node 'a' exactly, at some moment the BigNFET will switch on, but at too high voltage (-5.5 V).

Node 'e' should not be allowed to go negative, to be able to open the BigNFET. Therefore, an additional PMOS is added (M_1), Figure 7, to pull node 'e' to V_{SS} during negative ESD stress. Since node 'e' is now controlled to be low during negative ESD stress, the BigNFET turns on at a much lower voltage. The minimum voltage of node V_{DD} is -2.1 V according to the simulations in Figure 8. As can be seen from Figure 7, node 'e' is not well controlled. Since the PMOS M_1 is not in an inverter configuration, the output voltage at node e, depends on the load of the PMOS. The load consists of the output of the inverter between node 'd' and 'e'. The voltage at node 'd' is also seen in Figure 8, and in this configuration, the PMOS of that inverter is in a conducting mode, limiting the pull-down of node 'e'.

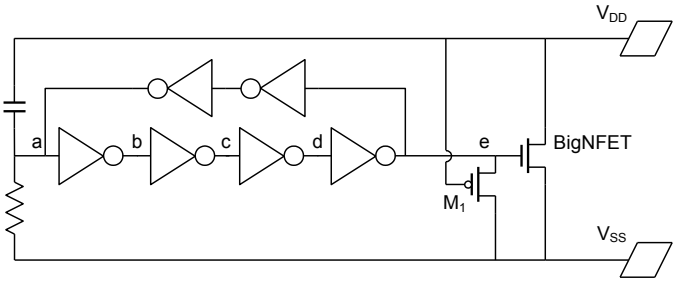

Figure 7: Schematic of symmetric RC-triggered FinFET power clamp. The addition of M_1 enables the BigNFET to operate in active mode also during negative stress events.

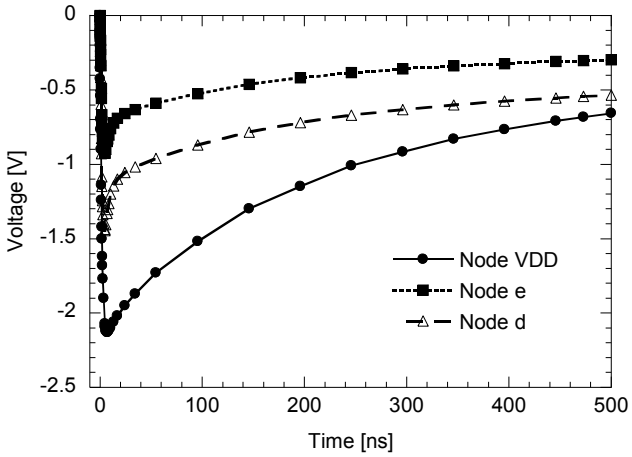

Figure 8: 1 kV HBM simulations of the circuit in Figure 7. HBM stress was applied negative between V_{DD} and V_{SS}.

This solution can further be improved by controlling node 'd' as well during negative ESD stress, trying to keep the output impedance of the inverter between node 'd' and 'e' as high as possible. Ideally, node 'd' should be pulled to V_{SS}. To achieve this, additionally the NMOS transistor M_2 is placed as

shown in Figure 9.

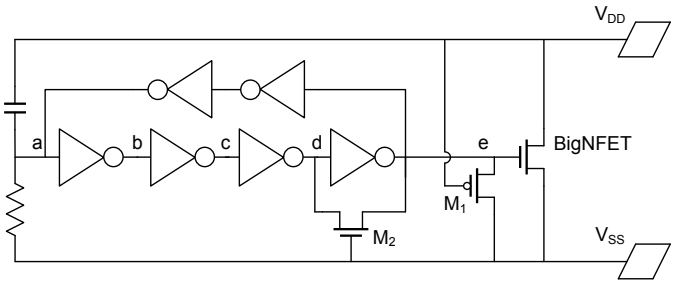

Figure 9: Schematic of symmetric RC-triggered FinFET power clamp based on Figure 7. The addition of M_2 further improves the turn-on voltage during negative stress events.

During negative ESD stress, M_2 pulls node 'd' as low as possible. This voltage is limited by the threshold voltage V_T of M_2 and therefore, node 'd' is not fully zero. As a result, the output impedance of the inverter between node 'd' and 'e' is not infinite, and hence node 'e' cannot be pulled fully to zero as well. However, the minimum voltage at the V_{DD} is now limited to -1.6 V as seen in Figure 10. This (absolute) value is slightly higher than the maximum voltage during positive stress (1.4 V) due to the reasons explained above.

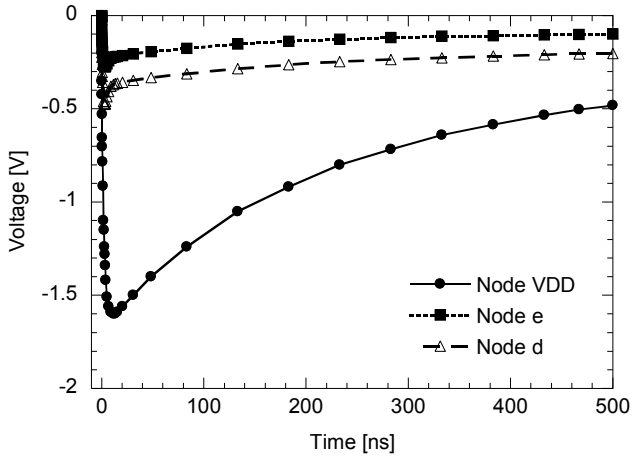

Figure 10: 1 kV HBM simulations of the circuit in Figure 9. HBM stress was applied negative between V_{DD} and V_{SS}.

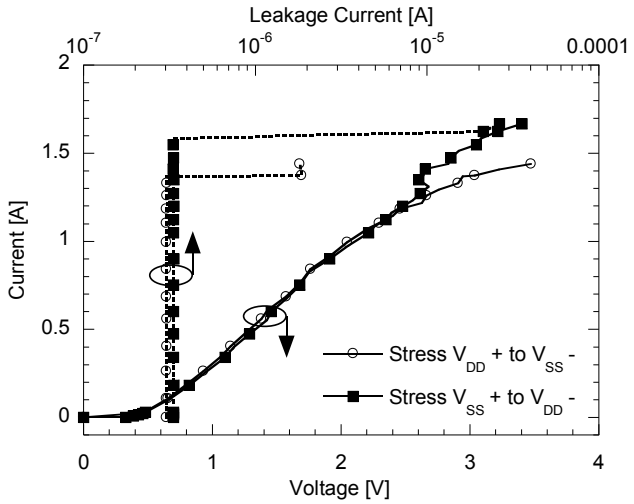

Figure 11: TLP measurements of the bidirectional FinFET power clamp, using a PMOS as BigFET.

TLP measurements were performed on a bidirectional power clamp where a PMOS was used as BigFET transistor. The operation principle of such PMOS implementation is analog to the NMOS version. The TLP results are shown in Figure 11, and almost no difference is seen in the I-V curves proving the concept of the fully bidirectional power clamp. During negative stress events, It_2 is ≈ 10 % higher than during positive stress which can be attributed to an additional current path through transistor M_1 in combination with the last driver stage.

V. Conclusions

In this paper, two novel techniques have been demonstrated to reduce the area of ESD power clamps in SOI CMOS technology. Even though a SOI FinFET technology was used, the concepts are valid for general SOI ESD protection design.

First, a layout technique was demonstrated to reduce the area consumption of a series diode stack, thereby reducing the on-resistance as well. A possible layout technique for further area reduction was proposed.

Secondly, a circuit technique was employed to convert an RC-triggered power clamp into a bi-directional protection element. As such, no additional area was needed for the reverse protection diode.

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