Thermal Stability of Silicon Carbide Power JFETs

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***Abstract*—Silicon carbide JFETs are attractive devices, but they might suffer from thermal instability. An analysis shows that two mechanisms could lead to their failure: the loss of gate control, which can easily be avoided, and a thermal runaway caused by the conduction losses. Destructive experimental tests performed on a dedicated system show that this latter mechanism is more severe than initially expected. A low thermal resistance and gate driver equipped with protections systems are thus required to ensure safe operation of the SiC JFETs.**

***Index Terms*—SiC, JFET, thermal runaway**

NOMENCLATURE

μ_n	Electron mobility ($cm^2.V^{-1}.s^{-1}$)
E_G	Energy band gap (eV)
I_D	Drain current (A)
k	Boltzmann's constant ($1.38.10^{-23}J.K^{-1}$)
$Kpsat$	JFET "transconductance" ($A.V^{-2}$)
N_c	Density of states in the conduction band (cm^{-3})
N_D	Doping atoms density in the drift layer (cm^{-3})
n_i	Intrinsic carrier concentration (cm^{-3})
N_v	Density of states in the valence band (cm^{-3})
P	Electrical power supplied to the device (W)
Q	Heat flux removed from the device (W)
q	Electron charge ($1.6.10^{-19}C$)
R_{300}	Value of $R_{DS_{on}}$ at 300 K (Ω)
$R_{DS_{on}}$	On-state drain-to-source resistance (Ω)
$R_{on,sp}$	Ideal specific resistance of a vertical FET ($\Omega.cm^2$)
R_{th}	Thermal resistance, junction to ambient ($K.W^{-1}$)
T	Temperature (K)
T_A	Ambient temperature (K)
T_J	Junction temperature (K)
U	Internal energy (J)
V_{DS}	Drain-to-source voltage (V)
V_{GS}	Gate-to-source voltage (V)
V_{pt}	Gate-to-source punch-through voltage (at a given current) (V)
V_{T0}	Gate-to-source threshold voltage (V)
W	Thickness of the drift layer (cm)

I. INTRODUCTION

COMPARED to silicon, devices made using wide bandgap materials can operate at a higher junction temperature. In particular, with a 3.26 eV bandgap and a relatively mature manufacturing technology, 4H silicon carbide (SiC) is a very attractive material for high (>200 °C) junction temperature operation [1]. SiC power devices working at up to 400 °C ambient were demonstrated in [2]. Many converters were built using SiC devices (mainly unipolar components) and confirm their successful operation at ambient temperatures exceeding 200 °C [3].

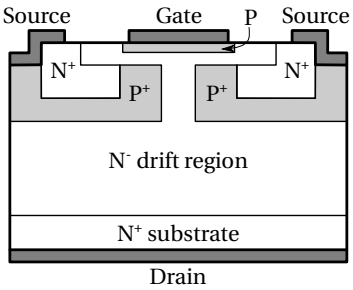


Fig. 1. Internal structure of the SiC JFET from SiCED [10]. This transistor is used in the present study.

An other approach is to take advantage of the high junction temperature capability of the SiC devices to reduce their associated cooling system: by allowing a higher temperature difference between the power devices and their environment, a less efficient cooling system can be used, resulting in lower costs and smaller thermal management systems. An example is given in [4], where a converter operates at 150 °C ambient temperature. SiC devices allowed a 100 °C temperature rise (to reach junction temeperature of 250 °C), enabling the designers to use a passive cooling system.

However, this "reduced cooling system" approach is discussed in [5] for unipolar devices (Schottky Barrier Diodes – SBD –, Junction Field Effect transistors – JFET –, etc.). It is shown that the conduction losses of these devices increase sharply with the temperature, resulting in a destructive failure mode known as thermal runaway. Experimental studies were performed to evaluate the extend of the issue, especially on SBDs. In [6], it is shown that a SBD diode is indeed sensitive to thermal runaway, but the addition of a bipolar junction (to form a Junction Barrier Schottky – JBS – or a Merged PiN Schottky – MPS – structure [7]) largely mitigates the thermal instability. This is confirmed in [8] and [9]. Most (if not all) SiC diodes available on the market today have this kind of Schottky/bipolar structure.

Unipolar controlled switches (JFETs, MOSFETs) do not have such a bipolar junction, and could therefore exhibit this thermal runaway behaviour. In this paper, we will describe the different failure mechanisms of a transistor that can be associated with thermal instability. An experimental approach will then be used to assess the thermal stability of a dual-channel SiC JFET (fig. 1). This type of transistor was chosen because it has been shown to operate reliably at high junction temperature, due to the absence of oxide interface in the structure [11]. It has a normally-on behaviour, which means that it conducts current in the absence of any gate-source bias. A negative gate-to-source voltage bias must be applied to turn this JFET off.

II. Causes of thermal instability

For any given semiconductor device, several thermally-assisted mechanisms may lead to failure. Their existence depends on many parameters: some are intrinsic to the semiconductor material (e.g. increase in on-resistance with temperature); some are related to the device structure (for the JFET under study, the gate punch-through is a good example); and some are related to the external circuit (e.g. paralleling of several devices).

In this section, we will focus on these mechanisms to evaluate which of them may affect dual-channel SiC JFETs.

A. Thermal runaway in blocked state

The two main parameters that define the voltage breakdown of a power device (PN structure) are the doping level (N_D) and the thickness (W) of the lightly-doped – drift – layer (usually the N layer) [7]. Basically, for a given thickness, the lower the doping level, the higher the breakdown voltage. However, if this doping level is too low, it can be overcome by the intrinsic carrier concentration (n_i) in the semiconductor. This intrinsic carrier concentration is given by [7]:

$$n_i(T) = \sqrt{N_c N_v} e^{-\frac{E_G(T)}{kT}}. \tag{1}$$

Where N_c and N_v are the density of available states in the conduction and valence bands respectively, $E_G(T)$ is the energy gap, k the Boltzmann's constant and T the absolute temperature. For a wide-bandgap material such as SiC, E_G is much higher than for silicon (3.26 for 4H-SiC vs. 1.12 for silicon at 300 K [1]), resulting in a much lower intrinsic carrier concentration.

However, following (1), as the temperature increases, so does n_i. In [12], it was shown that above 1600 K ($\approx$ 1300 °C), the intrinsic carrier concentration in 4H-SiC exceeds the doping level required to sustain 1200 V, making it basically unable to withstand the voltage. For a similar voltage, a silicon device would be limited to slightly less than 500K ($\approx$ 200 °C).

From a device point of view, this 1600 K limit is much higher than the maximum operating temperature of the aluminium metallization of the dies (660 °C, 933 K), or the decomposition temperature of the secondary passivation (polyimide, 500–620 °C [6]). We can conclude that the reduction of the voltage breakdown with the temperature should not yield to failure for the devices under test, as it occurs at temperatures that exceed their capabilities (other JFET devices, with alternative metallizations based for example on tungsten are not studied here). Therefore, there is no need for us to investigate this failure mechanism in the experimental part of the paper.

B. Loss of gate control

Two main parameters of the gate characteristic control the JFET: the gate-to-source threshold voltage (V_{T0}) and the gate-to-source punch-through voltage (V_{pt}). V_{T0} is defined as the gate-to-source voltage required to block the device, while V_{pt} is the gate-to-source voltage for which the gate current exceeds an arbitrary value, usually defined as the current that the gate drive circuit can supply continuously. To turn the device off, the following condition must be met (all voltages are negative):

$$V_{T0}(T) > V_{GS} > V_{pt}(T) \tag{2}$$

Indeed, attempting to drive the device with a V_{GS} exceeding the punch-through voltage would result in a large power dissipation in both the transistor and its associated driver. For practical reasons, quiescent currents above a few milliamps are usually avoided.

$V_{T0}(T)$ and $V_{pt}(T)$ tend to have opposite variation with temperature: $V_{T0}(T)$ decreases (i.e becomes more negative) or stays constant, while $V_{pt}(T)$ increases (punch-through occurs sooner) [13]. An obvious failure mode appears when $V_{pt} > V_{T0}$, in which case (2) can no longer be satisfied: it becomes impossible to fully block the transistor, and the resulting off-state losses will trigger a thermal runaway condition.

C. Increase in on-resistance

This mechanism, which we will refer to as "$R_{DS_{on}}$ thermal runaway", is described in [5]: the on-state resistance ($R_{DS_{on}}$) of a device increases with its temperature. This is due to the reduction in electron mobility (μ_n) caused by the interaction of the carriers with the lattice vibrations [7]:

$$R_{on,sp} = \frac{W}{q\mu_n(T)N_D}. \tag{3}$$

Where $R_{on,sp}$ is the ideal specific resistance of a unipolar device operating in the linear region of its I(V) characteristic, taking only into account the resistance of its drift layer. Hence $R_{DS_{on}} > R_{on,sp}/A$ with A the active area of the device. Integrating the temperature dependence $\mu_n(T)$ yields an approximation of $R_{DS_{on}}(T)$ (for a uniformly doped, SiC epitaxial N layer [5]):

$$R_{DS_{on}}(T) = R_{300K}\left(\frac{T}{300}\right)^{2.4}. \tag{4}$$

R_{300K} is the value of $R_{DS_{on}}$ at 300 K. Therefore, the on-state resistance exhibits a strong positive coefficient. If the device is operating under a constant current (as it is often the case in power converters), this increase in resistance results in an increase in power dissipation:

$$P = R_{DS_{on}}(T_J)I_D^2 \tag{5}$$

Where P is the power dissipated by the device, I_D its drain current and T_J the temperature of the device.

If we define Q, the heat removed by the cooling system as

$$Q = \frac{T_J - T_A}{R_{th}} \tag{6}$$

with T_A the ambient temperature and R_{th} the thermal resistance between the active region of the device (its "junction") and the ambient environment, the variation of the internal energy U of the system is given by (first law of thermodynamics):

$$\frac{dU}{dt} = P - Q \tag{7}$$

At the steady state, $\frac{dU}{dt} = 0$, hence $P = Q$. Using (5), (4) and (6), this can be written as:

$$P - Q = R_{300K} \left(\frac{T_J}{300} \right)^{2.4} I_D^2 - \frac{T_J - T_A}{R_{th}} = 0 \qquad (8)$$

The term associated with P has a higher dependence on the temperature ($T_J^{2.4}$) than the term associated with Q (T_J). In some cases (defined by I_D, R_{th} and T_A), (8) cannot be satisfied: the device dissipates more power (P) than the heat removal capability of the cooling system (Q). The junction temperature increases, causing in turn a faster increase in P than in Q. This is the $R_{DS_{on}}$ runaway, described in [5], and observed for some SiC MOSFETs [14]. Note that this mechanism is not specific to SiC, and it can occur with other semiconductor materials, such as silicon.

D. Current focusing effects

Some devices exhibit a positive temperature coefficient of their drain current: this means that under a constant drain-to-source voltage bias, the drain current will increase with the temperature. For unipolar devices, this is caused by a variation of the threshold voltage with the temperature. This can cause thermal runaway, as any "hot spot" across the die (or any temperature difference among paralleled dies) will result in a local increase of the current (the so-called current focusing effect), resulting in higher power losses and increase in temperature of these already-hot areas.

Such failure mechanism was described for low-voltage, silicon power MOSFETs [15]. The driving factor in both cases is the reduction in the threshold voltage V_{T0} of the MOSFETs with the temperature. In [15], it is demonstrated that this sensitivity of V_{T0} is related to the technological evolution of the low voltage MOSFETs, for which the contribution of the drift layer to the overall on-state resistance is negligible. This is not true for SiC power MOSFETs, which operate at higher blocking voltage (600 V and 1200 V devices are investigated in [16]). However, in spite of the increase in $R_{DS_{on}}$ with temperature due to the drift layer, under some thermal and electrical conditions, SiC MOSFETs were found to exhibit an unstable behaviour.

III. Device characterization

Three runaway mechanisms have been identified in the previous section: the loss of gate control, the $R_{DS_{on}}$ runaway, and the current focusing. In this section, we will use experimental data to demonstrate which of these mechanisms can affect SiC JFETs.

A. Experimental setup

A dedicated test vehicle was designed for this study. It is depicted in figure 2 and comprises:

- a 1200 V-rated SiC JFET die, supplied by SiCED, now part of Infineon
- a ceramic substrate (alumina DBC), from Curamik electronics Gmbh;
- a high temperature die attach, based on silver sintering;

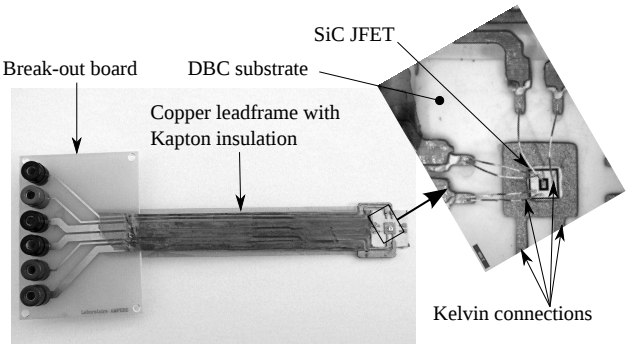


Fig. 2. Details of the high-temperature test vehicles

TABLE I
Details of the Test Vehicles (TV) (devices manufactured by SiCED with a voltage rating of 1200 V)

TV number	JFET Die size	JFET $R_{DS_{on}}$	TV R_{th}
#1	2.4×2.4 mm^2	490 mΩ	4.5 K/W
#2	4.08×4.08 mm^2	57 $m\Omega$	7.9 K/W
#3	4.08×4.08 mm^2	65 $m\Omega$	2 K/W

- Kelvin connections (4-point) for the drain and source terminals. The source terminals are connected using aluminium wirebonds (Thales TMI).
- A copper leadframe (thickness 350 μm) insulated using kapton tape to connect the high temperature substrate to a breakout board (which remains at room temperature);
- The breakout board, a simple PCB which offers an easy way to connect the test vehicle to the various measurement tools.

Three different test vehicles were assembled. The dimensions of the JFET dies used and their $R_{DS_{on}}$ are listed in table I. The R_{th} value is described later in the paper. The characterizations performed on the three test vehicles (one for each tested JFET) include:

- standard I_D/V_{DS} characterization, using a Tektronix 371A high power pulse curve tracer, over the complete power range (up to 30 V V_{DS} or 3 kW, whichever comes first);
- a I_G/V_{GS} characterization, using a Keithley 2410 Source and Measure Unit (SMU), offering very low current resolution (less than 1 nA). This characterization was performed from 0 to -40 V, with a current compliance of 1 mA.

All characterizations were performed over a large temperature range (-70 to 290 °C) using a temperature conditioner (Thermonics T2500/E). The temperature was measured on the back of the substrate after a short soaking delay.

A preliminary characterization, performed on a 4.08×4.08 mm^2 JFET (similar to JFETs #2 and #3) in a vacuum probe station, showed that the leakage current at 300 °C and 600 V is lower than 64 μA. This confirms the analysis of section II-A and we can assume that the power dissipated by the transistors in blocking condition is not high enough (< 0.1 W) to trigger any runaway mechanism. This measurement was not performed on the devices from table I

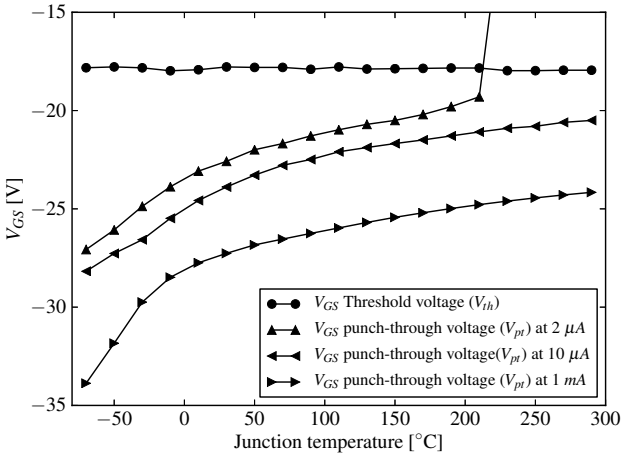


Fig. 3. Evolution of the gate-to-source punch-though voltage (V_{pt}) and the gate-to-source threshold voltage (V_{T0}) with temperature, for JFET #1. The punch-through voltage is measured at 2 μA, 10 μA and 1 mA gate current.

because it cannot be performed in air without encapsulation and because the test vehicles depicted in figure 2 are too long to fit in our vacuum probe station.

B. Evolution of the gate characteristic

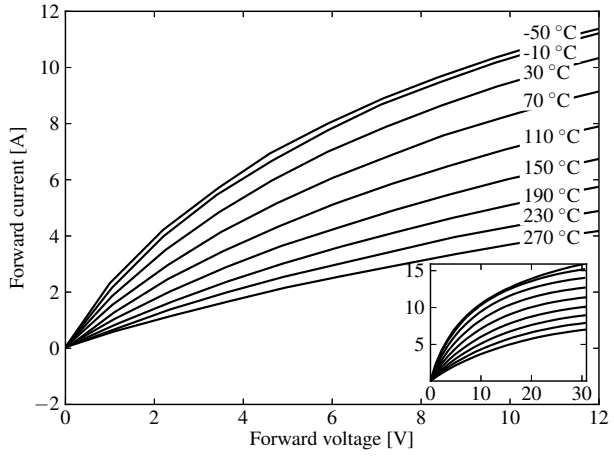
When the JFET operates in the saturation region, its I_D/V_{DS} characteristic can be approximated using the following equation, based on [17]:

$$I_D = \begin{cases} 0 & \text{if } V_{GS} < V_{T0} \\ Kpsat(V_{GS} - V_{T0})^2 & \text{if } V_{GS} \geq V_{T0} \end{cases} \quad (9)$$

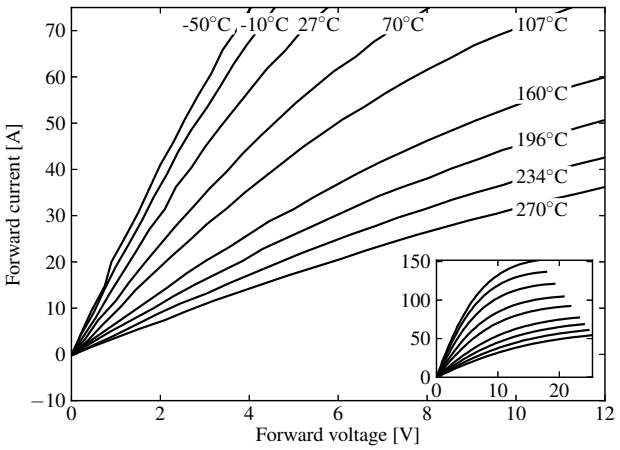
Where $Kpsat$ is the "transconductance" of the JFET, neglecting any channel modulation effect. Note that the I_D/V_{DS} characteristic is actually more complex, as the JFETs used here have two channels (one horizontal, one vertical) [17]. V_{T0} and $Kpsat$ can be identified with the experimental I_D/V_{DS} characterization data using a least squares technique. The evolution of V_{T0} with the temperature is plotted in figure 3 and shows that there is little change over the temperature range. This is confirmed by [11], as V_{T0} is mainly related to the doping level in the JFET and its geometry, all independent on the temperature.

The punch-through voltage of the gate-source junction (V_{pt}) is directly extracted from the experimental I_G/V_{GS} characterization. Its definition is somewhat arbitrary, as it corresponds to the gate-to-source voltage resulting in a defined gate current. V_{pt} is plotted in figure 3 for three values of I_G: 2 μA, 10 μA and 1 mA. It can be seen that the three curves exhibit a rising trend of the punch-through voltage with the temperature. For 10 μA, there is no intersect between V_{pt} and V_{T0} over the -70/+290 °C range, although the set of values allowed to properly block the device (eq. (2)) at any temperature becomes fairly small (-18 to -20 V). This "safety" margin becomes wider for an allowable gate current of 1 mA. For 2 μA, however, one can see in fig. 3 that it is not possible to turn the JFET off above 210 °C.

This means that to ensure a reliable control of this JFET, the gate drive must be able to supply a gate current of 10 μA



(a)



(b)

Fig. 4. Static characteristic of JFET #1 (a) and JFET #2 (b), for junction temperatures ranging from -50 to 270 °C, and a gate-to-source votage of 0 V (JFET fully-on). The graphs correspond to a "zoom" on the lower I,V range. An overview of the complete data (showing the saturation region) is shown in the insets.

at least (this condition should easily be met with most driver circuits), especially at the higher temperatures. Attempting to turn this JFET off with a lower current capability at elevated temperature would result in a catastrophic failure.

C. Evolution of the $R_{DS_{on}}$ with the temperature

The I_D/V_{DS} characteristics of JFET #1 and #2 are plotted in figure 4, for $V_{GS} = 0\ V$ (JFET fully-on). The characteristic of JFET #3 is not presented here, but it is essentially similar to that of JFET #2.

It can be seen that as the temperature increases, $R_{DS_{on}}$ increases and the saturation current of the JFETs decreases. This indicates that in any circumstances, if the JFETs are submitted to a constant V_{DS} bias, any increase in temperature will result in a decrease in the drain current. Therefore, as the drain current of the JFETs has a negative temperature coefficient, the current focusing effect demonstrated with SiC MOSFETs (as described in section II-D) is not possible with JFETs. This is caused by the almost constant gate to source

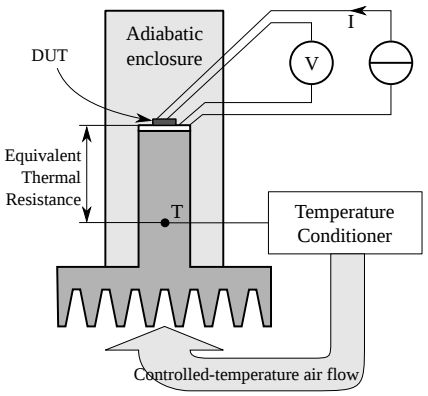


Fig. 5. Principle of the runaway test bench: the Device Under Test (DUT) is connected to a current source and the voltage across the DUT is measured. Its gate and source terminals are short-circuited to ensure it is "fully-on". The thermal environment is controlled using a thermal conditioner to achieve a constant temperature at point T, regardless of the heat dissipated by the DUT.

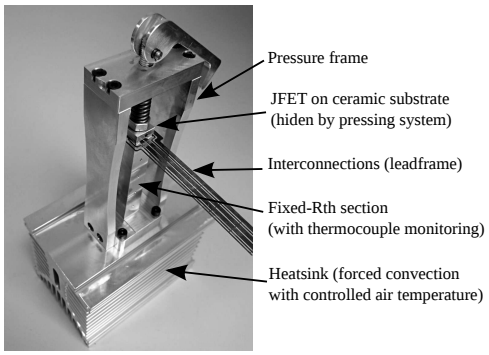


Fig. 6. The test support, showing the pressing frame, the location of the test vehicle, and the heatsink. Thermal insulation (not shown) is used to ensure that all the heat dissipated by the die is evacuated through the heatsink.

threshold voltage (see $V_{T0}(T)$ in figure 3) and by the increase in resistivity of SiC (eq. (3)).

However, as the $R_{DS_{on}}$ has a positive temperature coefficient, the thermal runaway mechanism described in section II-C can be expected. In the next section, we describe an experimental approach to assess the risk of $R_{DS_{on}}$ thermal runaway in realistic conditions.

IV. Experimental study of the $R_{DS_{on}}$ thermal runaway

A. Experimental setup

The thermal test setup shown in figure 5 was designed to host the test vehicles described in section III-A. It provides the test vehicles with a constant thermal resistance over a large range of (controlled) ambient temperature.

The test vehicles are placed on an aluminium pillar (with a layer of high temperature thermal interface material), which is secured to a large heatsink. A spring-loaded system ensures a good contact between the test vehicle and the pillar. A thermal conditioner is used to blow air on the heatsink, and we monitor the temperature at a specific location of the aluminium pillar (point T in figure 5). By adjusting the temperature of the air, it becomes possible to ensure a constant temperature at point T.

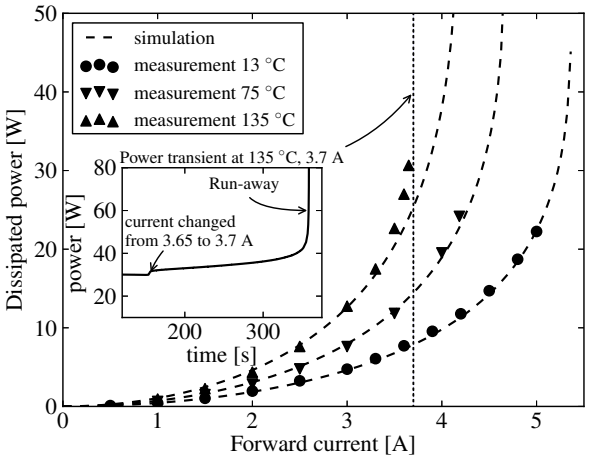


Fig. 7. Power dissipated by JFET #1 (4.5 K/W thermal resistance) as a function of its forward current, and for 3 different ambient temperatures (13, 75, and 135 °C). The symbols correspond to measurements, the lines to simulation (computing the solutions of (8)). The device entered (non-destructive) thermal runaway at 3.7 A, 135 °C ambient temperature. The transient power measured during runaway is plotted in the detail graph.

This is equivalent to having a perfect cold source at the T point in figure 5. Furthermore, the equivalent thermal resistance is only dependent on conduction mechanisms, and we can avoid any non-linearity that would be introduced by the convection mechanisms at the heatsink/air interface.

By adjusting the position of the thermocouple on the pillar, the equivalent thermal resistance can be varied (as visible in table I). The actual R_{Th} value is measured by monitoring the value of the $R_{DS_{on}}$ under a small current (0.5 to 2 A). At this current level, the JFET can be considered to have a purely resistive behaviour (no effect of current saturation, see figure 4) but dissipates enough power to produce a measurable temperature increase.

Figure 6 shows a picture of the test bench with the adiabatic enclosure removed. This enclosure is formed by a teflon sleeve filled with vermiculite.

The test vehicle is then connected to a power supply operating as a current source, and the voltage across the die is measured using a precision voltmeter (Keithley 2700). The current is controlled using a shunt (Metrix HA0171) and a precision voltmeter (Keithley 2000). Given the thermal mass of the test bench, 10 to 30 min are required for the system to reach equilibrium for each measurement point.

B. Results

For the experiment, measurements were performed at three ambient temperature values (i.e. constant temperature at point T): 13 °C, 75 °C, and 135 °C. The range of temperature was chosen as wide as possible, but was limited by the cooling and heating capability of the temperature conditioner: to maintain the temperature at point T constant, the actual air temperature had to be varied between -60 and more than 200 °C.

The current (I_D) value was then gradually increased, leaving enough time for the system to stabilize, and the dissipated power was calculated by multiplying I_D and V_{DS}. This cal-

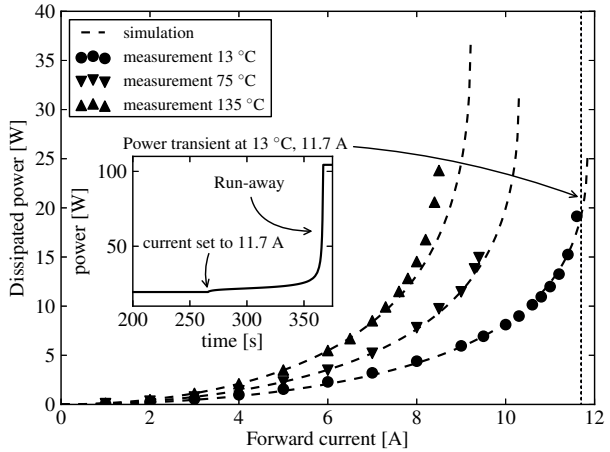


Fig. 8. Power dissipated by JFET #2 (7.9 K/W). The device entered (destructive) runaway at 11,7 A, 13 °C ambient temperature.

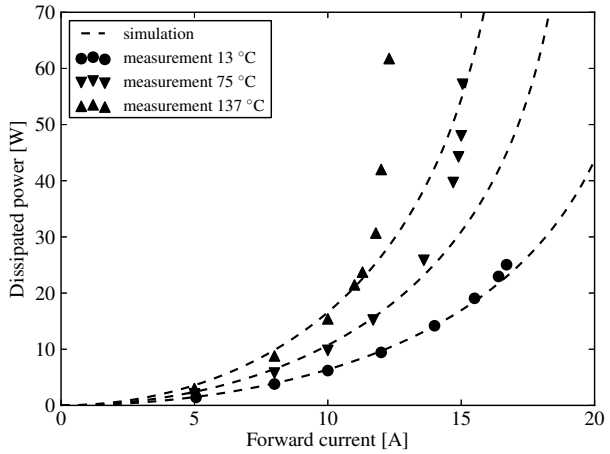


Fig. 9. Power dissipated by JFET #3 (2 K/W). For the "13 °C" curve, the power was limited by the cooling capability of our test bench. In all cases, the dissipated power was limited to 110 W to avoid the destruction of the device.

culation does not include the power losses in the interconnects, as kelvin connections were used up to the JFET die itself.

The P/I_D graphs are given in figures 7, 8 and 9 for the JFETs #1, #2 and #3 respectively. On these graphs, the dashed lines correspond to simulation (solving of (8)). All 3 JFETs exhibited thermal runaway at some point, where a small increase in drain current (e.g changing the drain current from 11.6 to 11.7 A in fig 8) would trigger an unstable behaviour.

For all tests, the power supplied to the dies was limited to around 110 W. This still allowed JFET #2 to enter destructive behaviour, due to its higher thermal resistance, but was too low to damage JFETs #1 and #3, which were able to recover from the thermal runaway.

Photographs of JFET #2 after destruction are visible in figure 10. The top metallization (aluminium) of the JFET exhibits some changes due to it melting during runaway. This indicates that the temperature exceeded 660 °C over a large part of the die. This is consistent with the power dissipated (limited by the power supply to 110 W during runaway) and the thermal resistance of the JFET (7.9 K/W).

The aluminium metallization of JFET #1 and #3 does not show any consequence of the tests, which is also consistent with the maximum power they were allowed to dissipate and their thermal resistance. For example, for the runaway waveform depicted in figure 7, the maximum junction temperature can be calculated as:

$$T_J = T_A + P \times R_{th} = 135 + 110 \times 4.5 = 630°C. \quad (10)$$

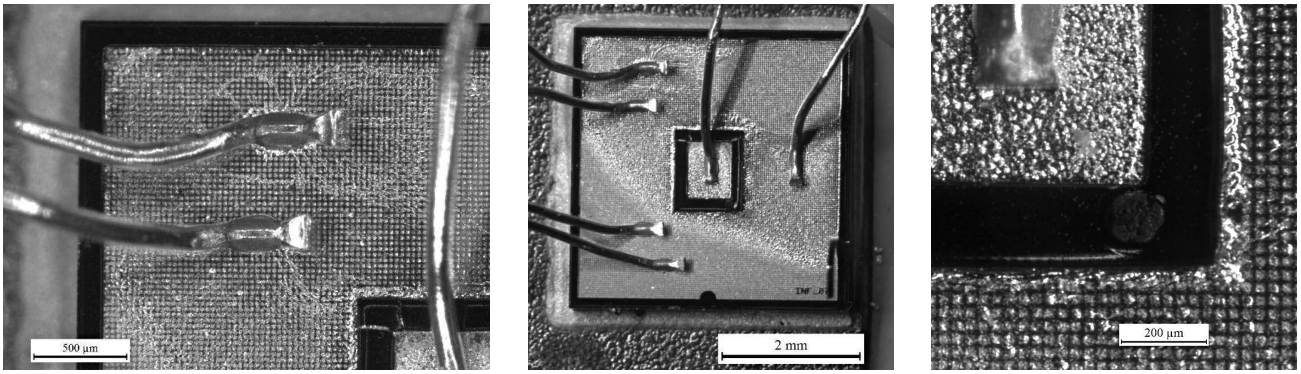
Although fairly high, such temperature is still lower than the melting point of aluminium, and can be sustained by the JFETs for a few seconds or minutes without short-term degradation. In the longer term, however, some degradation could occur. For example, the top metal layer (aluminium) of power devices has been found to become more resistive after thermal cycling [18].

C. Discussion on $R_{DS_{on}}$ thermal runaway

The experiments described in the previous section clearly show that all 3 JFETs are sensitive to $R_{DS_{on}}$ thermal runaway, for all ambient temperatures. A reduction in the thermal resistance (from 7.9 K/W for JFET #2 to 2 K/W for JFET #3) resulted logically in an increase in the drain current required to trigger the thermal runaway. However, note that in all cases, this maximum drain current was fairly low, from 3.7 A (64 A.cm^{-2}) for JFET #1 at 135 °C ambient to less than 20 A (120 A.cm^{-2}) for JFET #3 at 13 °C ambient. This is lower than the maximum current predicted by (8), which is plotted with dashed curves in figures 7, 8 and 9. Such behaviour can be explained by the influence of the saturation current in the JFETs: using the static characteristics depicted in figures 4(a) and 4(b), it appears that even for V_{DS} values lower than 5 V, the JFET does not exhibit a perfect, linear characteristic. Therefore it cannot be simply represented by the resistance of its epitaxial layer. The saturation current in the channel tends to limit the current, resulting in a higher voltage drop and higher losses. An illustration of this phenomenon is given in Fig. 11, and is especially visible for the "2 K/W" curves: the thermal runaway occurs at much sooner than expected when considering only the variation in resistivity of SiC.

Although it constitutes a severe limitation to use JFETs at high power levels, it is possible to protect the devices against this $R_{DS_{on}}$ thermal runaway mechanism: like with most silicon IGBT driver, the gate driver of the JFETs must include a "desaturation" protection, which monitors the V_{DS} voltage of the device, and turns it off above a certain value. This value should be chosen so that the protection is only activated at the onset of a thermal runaway, and never during normal operation. In the case of JFET #2 (fig. 8), this would correspond to a dissipated power level of around 15 W or more, for $I_D > 8\ A$. Therefore, a threshold of $\approx$2 V seems adequate for this component.

Furthermore, as visible in figures 7 and 8, the runaway waveforms are fairly slow compared to the switching speed of a JFET (seconds as compared to a few tens of nanoseconds). Indeed, as no focusing effect is associated with the $R_{DS_{on}}$ thermal runaway, the dissipated power is dissipated evenly



(a) (b) (c)

Fig. 10. Photographs of the SiC JFET #2 after destructive runaway. The aluminium metallization melted in places, especially around the top left wirebonds (a). This indicates that the surface temperature of the die exceeded 660 °C. Other consequences of the runaway include the lift-off of the polyimide passivation (b), bottom right corner of the die, and a (hardly visible) round mark under the polyimide layer between gate and source (c). The gate is the small aluminium rectangle in the center of the die (b). Note that 5 wirebonds are connected to the source, 4 to supply the current, the last one to measure the voltage (Kelvin configuration).

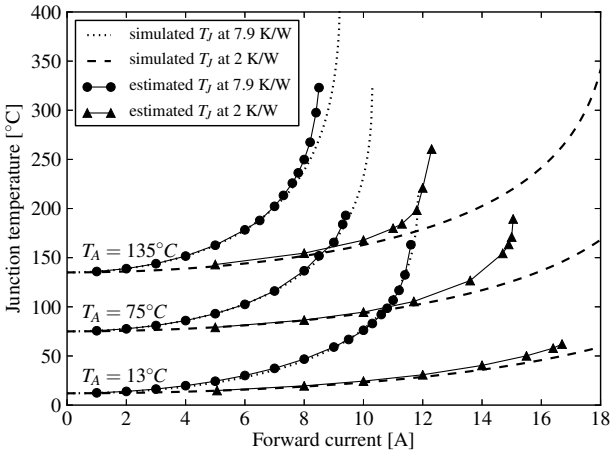


Fig. 11. Calculated JFET junction temperature as a function of the forward current, for different ambient temperatures (13, 75 and 137 °C and two different thermal resistances. The "simulation" curves are computed using eq. (8).

over the complete die, increasing the thermal mass involved, and slowing down the temperature rise.

Another solution to mitigate the effect of thermal runaway could be to drive the JFET with a small, positive V_{GS} bias (lower than 2.5 V, in order not to exceed the gate-to-source PN junction threshold). As described in [19], applying 2 V between gate and source only has a minor effect on the $R_{Ds_{on}}$ (4% decrease for a JFET comparable to JFET #1), but results in a much higher saturation current (30% increase compared to $V_{GS} = 0\ V$). This would result in lower power dissipation for the JFET for a given I_D. Applying a positive bias, however, requires modifications to the gate drive circuit, and might prove unpractical.

V. Conclusion

Two failure modes related to thermal instability were found to affect SiC JFETs: the loss of gate control, and the $R_{DS_{on}}$ thermal runaway. The first of them can be easily avoided by using a gate driver with a quiescent current capability exceeding a few microamps.

The second failure mode, however, was found to be even more severe than expected initially, based on the simple temperature-dependence of the resistivity of SiC. Indeed, as the temperature increases, the saturation current drops, resulting in an apparent increase in the $R_{DS_{on}}$ value of the transistor. This in turn results in higher losses, and triggers the thermal runaway.

These results confirm that JFETs must be associated with an efficient cooling system. Furthermore, a protection circuit must be implemented in the gate driver to turn the transistor off if its drain-to-source voltage exceeds a few volts. Providing both conditions are met, SiC JFETs can be used reliably over a large temperature range, albeit at a moderated current density (for the JFETs studied here, the current density achived before runaway was in the order of 60 to 80 A.cm^{-2}). These results pinpoint the need for accurate, electro-thermal JFET models to analyze the failure modes of a converter at the design stage.

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References

[1] J. Casady and R. Johnson, "Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review," *Solid-State Electronics*, vol. 39, no. 10, pp. 1409 – 1422, 1996. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0038110196000457

[2] T. Funaki, J. C. Balda, J. Junghans, A. S. Kashyap, H. A. Mantooth, F. Barlow, T. Kimoto, and H. Takashi, "Power Conversion With SiC Devices at Extremely High Ambient Temperatures," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1321–1329, jul 2007.

[3] C. Buttay, D. Planson, B. Allard, D. Bergogne, P. Bevilacqua, C. Joubert, M. Lazar, C. Martin, H. Morel, D. Tournier, and C. Raynaud, "State of the art of high temperature power electronics," *Materials Science and Engineering: B*, vol. 176, no. 4, pp. 283 – 288, 2011, microtechnology and Thermal Problems in Electronics. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0921510710006136

[4] J. M. Hornberger, E. Cilio, R. M. Schupbach, A. B. Lostetter, and H. A. Mantooth, "A High-Temperature Multichip Power Module (MCPM) Inverter utilizing Silicon Carbide (SiC) and Silicon on Insulator (SOI) Electronics," in *Proceedings of the 37th Power Electronics Specialists Conference (PESC)*. Jeju, Korea: IEEE, Jun. 2006, pp. 9–15.

[5] K. Sheng, "Maximum Junction Temperatures of SiC Power Devices," *IEEE Transactions on Electron Devices*, vol. 56, no. 2, pp. 337–342, feb 2009. [Online]. Available: http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?isnumber=4757346&arnumber=4752775&count=33&index=26

[6] C. Buttay, C. Raynaud, H. Morel, G. Civrac, M.-L. Locatelli, and F. Morel, "Thermal Stability of Silicon Carbide Power Diodes," *IEEE Transactions on Electron Devices*, vol. 59, no. 3, pp. 761–769, 2012.

[7] B. J. Baliga, *Power Semiconductor Devices*. Boston: PWS Publishing Company, 1997.

[8] W. Janke and A. Hapka, "The thermally induced limitations of SiC SBDs operation conditions," *Microelectronics Journal*, vol. 43, pp. 656–660, 2012.

[9] A. Hapka, W. Janke, and J. Krasniewski, "Influence of series resistance and cooling conditions on I–V characteristics of SiC merged PiN Schottky diodes," *Materials Science and Engineering: B*, vol. 177, no. 15, pp. 1310 – 1313, 2012, microTherm2011 – Microtechnology and Thermal Problems in Electronics. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0921510712001018

[10] P. Friedrichs, "Compact Power Electronics due to SiC Devices," in *Proceedings of the Conference on Integrated Power Systems (CIPS 08)*, nuremberg, march 2008.

[11] P. Friedrichs and D. Stephani, "Unipolar SiC power devices and elevated temperature," *Microelectronic Engineering*, vol. 83, pp. 181–184, 2006. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0167931705005125

[12] C. Raynaud, D. Tournier, H. Morel, and D. Planson, "Comparison of high voltage and high temperature performances of wide bandgap semiconductors for vertical power devices," *Diamond and Related Materials*, vol. 19, no. 1, pp. 1 – 6, 2010. [Online]. Available: http://www.sciencedirect.com/science/article/B6TWV-4XCJ4M2-1/2/76c76271c9345bf77d4fc29077179d2a

[13] F. Dubois, D. Bergogne, D. Tournier, C. Buttay, R. Meuret, and H. Morel, "Analysis of the SiC VJFET gate punch-through and its dependence with the temperature," in *Proceedings of the European Conference on Power Electronics and Applications (EPE)*, Lille, France, sep 2013.

[14] S. Pyo and K. Sheng, "Junction temperature dynamics of power MOSFET and SiC diode," in *Power Electronics and Motion Control Conference, 2009. IPEMC '09*. Wuhan: IEEE, may 2009, pp. 269–273.

[15] A. Consoli, F. Gennaro, A. Testa, G. Consentino, F. Frisina, R. Letor, and A. Magri, "Thermal instability of low voltage power-MOSFETs," *Power Electronics, IEEE Transactions on*, vol. 15, no. 3, pp. 575 –581, may 2000.

[16] A. Castellazzi, T. Funaki, T. Kimoto, and T. Hikihara, "Thermal instability effects in SiC Power MOSFETs," *Microelectronics Reliability*, vol. 52, pp. 2414–2419, 2012. [Online]. Available: http://www.sciencedirect.com/science/journal/00262714

[17] T. Ben Salah, H. Morel, and S. Mtimet, "Toward SiC-JFETs modelling with temperature dependence," *European Physical Journal Applied Physics*, vol. 52, no. 20301, p. 8, 2010.

[18] bouarroudj M., Z. Khatir, J.-P. Ousten, F. Badel, L. Dupont, and S. Lefebvre, "Degradation behavior of 600 V–200 A IGBT modules under power cycling and high temperature environment conditions," *Microelectronics Reliability*, vol. 47, pp. 1719–1724, 2007.

[19] S. Round, M. Heldwein, J. Kolar, I. Hofsajer, and P. Friedrichs, "A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter," in *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, vol. 1. IEEE, 2005, pp. 410–416.

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