A Unique FPGA for the Implementation of Neural Strategies for Identifying Harmonic Distortions

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***Abstract* – In this paper, three optimized neural harmonics extraction methods are presented and compared in terms of simulation results, FPGA implementation and practical considerations. Those distortion identification schemes are used in nonlinear loads compensation with Active Power Filters (APF). This optimization is performed in order reduce the number of hardware resources required for digital implementations. The given approaches tend to use only one Adaline and remain powerful even under unbalanced conditions of voltage. In this way, the implementation of all the functionalities of the active filter control has been realized by means of a unique FPGA chip. Moreover, even the most consuming method (i.e., the ITM) uses less than 52% of hardware resources. Even though the *mp-q* technique (based on the instantaneous reactive power theory) is not the fastest in terms of hardware response time, it stills appear the most powerful for its filtering aptitudes with an experimental source-side current THD of 3.3% after compensation.**

I. INTRODUCTION

In order to reduce distortions created by non-linear loads (static rectifiers, adjustable speed drives, DC/AC converters, etc.), the Active Power Filter (APF) is nowadays one of the most powerful solutions. It is therefore used in a distribution power system to avoid serious inherent problems such as transformer overheating, machine vibration, motor failures, higher line losses, etc. The switching actions of power converters result in distorted input currents, which contain a fundamental and some other higher order harmonics. Injection of compensation currents in the electrical power supply by means of an APF allows sinusoidal current shape recovery as well as reactive power compensation. In the process of harmonic compensation, detection of load current harmonics is one part, while the generation of compensating harmonic currents by means of converter switching is the other part of APF. Performances of APFs depend on harmonic detection methods for generating current references, current control method, and dynamic characteristics of their power converter circuit. The filtering performances are essentially affected by the current references generation.

Most of the contributions for harmonics extraction were in time domain. For example, the Synchronous Reference Frame (SRF) theory is based on the filtering of DC current components by a low-pass filter in synchronously rotating frame [1]. At the beginning of the 1980s, Instantaneous Reactive Power Theory (IRPT) emerged and is still now one the most powerful technique for distortion identification in power systems. The objective of the IRPT was to find an effective control strategy to compensate three-phase nonlinear loads by means of an APF [2][3].

A lot of recent research work investigates and tries to improve APFs by developing new control laws. In this way, Artificial Neural Networks (ANNs) have been successfully applied in power systems like APF. Indeed, some ANNs-based harmonics detection schemes such as Improved Three-Monophase (ITM) and the Modified SRF *(MSRF)* methods also called TPF for Two-Phase Flow have been discussed in [4][5] with interesting adaptive properties. Another way is an IRPT formulation based on a neural approach which works properly for phase and symmetrical components estimation in power systems perturbed by harmonics, random noise and source voltage sags [6][7]. In [8][9], authors discuss a multiplexing approach focused on the IRPT, and based on a single neural network, i.e., the Adaline. This was motivated by a need for simplicity and flexibility inherent to ANNs-based control strategies, but also to optimize the hardware resources required in digital implementations.

Implementing complex algorithms on reprogrammable devices allows fast time-to-market, enables easy prototyping through Hardware Description Language. Since ANNs in general are inherently parallel architectures, implementing ANNs on Field Programmable Gate Array (FPGA) seems to be an excellent choice due to its aptitudes for parallel processing [10][11][12].

The work presented in this paper gives a comparative study of three recent neural schemes for distortion identification in terms of settling time and filtering capability against load currents fluctuations and unbalanced conditions. These methods are also compared in terms of execution times and

required resources area in case of FPGA implementation. In recent works, the APF control scheme is generally implemented in real time using a Digital Signal Processor (DSP) in a dSPACE board board. Sometimes this board is used in association with an FPGA card in which the current controller which drives the gating signals for the APF inverter is implemented. Another purpose of this work is to show that it is possible to implement all the functionalities of the APF control unit by means of a unique FPGA chip.

The harmonics identification methods are simulated in Matlab/Altera Dsp Builder™. In Section 2, neural methods for reference current generation are investigated and algorithms are introduced. Performances of the methods regarding simulation results and FPGA programming abilities are analyzed in Section 3. Finally, in Section 4, experimental results are presented to confirm those obtained after simulations, and on the other hand to show the feasibility of implementing the whole APF control unit in FPGA as the unique target.

II. ANN-BASED MAJOR DISTORTION IDENTIFICATION APPROACHES

In general, the APF control unit can be decomposed in the following blocks. A first block which has to identify all the present harmonic components and to separate the fundamental component from the other harmonic components which are converted in resulting reference currents. A second block uses these reference currents to re-inject them in real-time into the utility source with opposite phase though a power circuit, i.e. an inverter and an output filter, and a third block which preserves the DC-link voltage at its reference value. The reference currents are issued from an ANN which learning process is done on line. Fig. 1 presents a shunt APF in an electrical power grid. As it is one of the most important block of the APF control unit, this paper discusses three neural methods for generating the reference currents.

A. IRPT based multiplexing approach

The original reference currents generation architecture is made up of three identical ANNs. In [8][9], a simplified structure is proposed which uses only one ANN by a multiplexing technique. Fig. 2 shows the obtained structure which results in optimizing hardware resources consumption.
The instantaneous powers p and q are calculated from the voltages and currents in $\alpha\beta$−frame with (1):

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (1)$$

Let z_k be at iteration k one of the desired instantaneous powers to be learned by the ANN. After a training process, the neural network will estimate its value $\hat{z}_k$. The corresponding errors $e_k = z_k - \hat{z}_k$ should be stored in a memory. The learning serves to update the weight w_{kj} of the neural structure for any input x_j as illustrated by relation (2):

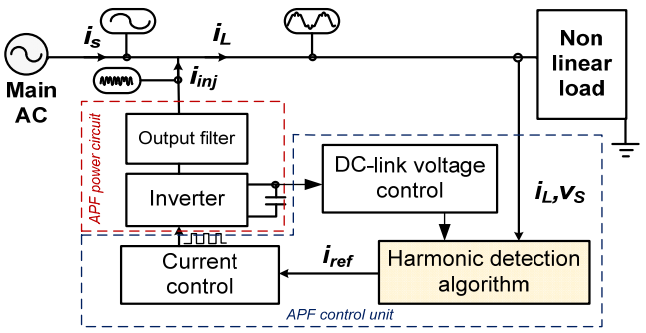

Fig. 1. A shunt APF in an electrical power system

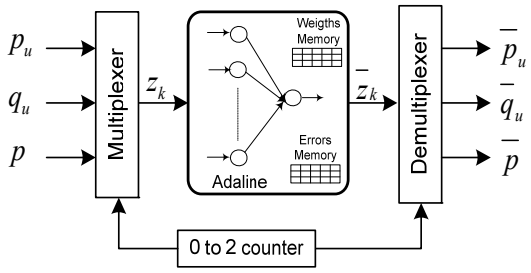

Fig. 2. Application of the multiplexing technique on the *p-q* harmonics detection method.

$$\mathbf{W}_{(k+3)j} = \mathbf{W}_{kj} + \frac{\mu . e_k . \mathbf{X}_j}{\lambda + \mathbf{X}_j^T . \mathbf{X}_j}; j = 1, \ldots, N \quad (2)$$

This learning process is based on the Widrow-Hoff algorithm where μ is the learning rate ($0<\mu<1$), λ is an appropriate constant to ensure a non-zero denominator and N the number of Adaline inputs.
Finally, the estimated DC component $\hat{z}_k$ of z_k is obtained by using the first two elements of the weight vector w_k. p_u and q_u are fictitious instantaneous powers obtained from the symmetrical component extraction block. On the other hand, a demultiplexer is used to separate the DC components $\bar{p}_u$, $\bar{q}_u$ and $\bar{p}$ respectively. AC values of p and q ($\tilde{p}$, $\tilde{q}$) are produced with the harmonic components of the load current. The design is then simplified for area efficient implementation.

In order to compensate the harmonics and instantaneous reactive power, the compensating currents $i_{ref\alpha}$ and $i_{ref\beta}$ on $\alpha\beta$ coordinates are calculated by using $-\tilde{p}$ and $-q$ as given in (3):

$$\begin{bmatrix} i_{ref\alpha} \\ i_{ref\beta} \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} -\tilde{p} + p_{dc} \\ -q \end{bmatrix}, \quad (3)$$

p_{dc} is the added power to achieve the capacitor voltage v_{dc} regulation, at the DC side of the inverter. The reference compensating currents in the *a–b–c* coordinates are then obtained with (4):

$$\begin{bmatrix} i_{refa} \\ i_{refb} \\ i_{refc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}^T \begin{bmatrix} i_{ref\alpha} \\ i_{ref\beta} \end{bmatrix} = T_{32} \begin{bmatrix} i_{ref\alpha} \\ i_{ref\beta} \end{bmatrix}. \quad (4)$$

where T_{32} is the Concordia matrix.

B. *ITM identification method*

As presented in [4][5], the three-monophase method works directly with the distorted current iL(t) and identifies fundamental component iLf(t), and thus the harmonics iLh(t) for each phase with two Adalines. By multiplying the load current by sinωt, we obtain the expression (3) which is then represented by one Adaline.

$$\begin{aligned} i_L(t)\sin\omega t &= \frac{1}{2}\left(I_{12} - I_{12}\cos 2\omega t + I_{11}\sin 2\omega t\right) \\ &+ \frac{1}{2}\sum_{n=2\ldots n}\left(I_{n2}\cos(n-1)\omega t - I_{n2}\cos(n+1)\omega t\right) \\ &+ \frac{1}{2}\sum_{n=2\ldots n}\left(I_{n1}\sin(n+1)\omega t - I_{n1}\sin(n-1)\omega t\right) \end{aligned} \quad (3)$$

where I_{12} is the bias weight of the corresponding Adaline. For the other Adaline, issue from the multiplication of $i_L(t)$ and $\cos\omega t$, I_{11} is the bias weight. By looking more closely at equation (3), it can be noticed that besides the weight I_{12}, I_{11} can also be determined as the steady state weight corresponding to the input $\frac{1}{2}\sin 2\omega t$ of the same Adaline. In this way, it is shown that the three-phase harmonics identification can be done with one Adaline per phase.

C. *MSRF method*

The other neural identification method, i.e. the MSRF [4][5] is based on the known SRF technique. This approach relies on an original decomposition of the three-phase currents. These currents are successively converted into the αβ- and DQ-spaces with respectively the Concordia and Park transforms. In DQ-space the currents are decomposed in linear expressions, AC components are separated from the DC's by an Adaline. The AC components represent harmonic currents into the same space. By applying Concordia and Park transforms to those currents, we can finally obtain the three-phase reference currents. With the proposed ANN-based it is then possible to obtain all the reference currents with only one Adaline.

III. SIMULATION RESULTS AND FPGA IMPLEMENTATION

Simulations have been made in various utility conditions using Simulink™ with Altera Dsp Builder™ toolbox for different controller configurations. Switching frequency of the inverter is set at 12.5 kHz. Neural reference currents generation associated to a three-phase neural approach for symmetrical components estimation was developed. The instantaneous phase estimation block was added to deal with changing parameter in power grid by obtaining real time reference currents. The current controller based on a neural PI regulator was tested as well as with Bandless Hysteresis approach [13]. This allows generating phase-opposite the three-phase reference current on the grid to suppress harmonic and compensate reactive power.

Fig. 3 shows simulation results under a 20% unbalanced source voltage (Fig.3a) for mp-q and MSRF methods. The simulation parameters are given below: Source voltage (Vsa=55V, Vsb=40V, Vsc=81.6V, f=50Hz), Load (a rectifier and a R-L branch; R=20Ω, L=12.5mH). All type of non linear loads can be used. Results are shown for inductive loads because they are widely founded in industrial domain. The distorted load current is shown in Fig. 3b) while the source current after compensation corresponds to the waveform of Fig. 3c). This current reveals a THD up to 1.92% for a sampling time of 10µs which corresponds to the mp-q method. Fig. 4 presents waveforms under balanced load with a sudden decrease of load currents amplitude at time 0.08s. During simulations, we obtained the same results for the proposed distortion identification techniques. In addition, Table I shows the settling time and the source-side current THD after compensation. The fastest method is the MSRF with a settling time of 20ms whereas the ITM method is the slowest one with a settling time of 45ms. Moreover, we can there notice that contrary to the other methods, ITM is adequate for single phase systems despite the lack of efficiency under unbalanced source voltage.

Hardware implementation was done on FPGA Stratix II target from the synthesis tool called Quartus™ II. Because of the limited quantity of logics resources available on the target, implementation optimization techniques were necessary for the algorithms. An efficient comparison of hardware resource consumption for different harmonic detection approaches takes also into account particular resources used for calculations. Embedded 9 bits-DSP blocks used to implement multipliers and Arithmetic Look-Up Tables (ALUT), basic cells used in the Quartus® II software for logic synthesis are one of them. As the multiplexing technique were applied to the neural p-q to obtain a more area efficient structure called mp-q, the SRF and the Three Monophase methods have also been simplified to obtain respectively the MSRF and the ITM

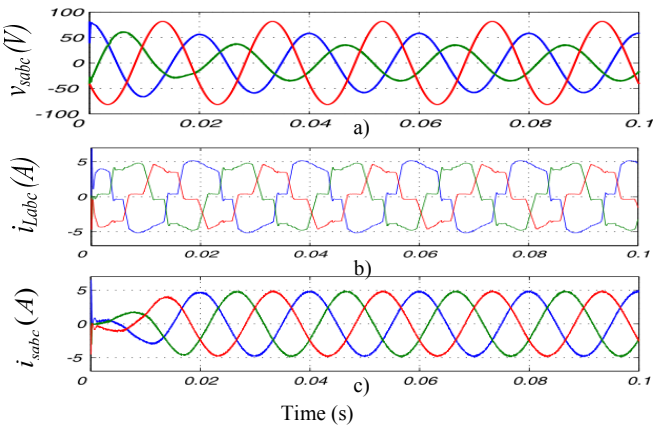

Fig. 3. Results under unbalanced and sinusoidal voltage source with balanced load for MSRF and mp-q methods: a) Unbalanced source voltage, b) Three-phase distorted load current, c) Source current after compensation

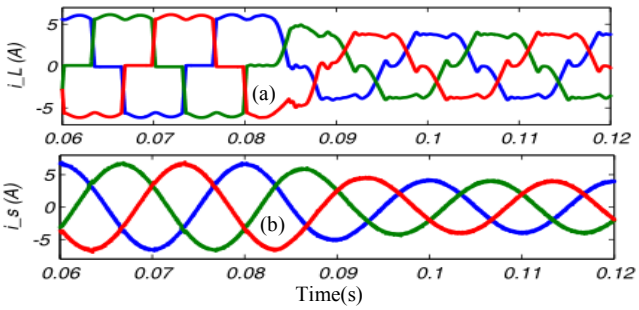

Fig. 4. Results under balanced load with a sudden change at 0.08s for mp-q, MSRF and ITM methods : (a) Load current, (b) Source currents after harmonics suppression

techniques. Consequently, none of these identification methods exceeds 52% of the available resources on FPGA, as presented in Table II. The MSRF technique is the less consuming technique. It uses only 21.6% of FPGA calculation resources whereas the mp-q formulation uses 45.3% and the ITM technique 52%. This can be explained by the important number of Adalines used for harmonics detection, i.e. three for the ITM method instead of one for the others.

On the other hand, considering the medium scale FPGA used at a 100 MHz frequency (corresponding to a period of 10ns), we can evaluate the latencies of the basic blocks. By adding them according to the dataflow, we raised latency of each functional module and thereafter the hardware execution time of the whole APF control unit architecture. As shown in Table III, the response time results for the identification methods are presented and compared each other. So, ITM appears to be the fastest technique with a response time of 0.6 µs when the mp-q is the slowest with a value of 1.34 µs. The reason is that the ITM technique is modeled without the symmetrical component extraction unit and the Concordia/Park transformation. In this way, obtained results in unbalanced conditions are not also good as for the others techniques. In all cases, the response times remain very short

TABLE I. RESULTS FROM THE HARMONICS DETECTION METHODS

Harmonic detection	Settling time	Adequate for single phase	Obtained Source current THD
mp-q	27ms	no	1.92%
ITM	45ms	yes	1.75%
MSRF	20ms	no	1.78%

TABLE II: EVALUATION OF RESOURCE CONSUMPTION FOR THE IDENTIFICATION METHODS

Resources	Available	FPGA resources in %		
		MSRF	*ITM*	*MP-Q*
ALUT	143,520	4%	32%	17%
Memory (RAM)	9,383,040	4	24	8
9-bits DSP	768	57	100	99
Register blocks	147,818	0.6	2.6	0.50
Pins	783	11	11	11
PLL	12	8	8	8
Average *(RAM+DSP+ALUT)* **consumption**		21.6%	52%	41.33%

TABLE III. RESPONSE TIME OF THE APF CONTROL UNIT ARCHITECTURE EVALUATION

Module	*Execution time* (µs)		
	SRFM	*ITM*	*MP-Q*
phase detection	0.27	0.27	0.27
symmetrical component	-	-	0.49
concordia/Park transform	0,16	-	0.16
dc components	0,12	0,12	0.1
Inverse Concordia/park transform	0,14	-	0.25
other multipliers		0.14	
current control	0.07	0.07	0.07
Response time	**0.76**	**0.6**	**1.34**

and this confirms choice of a FPGA target especially in implementing neural based architectures.

IV. EXPERIMENTAL RESULTS

As can be seen in Fig. 5, we used an experimental platform including a three-phase APF, a three-phase power supply, a nonlinear load, a computer, and the control unit built from the FPGA board associated with an analog inputs card. The power stage consists of a Semikron SKM 50 GB 123D inverter with insulated-gate bipolar transistor (IGBT) modules. The split capacitor of the DC bus is 4400µF and R-L branches are applied to suppress the filter current ripple. Such a design can operate at a line-to-neutral voltage of 230V rms and 10-kVA power.

APF control unit implementation with a unique FPGA is possible without association with a DSP as it is almost always the case. An auxiliary card is used for assuring acquisition and A/D conversion of the current and voltage signals for the FPGA, and also to amplify the gating signals from 0-3.3V to 0-15V needed by IGBTs. ADCs are simultaneously controlled at a sampling frequency of 5 MHz from the FPGA. The nonlinear load is made up of a diode rectifier and a R-L branch in the DC side. Due to real-time constraints, the switching frequency of the IGBT has been set to12.5 kHz which is adequate for this application. The system parameters are summarized in Table IV where *Vs* is the line source voltage, *f* is the system frequency, V_{DC} is the voltage of the DC bus capacitor C_{DC}, R_f *and* L_f are respectively the filter resistance and inductance, f_{sw} is the switching frequency, R_L *and* L_L are respectively the load resistance and inductance.

First, experimental study is made for *ITM* and *MSRF* harmonics detection methods. Fig. 6 shows the waveforms for balanced and nonlinear load. These waveforms are obtained after reducing the 230V source voltage by a transformer. The source voltage, the load current, the compensating current and

TABLE IV. SYSTEM PARAMETERS

Power source	Values
Vs, f	40V, 50Hz
Active power filter	Values
V_{DC}, C_{DC}	85V, 4400µF
R_f, L_f	5Ω, 5.8mH
f_{sw}	12.5Khz
Non linear load	Values
R_L, L_L	20Ω, 15.4mH

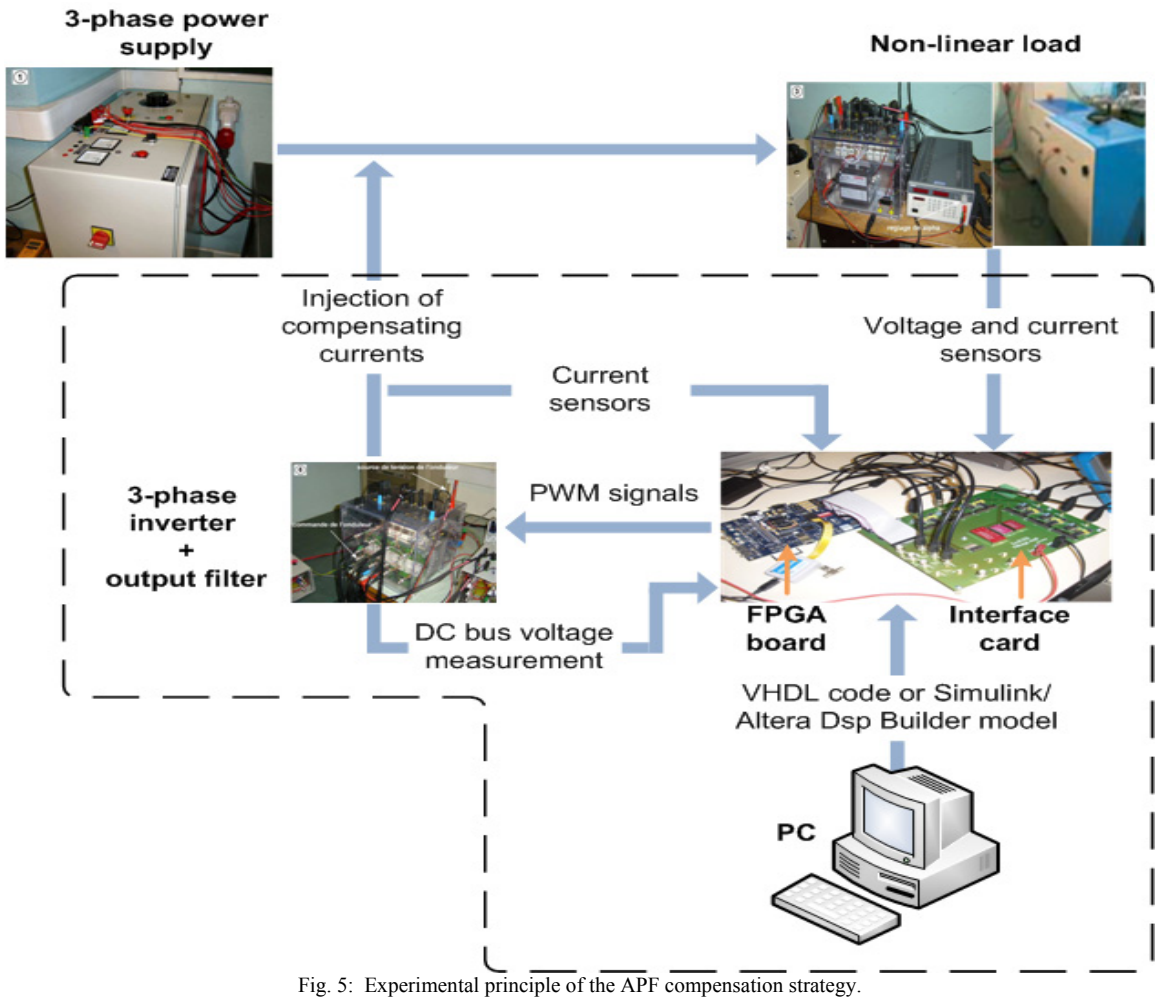

Fig. 5: Experimental principle of the APF compensation strategy.

the source-side current after compensation are shown in top-to-bottom order. Harmonics spectra of the compensated source current and load current are represented in Fig. 7. We can see that all harmonic components are cancelled to obtain good sinusoidal source currents in phase with the voltage signal so as to correct the power factor of the supply current near to unity. It can also be seen from Fig. 8 that the designed adaptive shunt APF can adapt to a change in the non-linear load current. When non linear load values change from (R_L=20Ω, L_L=15.4mH) to (R_L=6.55Ω, L_L=20mH), we still obtain good filtering performance. The reference current waveforms extracted from the load current are quite similar for the different methods especially in balanced conditions (mp-q, MSRF and ITM). Table V shows the THD of the source-side current after the APF compensation for an initial THD of 30%. The best result is obtained for the mp-q

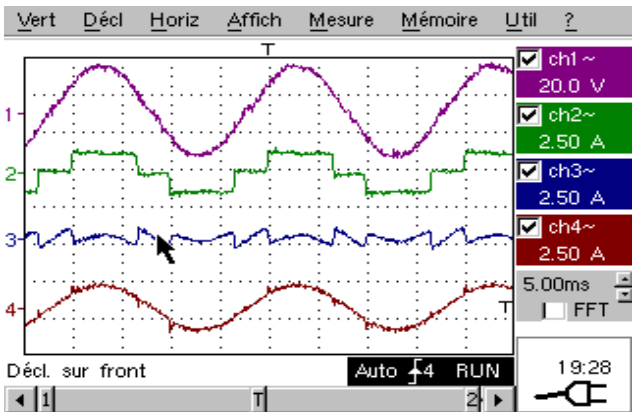

Fig.6. Experimental results for ITM and MSRF methods: 1) source voltage 2) load current 3) reference current, 4) source-side current after compensation

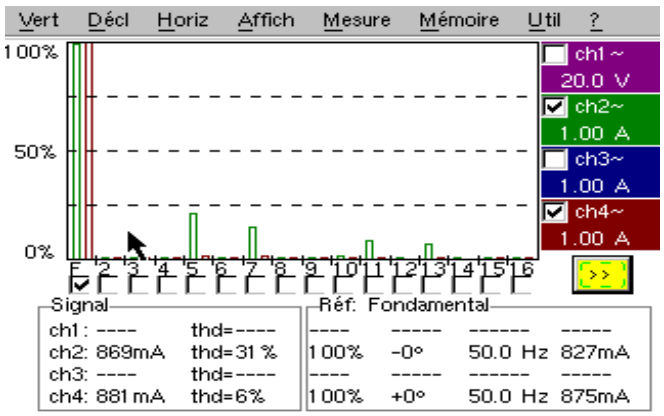

Fig.7. Spectral decomposition of the source-side current before and after compensation

method with a THD of 3.3%. All the THD values, even the one for the ITM method can be significantly reduced by choosing an APF output filter of third order to fit the source current inside the distortion bounds set at 5% by the standards. The results have confirmed very good performance in terms of waveform quality and response time.

V. CONCLUSION

Experimental results of distortions compensation through the APF have been presented and confirm those obtained after simulation in various utility conditions. The APF control unit was implemented on a unique target, i.e a FPGA Stratix II available on a development board which worked in association with an analog inputs card. A comparative study was presented after simulation and Hardware implementation of three adaptive distortions identification techniques based on neural networks. Whatever the harmonic detection method used, we can argue that it is possible to obtain the compensated source current THD value which agrees with IEC standards. In addition to the APF performances, even the most consuming ITM method presents interesting perspectives in terms of FPGA material resources reduction by consuming less than 52% of FPGA calculation resources.

So, with appropriate design, mapping the algorithm with adequate system performance is reachable despite the lack of resources. Despite MSRF distortion identification has the fastest response in simulation, i.e., a settling time of 20ms, the smallest resource utilization ratio, i.e., 21.6%, and practically the smallest execution time after hardware implementation for three-phase compensation, the mp-q technique appears as one of the best harmonics identification strategy for its filtering aptitudes with an experimental source-side current THD of 3.3% after compensation. Moreover, its results are still interesting under unbalanced conditions.

Although other methods for the control of APF are widely known, the hardware implementation of the whole APF control unit with only neural networks is an interesting issue.

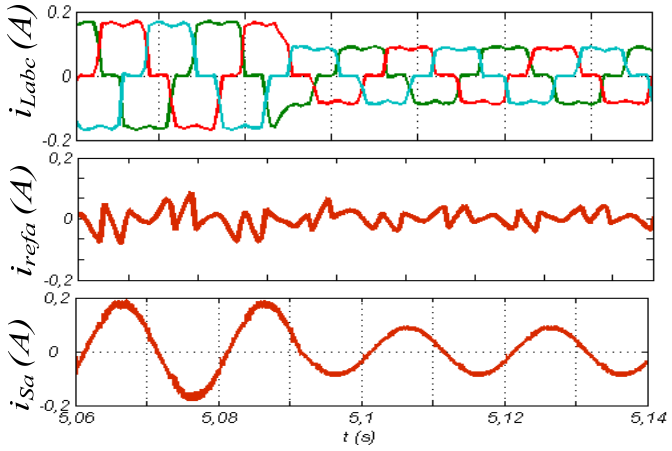

Fig. 8. Experimental results for the mp-q method - 1) three-phase load current 2) Single phase reference current, 3) source-side current after compensation

TABLE V. THD OF THE GRID CURRENT UNDER SINUSOIDAL VOLTAGE CONDITIONS AFTER THE CONNECTION OF THE APF

Harmonics extraction method	THD after compensation
mp-q	3.3%
ITM	7%
MSRF	6%

The use of FPGA target for such applications certainly improves the global performances due to its aptitudes for parallel processing.

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