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Abstract: The recent introduction of silicon-germanium (SiGe) alloys has proven exceptionally promising for achieving excellent bipolar transistor performance at cryogenic temperatures, while maintaining the cost and yield advantages traditionally associated with silicon (Si) manufacturing. In this paper we review the features of silicon-germanium heterojunction bipolar transistors (SiGe HBTs) which make them particularly suitable for cryogenic operation. Using *dc* and *ac* experimental results, we also address the issues associated with profile optimization of SiGe HBTs for the cryogenic environment, the potential for cryogenic SiGe BiCMOS technologies, and present new results on liquid-helium temperature operation of SiGe HBTs. We conclude that SiGe HBT technology offers significant leverage for future cryogenic digital, analog and mixed-signal applications requiring the highest levels of performance.

1. INTRODUCTION

Si bipolar technology, despite its desirable features of fast switching speed, high transconductance, and excellent current-drive capability at room temperature (RT = 300K), is often viewed as unsuitable for the cryogenic environment because its current gain ($\beta = J_C / J_B$), frequency response, and circuit speed typically degrade with cooling [1,2]. Recent evidence [3-6] indicates, however, that careful profile design can be used to achieve respectable Si bipolar performance down to liquid-nitrogen temperature (LNT = 77K). Even with these improvements, however, it is unlikely that conventionally designed Si bipolar technology will offer performance attractive enough to make it a serious contender to CMOS, a proven technology for cryogenic applications.

The recent introduction of epitaxial SiGe alloys has the potential to change this situation dramatically. Because of its bandgap-engineered base, the SiGe HBT is particularly well-suited to operation at cryogenic temperatures [7-10]. As can be seen from the trends shown in Figures 1 and 2, at present SiGe HBT technology is capable of producing transistors with higher current gain at LNT than RT, and unloaded ECL circuits which are as fast at LNT as they are at RT. Development of SiGe HBT technology has progressed very rapidly, and is being actively pursued by a number of groups around the world [11-23]. Highlights from the evolution of SiGe HBT technology include: the first demonstration of a SiGe HBT in 1987 [11], the announcement of a 75 GHz f_T non-self-aligned SiGe HBT in 1990 [12], and the report of a full SiGe ECL-BiCMOS technology which integrated 60 GHz f_{max} SiGe HBTs with state-of-the-art 0.25 μm CMOS in 1992 [13]. In 1993, effort was aimed at exploiting the unique capabilities of SiGe HBT technology for very-high-performance analog applications, resulting in the demonstration of a 1.0 GS/sec 12-bit digital-to-analog converter [14]. Recent work suggests that the ultimate performance of SiGe technology will be in the above-100 GHz regime, comparable to more expensive III-V

semiconductor technologies such as GaAs [15,16]. SiGe growth techniques are maturing quickly, and are nearing the point at which reliable manufacturing on 200 mm wafers can be considered practical [24]. While the immediate focus of SiGe HBT technology has clearly been on realizing commercially viable RT hardware, cryogenic applications will naturally follow.

To date, SiGe HBT technology optimized specifically for cryogenic temperatures has achieved current gains of 500, peak cutoff frequencies in excess of 60 GHz, and unloaded ECL gate delays below 22 psec at LNT [25]. In all cases, these performance levels are significantly better than those of the same technology operated at RT, and are vastly superior to what can be achieved in conventional Si bipolar technologies at cryogenic temperatures. The integration of SiGe HBT technology with aggressively scaled CMOS to form a SiGe BiCMOS technology can thus be expected to provide very attractive system performance at cryogenic temperatures on a realistic power budget for high-performance digital, analog, or mixed-signal applications.

In this paper we review the basic physics of the SiGe HBT, with particular emphasis on its unique cryogenic capabilities, discuss the realization of an optimized LNT SiGe HBT technology using the UHV/CVD growth technique, and present experimental results demonstrating the performance potential of such technologies at cryogenic temperatures. In addition, we will address the potential for a high-speed SiGe BiCMOS technology operating at LNT, as well as show new data on SiGe HBT operation at temperatures as low as liquid helium temperature (LHeT = 4K).

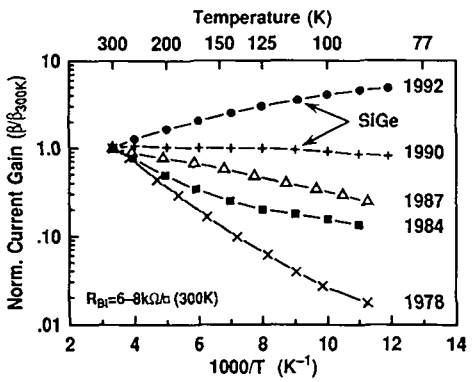

Fig. 1. Trends in current gain as a function of temperature for Si-based bipolar technologies.

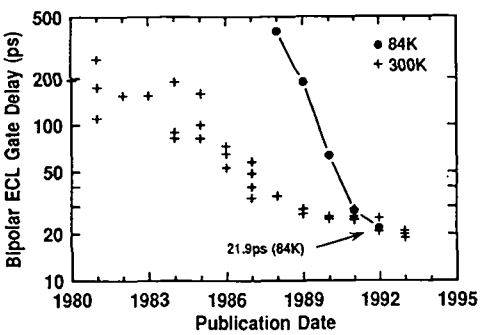

Fig. 2. Trends in unloaded ECL gate delay at 300 K and 84 K for Si-based bipolar technologies.

2. SiGe HBT OPERATION AT CRYOGENIC TEMPERATURES

In a conventionally designed Si bipolar junction transistor (BJT), the temperature dependence of the current gain (β) is to first order determined by the difference in doping-induced bandgap narrowing between the emitter and base regions according to:

$$\beta_{Si}(T) \propto e^{-(\Delta E_{ge} - \Delta E_{gb})/kT} \propto e^{-E_o/kT} \quad (1)$$

where ΔE_{ge} is the bandgap narrowing associated with the emitter region, and ΔE_{gb} is the bandgap narrowing associated with the base region. Because the Si BJT is designed with an emitter doping level much higher than the base doping level to enhance the emitter injection efficiency, the current gain is an exponentially decreasing function of temperature, resulting in a degraded current gain at 77K.

From a *dc* standpoint, the smaller base bandgap resulting from the presence of Ge in a SiGe HBT compensates the bandgap narrowing associated with the high emitter doping to give a current gain which is larger than that of a Si BJT. The presence of Ge in the base can have a much more profound effect at low temperatures than at room temperature, since the minority electron injection is exponentially dependent on the ratio of the bandgap decrease due to the Ge and the thermal voltage. Consequently, even small bandgap reductions (roughly 75 meV for 10% Ge) can lead to very large and beneficial device parameter changes at low temperatures. Consider, for instance, a device with a triangular Ge profile. In this case, for the same emitter contact technology and base doping level, the current gain in a SiGe HBT is enhanced over a Si BJT in low-injection by approximately,

$$\frac{\beta_{SiGe}}{\beta_{Si}} = \left\{ \frac{e^{\Delta E_{g,Ge}(x=0)/kT}\, \Delta E_{g,Ge}(grade)/kT}{1-e^{-\Delta E_{g,Ge}(grade)/kT}} \right\} \tag{2}$$

where x=0 is the emitter-base (EB) edge of the neutral base, and $\Delta E_{g,Ge}$ (grade) = $\Delta E_{g,Ge}$ (x=W_B) - $\Delta E_{g,Ge}$ (x=0). Hence, for a SiGe HBT, current gain at low temperatures depends exponentially on the bandgap reduction at the EB edge of the quasi-neutral base and thus can in principle be easily made as large as desired, subject to the stability constraints on the SiGe film.

The primary dynamic consequence of using a graded bandgap SiGe base is an improvement in the base transit time (τ_B), typically the limiting factor in the transistor frequency response. The Ge grading induces a drift-field in the base (typically 15-20 kV/cm) which aids minority electron transport. For a transistor with a triangular Ge profile, the temperature dependent improvement in τ_B of a SiGe HBT compared to a Si BJT can be expressed as,

$$\frac{\tau_{B,SiGe}}{\tau_{B,Si}} = \frac{2\ kT}{\Delta E_{g,Ge}(grade)} \left\{ 1 - \frac{kT\left(1-e^{-\Delta E_{g,Ge}(grade)/kT}\right)}{\Delta E_{g,Ge}(grade)} \right\} \tag{3}$$

Equation (3) indicates that the base transit time ratio is favorably effected by cooling. This improvement in base transit time with cooling is important because it offsets the reduction in electron diffusivity at low temperatures ($D_{nB} = \mu_{nB}$ kT/q), and thus produces a better frequency response at LNT than at RT. With the superior freeze-out properties of epitaxial base profiles, this improved frequency response can be expected to translate directly into superior cryogenic circuit performance [9,10], as will be demonstrated experimentally in the next section.

3. OPTIMIZATION OF SiGe HBT TECHNOLOGY FOR CRYOGENIC OPERATION

During our previous studies of SiGe HBTs for LNT applications, we identified a number of key design issues which must be properly accounted for when optimizing the SiGe HBT explicitly for the LNT environment [9,10]. These LNT design issues include: 1) the increased importance of parasitic EB tunneling current at LNT compared to RT, 2) the minimization of carrier freeze-out in the base under the constraints of issue 1), 3) designing the collector profile to leverage the increases in Kirk knee current density with cooling, 4) accounting for the effect of Ge-grading on current gain, and 5) designing around LNT SiGe-Si heterojunction barrier effects at the collector-base (CB) junction under high injection. The epitaxial "emitter-cap" design introduced in [25] represents a SiGe HBT design which addresses these uniquely low-temperature issues, and thus can be considered optimized for LNT operation.

The emitter-cap SiGe HBT uses a planar, self-aligned structure (Figure 3) and was fabricated with deep-trench and shallow-trench isolation [26]. A 40 nm epitaxial "emitter-cap" layer doped with phosphorus at approximately $1x10^{18}$ cm^{-3} was deposited *in-situ* in an ultra-high vacuum / chemical vapor deposition (UHV/CVD) tool [27] on top of the SiGe-base to form the EB junction [28]. It is important to

emphasize that while the idea of using a lightly-doped emitter structure in SiGe HBTs is not new, the present emitter-cap SiGe HBT is made in a unique, highly-integrated, self-aligned structure. Because carrier tunneling processes depend exponentially on the peak junction field, the lightly-doped emitter cap is expected to minimize the parasitic EB tunneling current at LNT compared to a conventional SiGe HBT design (by "conventional" we mean an i-p-i SiGe design optimized for RT applications [9,10]). During device processing ion-implantation was used to form a heavily-doped, self-aligned extrinsic base contact, which was later silicided to minimize base resistance.

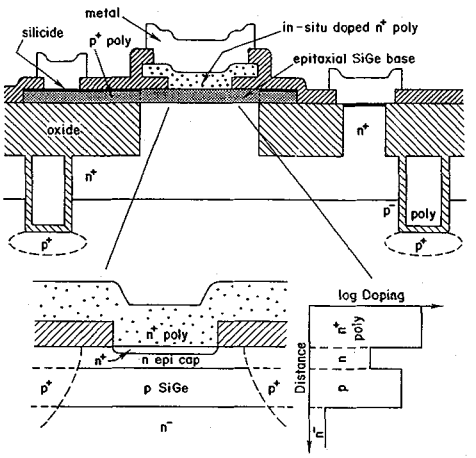

Fig. 3. Schematic device cross section of the emitter-cap SiGe HBT.

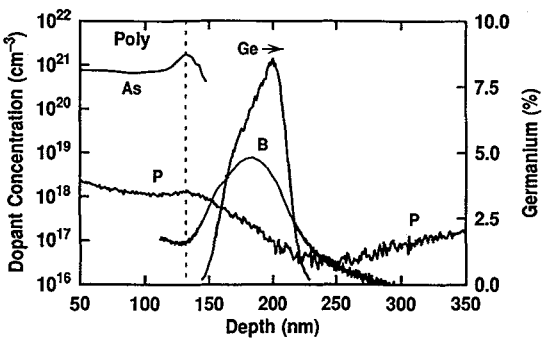

Fig. 4. Doping profile of the emitter-cap SiGe HBT as measured by SIMS.

Because of the increase in carrier saturation velocity with cooling as well as the presence of velocity overshoot in the CB space-charge region at LNT, the onset current density of base push-out (Kirk effect) is larger at LNT than at RT [7]. Thus, compared to a RT design, the collector doping level can be decreased in an optimized LNT profile. In the present work, the doping level at the metallurgical CB junction was decreased from $1x10^{17}$ cm^{-3} for the conventional design to about $2x10^{16}$ cm^{-3}, and ramped upward toward the sub-collector to minimize freeze-out deep in the neutral collector. This LNT collector profile is used to reduce the parasitic CB capacitance under the constraint that the onset current density of the SiGe-Si heterojunction barrier be above the maximum operating current density of about 1.0 $mA/\mu m^2$.

To ensure a low emitter resistance, an *in-situ* doped polysilicon contact with a buried diffusion source was deposited on top of the composite EB profile (n^+ poly / n-cap / p-SiGe). Because the arsenic out-diffusion is used only to contact the epitaxial phosphorus emitter and does not determine the metallurgical EB junction (Figure 3), only a very short rapid thermal annealing (RTA) step is required to activate and redistribute the dopants. To minimize minority carrier charge storage in the emitter-cap layer, a large LNT β is desirable ($\tau_E \propto 1 / \beta_{ac}$). Thus, a trapezoidal Ge profile with a high Ge concentration at the EB junction compared to the i-p-i design was used. The resultant Ge profile satisfied the thermodynamic stability criteria for UHV/CVD blanket films [29]. Representative secondary ion mass spectroscopy (SIMS) data is shown in Figure 4.

Figure 5 shows the current-voltage characteristics of a 0.7x4.4 μm^2 circuit transistor at 310 K and 84 K. Table I gives typical parameters for this transistor at 310 K and 84 K, and for completeness compares the present results to those of the more conventional *i-p-i* SiGe HBT design [9,10]. The higher Ge concentration at the EB junction, the beneficial effects of the emitter *high-low* (n^+ / n-cap) junction [5], and the bandgap narrowing of the heavily doped base, offset the bandgap narrowing of the heavily doped emitter region to give a β which increases rapidly with cooling from 102 at 310 K to 498 at 84 K (Figure 6). This large β value at LNT serves to minimize the unwanted charge storage associated with the emitter cap layer as well as to circumvent the degradation of β at medium injection levels due to bias-dependent Ge ramp effects [30], giving a desired β of 99 at a collector current density of 1.0 $mA/\mu m^2$. An

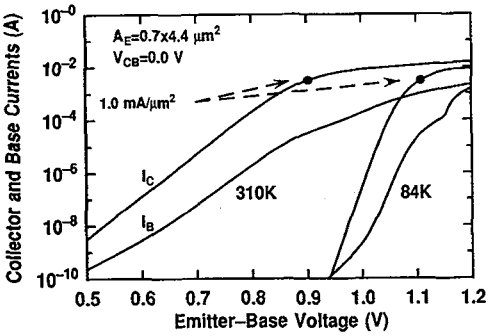

Fig. 5. Current-voltage characteristics of an emitter-cap SiGe HBT at 310 K and 84 K.

SiGe Profile		emitter cap design		i-p-i design	
Temperature		310 K	84 K	310 K	84 K
β_{MAX}	(J_C/J_B)	102	498	105	82
β at 1 mA/μm²		94	99	96	34
R_{BI}	(kΩ/□)	7.7	11.0	8.2	15.9
R_E	(Ω μm²)	44	34	26	23
I_{EB} at –1.0V	(nA)	$8.44x10^{-3}$	$1.91x10^{-3}$	2.89	1.11
BV_{CEO}	(V)	3.1	2.3	3.2	3.2
BV_{CBO}	(V)	10.8	9.6	10.8	9.5
C_{EB}	(fF/μm²)	5.47	5.13	6.30	5.90
C_{CBX}	(fF/μm²)	0.46	0.40	1.04	0.93
Peak f_T	(GHz)	43	61	53	59
Peak f_{max}	(GHz)	40	50	37	48

Table I. Measured transistor parameters of an emitter-cap SiGe HBT compared to an i-p-i SiGe HBT of comparable size at 310 K and 84 K.

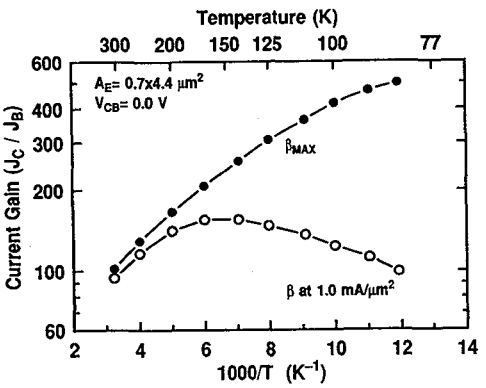

Fig. 6. Current gain as a function of temperature for the transistor shown in Figure 5.

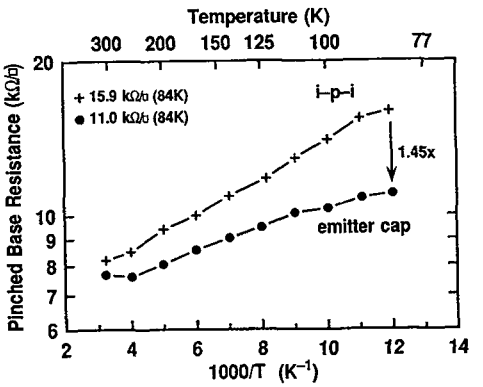

Fig. 7. Freeze-out properties of the pinched-base sheet resistance at zero-bias comparing the emitter-cap SiGe profile to the i-p-i SiGe profile.

undesirable result of the high β at LNT is a decrease in the BV_{CEO} from 3.1 V at 310 K to 2.3 V at 84 K, but at LNT BV_{CEO} remains acceptable for most circuit applications.

The 0.7x4.4 μm² circuit transistor achieves a peak extrinsic transconductance (g_m) of 133 mS at 84 K. The best reported g_m for a silicon MOSFET has a normalized value of 1040 mS / mm at 85 K for a 0.05 μm L_{eff} nFET at 1.5 V [31]. If we consider the available g_m for a given transistor to be a meaningful figure-of-merit, then it is instructive to note that to obtain the equivalent total g_m as the SiGe HBT at LNT (designed at 0.70 μm lithographic groundrules), the 0.05 μm nFET would have to be designed with a W_{eff} = 108.7 μm, or a W/L of 2173!

The reduction in overall thermal cycle compared to a conventional i-p-i design is key to maintaining the heavily-doped, as-deposited boron base profile, and thus providing immunity to carrier freeze-out at LNT. For this profile, the pinched-base sheet resistance only increases from 7.7 to 11.0 kΩ/□ between 310 K and 84 K (Figure 7). Importantly, this immunity to base freeze-out does not come at the expense of increased EB leakage (as it does for instance in a spacer-free *p-i* SiGe profile with a very heavily doped base [9]). The lower doping level of the emitter-cap layer results in a reverse EB leakage at 1.0 V at 84 K which is more than 500 times smaller than for the conventional *i-p-i* SiGe design (Table I). The consequence is a much smaller forward tunneling component in the base current (larger low-current β), a smaller EB capacitance, and an expected improvement in LNT hot-carrier reliability.

As shown in Figure 8, the transistor cutoff frequency (f_T) rises from 43 GHz at RT to 61 GHz at LNT due to the beneficial effects of the Ge-grading-induced drift field (equation 3). This improvement

in f_T, coupled to the low total base resistance, and slightly decreased CB capacitance, yields an increase in maximum oscillation frequency with cooling as well, from 40 GHz at 310 K to 50 GHz at 84 K for the device shown in Figure 8. To assess the LNT circuit capabilities of this technology, unloaded ECL ring oscillators were measured (Figure 9). ECL circuits switch at a record 21.9 psec at 84 K, 3.5 psec faster than at RT, and show a substantial improvement in temperature dependence over an i-p-i design with comparable emitter area (Figure 10). Circuit models were built and calibrated to data in order to examine circuit operation under conditions which were not directly measurable. Of particular interest is the impact of reduced logic-swing operation [6] as well as the improved metal conductivities on the circuit delay in more realistic loaded situations at LNT. Figure 11 shows the simulation results of RC-loaded circuits for a power dissipation of 5.65 mW under 500 mV logic-swing at 310 K and 300 mV logic-swing at 84 K. Observe that while the 310 K and 84 K unloaded delays (0 mm wire length) are nearly identical, at long wire lengths the 84 K delay is substantially faster than the 310 K result (by 2.7x at 10 mm wire length). Thus, under realistic system loading conditions, a high-performance SiGe HBT technology is capable of achieving dramatic reductions in delay compared to a RT technology.

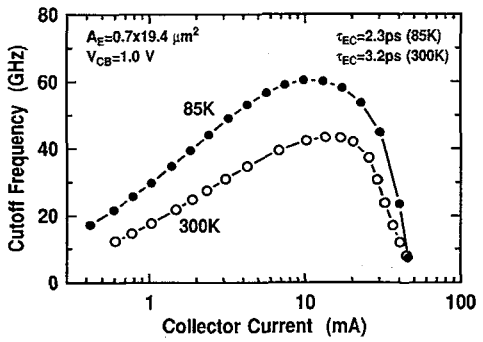

Fig. 8. Cutoff frequency as a function of collector for an emitter-cap SiGe HBT at 300 K and 85 K.

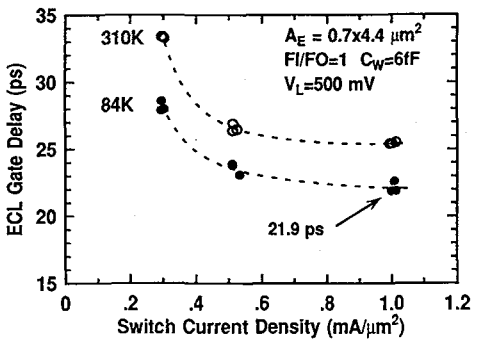

Fig. 9. Unloaded ECL gate delay as a function of switch current density for the emitter-cap SiGe HBT technology at 310 K and 84 K.

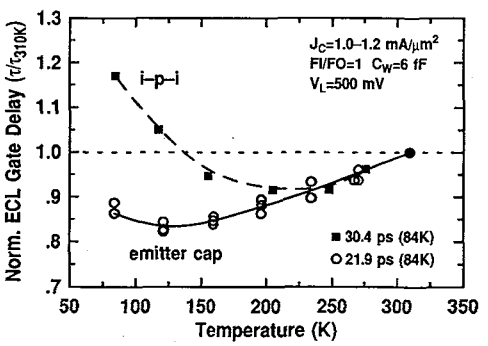

Fig. 10. Temperature dependence of the unloaded ECL gate delay comparing the emitter-cap SiGe HBT technology to the i-p-i SiGe HBT technology.

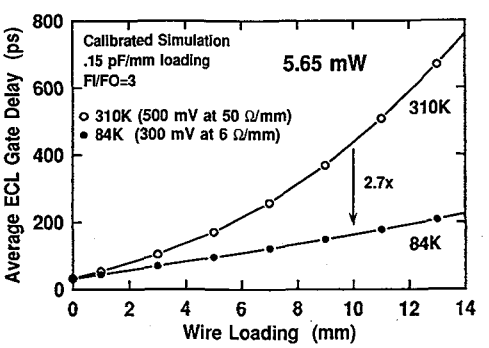

Fig. 11. Simulated ECL gate delay as a function wire loading at 310 K and 84 K. Delay results are calibrated to unloaded ring oscillator data at both temperatures.

4. CRYOGENIC SiGe BiCMOS

With the increasing emphasis being placed on power minimization and portability in RT systems, the integrated circuit industry is clearly shifting its focus from bipolar-only technologies towards BiCMOS implementations. This is particularly true for digital applications requiring fast loaded circuits together with

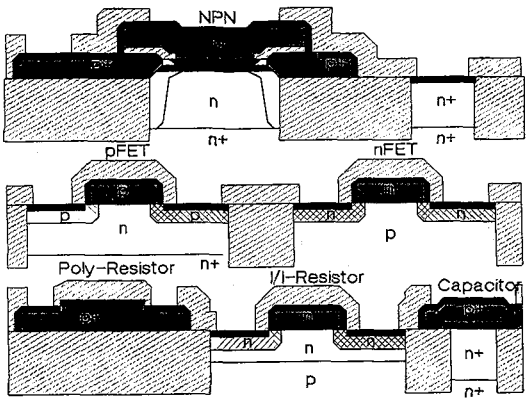

Fig. 12. Schematic cross section of SiGe BiCMOS technology.

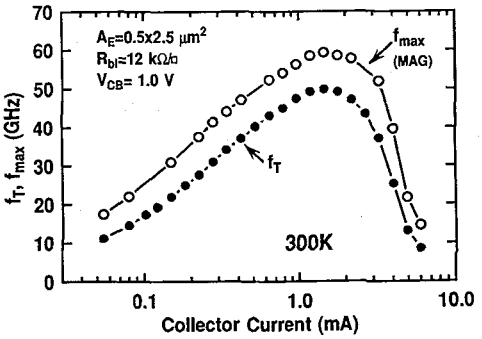

Fig. 13. Measured frequency characteristics at 300K of the 0.5μm SiGe-HBT from the SiGe ECL-BiCMOS technology.

high integration levels. Power dissipation is clearly an even more serious design constraint in cryogenic systems, where cooling capacity is limited and expensive. Hence, if SiGe HBT technology is to play any major role in future cryogenic systems, it appears critical that it take the form of a SiGe BiCMOS technology. In this case the SiGe HBT would be used in selected areas to maximum advantage without incurring excessive cooling burden. Examples for potential uses of the SiGe HBT in cryogenic systems might include: logic in critical signal paths, on-chip and off-chip drivers, sensing circuits, analog applications such as high-bandwidth amplifiers, RF and microwave components, and high-speed D/A and A/D conversion, as well as critical mixed-signal elements. The CMOS devices, with their superior power-delay performance, could then be used for the remaining functions requiring lower performance and/or higher density. Thus, rather than a conventional BiCMOS logic, which becomes difficult to implement at low supply voltages, we envision the use of cryogenic bipolar circuits plus CMOS circuits on a chip. The intent would be to use each device independently to maximum advantage.

The SiGe HBT structure described in the present work was in fact designed to easily integrate with conventional CMOS technology. Recent attempts to realize the type of SiGe BiCMOS envisioned here have been successful, with quite impressive results. Figure 12 shows a schematic cross section of a SiGe BiCMOS technology [13]. This technology integrates advanced 0.25 μm CMOS with 0.50 μm SiGe HBTs, as well as passive elements such as polysilicon resistors, ion-implanted resistors, and thin-oxide capacitors. Importantly, the performance of the SiGe HBT was not compromised to achieve this high level of integration. Figure 13 shows the RT frequency response of a 0.5x2.5 μm² circuit transistor. A record peak f_{max} of 60 GHz was achieved, together with an unloaded ECL gate delay of 19 psec. The CMOS devices also exhibit state-of-the-art performance, with a saturated g_m of 227 mS/mm and 140 mS/mm at 2.5 V at RT for the 0.25 μm nFET and pFET devices, respectively. While the cryogenic performance of this SiGe BiCMOS technology has not at present been measured, the SiGe HBT has been fabricated with the LNT-optimized emitter cap profile discussed above. Thus, there is every reason to believe that the low-temperature performance of both the SiGe HBT and the CMOS will be excellent.

5. HELIUM-TEMPERATURE RESULTS

While excellent SiGe HBT performance down to LNT has been clearly demonstrated, certain cryogenic applications such as long wavelength infrared (LWIR) detector and imaging systems often require temperatures below 77 K. We have recently reported the first measurements of SiGe HBTs down to temperatures as low as liquid-helium [32]. The optimized emitter-cap SiGe HBTs described above continue to behave as transistors, with useful current gain, high transconductance, and large output current-drive, down to the LHeT regime, even in the presence of strong carrier freeze-out in the neutral base and

collector regions (Figure 14). In contrast to measurements of Si bipolar transistors, the peak current gain in the SiGe HBT rises from 100 at 300 K to nearly 2000 at 16 K, although parasitic base current leakage limits the useful operating range to collector currents above about 1.0 μA (Figure 15). Comparison of these results on the LNT-optimized emitter cap SiGe HBT to the i-p-i SiGe HBT show that Ge profile design is more critical to maintenance of adequate current gain at LHeT than at LNT (Figure 16), although even with the i-p-i SiGe HBT design, peak current gains above 35 down to 6 K have been achieved.

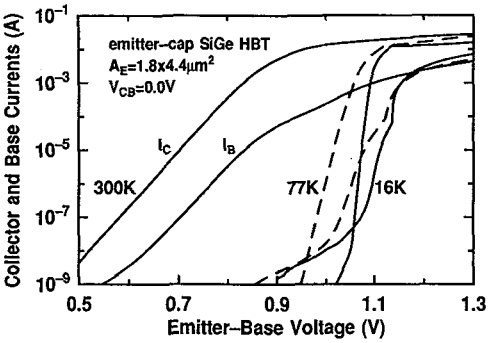

Fig. 14. Current-voltage characteristics of an emitter-cap SiGe HBT at 300 K, 77 K, and 16 K.

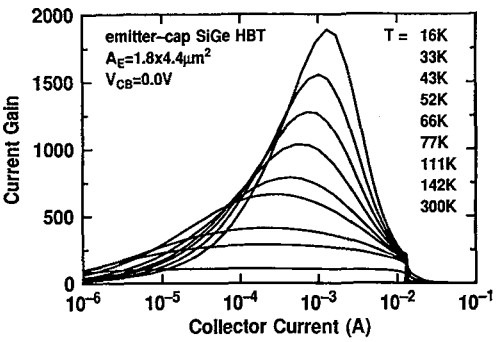

Fig. 15. Current gain as a function of collector current for temperatures down to 16 K for the transistor shown in Figure 14.

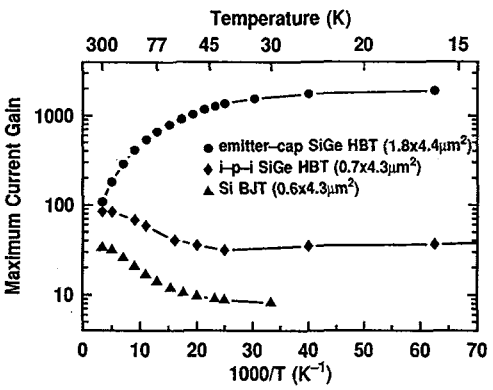

Fig. 16. Maximum current gain as a function of temperature for an emitter-cap SiGe HBT, an i-p-i SiGe HBT, and a Si BJT down to 15 K.

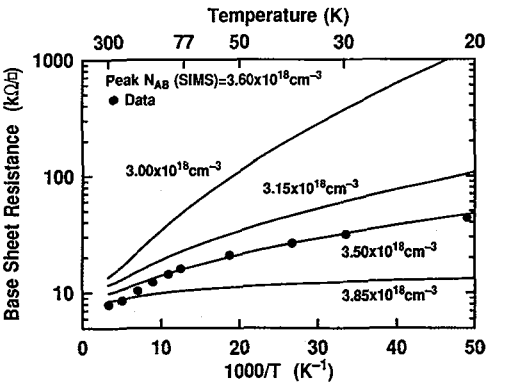

Fig. 17. Measured pinched-base sheet resistance at zero-bias for an i-p-i SiGe HBT down to 20 K compared to simulations using SCORPIO.

One of the most important parameters limiting the dynamic performance of bipolar circuits at cryogenic temperatures is the base resistance. To assess the impact of carrier freeze-out on base resistance at temperatures below 77 K, measurements of the pinched-base sheet resistance at zero-bias of the i-p-i SiGe HBT were made down to 4.6 K. The results down to 20 K are shown in Figure 17. The pinched-base sheet resistance reaches a value of about 96 kΩ/□ at 4.6 K, compared to its initial value of about 8 kΩ/□ at 300 K and modest rise to 16 kΩ/□ at 77 K, indicating that relatively strong carrier freeze-out is occurring in the base region at LHeT. (Although we have not yet measured the pinched-base resistance of the emitter cap SiGe HBT, results from Figure 7 suggest that it will be significantly better at LHeT.) To better understand the profile design constraints associated with maintaining reasonable base sheet resistance at LHeT, we performed simulations based on the actual measured SIMS doping profile data using SCORPIO, a newly developed 1-D SiGe HBT drift-diffusion simulator optimized for convergence at cryogenic temperatures [33]. Reasonable agreement between the measured results and simulation was obtained. To gauge the sensitivity of the base freeze-out properties of this device to the specifics of the

profile design, we also performed simulations with the doping profile uniformly scaled either up or down. Observe in Figure 17 that very modest changes in peak base doping level change the freeze-out properties in the below-77K regime dramatically. For instance, by varying the peak base doping level from $3.85x10^{18}$ cm^{-3} to $3.00x10^{18}$ cm^{-3} spans the range from negligible base freeze-out (8 kΩ/□ at 300 K to 12 kΩ/□ at 20 K) to extremely strong base freeze-out (8 kΩ/□ at 300K to nearly 2 MΩ/□ at 20 K). This strong dependence is not unexpected, given that the peak base doping level is near the Mott transition for boron in silicon (approximately $3.8x10^{18}$ cm^{-3}). While this strong sensitivity to doping level is undesirable since it suggests a very narrow profile design window for a SiGe HBT optimized for LHeT, it also indicates that the abrupt, heavily-doped base profiles made possible by epitaxial growth techniques should be more than adequate for obtaining SiGe HBTs that have little or no base freeze-out down to LHeT. In such a situation, we can anticipate that the performance of SiGe circuits would remain attractive down to LHeT.

One striking feature of all of the transistors measured down to LHeT is that the collector current develops a distinctly non-exponential character at very low injection levels below 77 K (Figure 14). This is unexpected in conventional bipolar device theory, and has not been previously reported. Because the exponential dependence of collector current on emitter-base voltage is fundamentally the result of the drift-diffusive character of the electrons across the base region in a bipolar transistor, it is logical to infer that the observed non-exponential behavior at extremely low temperatures is the result of a different carrier transport mechanism. Initial calculations indicate that the temperature dependence of the observed non-ideal collector current is suggestive of a trap-assisted tunneling mechanism across the potential barrier of the base. In this situation, the measured terminal current would be a parallel combination of the conventional diffusion current and the tunneling current, and thus would explain why the tunneling current occurs only at very low injection levels. It is clear, in any case, that the effect does not depend on the presence of Ge in the base, since it is observed in both SiGe HBTs and Si bipolar transistors, and would thus appear to be fundamental to advanced bipolar transistors operating in this temperature regime. Aside from its obvious interest as a novel device physics problem, the observed non-ideality of the collector current is potentially important for low-current analog applications in the LHeT regime since there is a consequent loss in transconductance associated with the effect.

6. CONCLUSIONS

The recent introduction of SiGe alloys has proven exceptionally promising for achieving excellent bipolar transistor performance at cryogenic temperatures, while maintaining the cost and yield advantages traditionally associated with silicon (Si) manufacturing. At present, SiGe HBT technology optimized specifically for cryogenic temperatures have achieved current gains of 500, peak cutoff frequencies in excess of 60 GHz, and unloaded ECL gate delays below 22 psec at LNT. Under realistic loading conditions typical of the system environment, reductions in logic-swing and wiring resistance at LNT yield dramatic improvements in speed over comparable RT technologies. The integration of SiGe HBT technology with aggressively scaled CMOS in a SiGe BiCMOS technology can thus be expected to provide very attractive system performance at cryogenic temperatures on a realistic power budget for future high-performance digital, analog, or mixed-signal applications.

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