Power reconfigurable receiver model for energy-aware applications

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Amine Didioui[1,2], Carolynn Bernier[1], Dominique Morche[1], and Olivier Sentieys[2]
[1]CEA/LETI - Minatec, Grenoble, France
[2]IRISA/INRIA - University of Rennes 1, Lannion, France

***Abstract*—This paper presents a reconfigurable receiver model whose purpose is to enable the study of reconfiguration strategies for future energy-aware and adaptive transceivers. This model is based on Figure of Merits of measured circuits. To account for real-life RF interference mechanisms, a link quality estimator is also provided. We show that adapting the receiver performance to the channel conditions can lead to considerable power saving. The models proposed can easily be implemented in a wireless network simulation in order to validate the value of a reconfigurable architecture in real-world deployment scenarios.**

I. Introduction

Extending the lifetime of wireless sensor networks (WSN) typically implies minimizing the power consumption of the RF wireless transceiver, often the most power-hungry component of a wireless sensor node. To this end, a recent field of research has proposed to improve the network energy efficiency by dynamically adjusting the transmission power which typically has a high impact on the node's power consumption. An estimation of the link quality is used in order to maintain a "good-enough" link between nodes [1]. However, on the other side of the link, receiver reconfiguration has received much less attention in the literature. Most modern receivers are designed to achieve a minimum signal-to-noise ratio (SNR) when the channel conditions are in worst-case (e.g. noise, interference, multipath). However, when the channel conditions are favorable, the transceiver may consume more energy than required to meet the target minimum bit-error-rate (BER). Since worst-case conditions may be rarely or only periodically experienced in the actual network deployment, a reconfigurable receiver, able to adjust its performance and power consumption to the instantaneous propagation conditions of the signal and interference, could provide considerable power savings.

This idea has already fostered research in the field of circuit design. In [2] the authors propose a reconfigurable low noise amplifier (LNA) with three different levels of performance. The reconfiguration is achieved using an external DAC that controls the supply voltage. Authors in [3] propose a power scalable digital baseband that reduces its power consumption by varying the word length and sampling frequency. In [4] the authors propose to control the power consumption of a receiver by varying the gain and the linearity of a LNA based on the calculated error vector magnitude (EVM).

While this research is indeed invaluable, evaluating the power savings that could be obtained using reconfigurability is difficult since the time-varying signal and interference propagation conditions so highly depend on the WSN deployment scenario. In this work, we propose a reconfigurable receiver model that can be easily implemented in a network simulator in order to validate the benefit of reconfiguration in a realistic environment. Indeed, since reconfigurable receivers are still objects of the future, we expect that this approach will be used to ease their specification and implementation.

II. Reconfigurable Receiver Model

When designing a low power RF receiver, there are a number of architectural design choices that must be made (e.g. Zero-IF or Low-IF architecture, linear or non-linear amplification, analog or digital channel selection, etc.). The receiver chain blocks where reconfiguration can be usefully applied will therefore vary with the implementation and affect the reconfiguration strategy. In this paper, we limit our model to a Zero-IF architecture with digital channel selection. The model could, of course, be adapted to any other receiver architecture. A reconfigurable receiver necessarily includes a number of reconfigurable blocks, a means for calculating a reconfiguration metric, for example a link quality estimator (LQE), and a decision algorithm for applying the reconfiguration strategy. An example of a reconfigurable receiver is presented in Fig.1. The reconfigurable blocks, identified by a red arrow, are the LNA, mixer, voltage controlled oscillator (VCO) and analog to digital converter (ADC). The LQE measurement and decision blocks are implemented in the digital baseband.

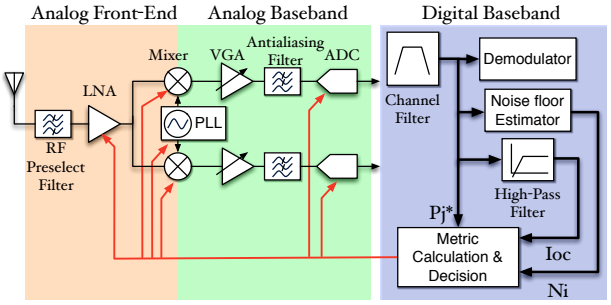

Fig. 1. Architecture of the reconfigurable receiver.

Since the design of power reconfigurable RF and analog blocks is a brand new field of research, the modeling approach adopted for the receiver's reconfigurable blocks is based on the figure-of-merits (FoMs) of measured blocks reported in the literature. We assume that the FoM correctly captures the design space of a given block. For each block, we

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therefore choose an average FoM for a given technology node and deduce the block characteristics for different levels of performance. Our adaptive models can later be refined when more circuits, specifically designed for power adaptability, become available. As a first step, we define three power consumption/performance modes for each block.

A. Reconfigurable LNA and Mixer model

In [5] the FoM_{LNA} is defined as

$$FoM[\text{GHz}] = \frac{G[\text{lin.}] \cdot \text{IIP}_3[mW] \cdot f[\text{GHz}]}{P_{\text{DC}}[mW] \cdot (F[\text{lin.}] - 1)}, \quad (1)$$

where G is the power gain, F is the noise floor, IIP3 is the third-order intercept point, f the operating frequency, and P_{DC} is the power consumption. Based on [6], an average FoM_{LNA} of 15 GHz is chosen. Similarly to the LNA, the $\text{FoM}_{\text{Mixer}}$ is given as [7]

$$\text{FoM}_{\text{Mixer}}[\text{dB}] = 10 \log \left(\frac{G[\text{lin.}] \cdot \text{IIP}_3[mW]}{P_{\text{DC}}[mW] \cdot (F[\text{lin.}] - 1)} \right) \quad (2)$$

Based on [7], an average $\text{FoM}_{\text{Mixer}}$ of -17 dB is chosen. Using (1) and (2), the LNA and mixer characteristics are given in Table I for three performances: high, moderate and low.

TABLE I
LNA AND MIXER PERFORMANCES.

Component	Mode	Pdc [mW]	G [dB]	NF [dB]	IIP3 [dBm]
LNA	High	5.9	16	1.5	-4
	Moderate	1	14	2.8	-6.5
	Low	0.1	12.5	6	-9.8
Mixer	High	3.5	10	14.5	-7
	Moderate	1.2	9	15	-11
	Low	0.2	7	16	-15.5

B. Reconfigurable VCO Model

The contribution of the VCO power consumption can be up to 78% in some modern frequency synthesizer designs [8]. The power consumption of a VCO is usually inversely proportional to its phase noise which, in turn, is responsible for in-channel interference due to reciprocal mixing. Thus, reducing the VCO power consumption in the case of low or inexistent adjacent interferers will result in a reduction of the overall power consumption of the PLL. Of course, the possibility of reconfiguring the VCO assumes that the PLL lock time and stability are guaranteed in each mode. The FoM_{VCO} is

$$\text{FoM}_{\text{VCO}}[\text{dBc/Hz}] = 10 \log \left[\left(\frac{f_c}{\Delta f} \right)^2 \cdot \frac{1}{L(\Delta f) \cdot P_{\text{DC}}[mW]} \right], \quad (3)$$

where f_c is the frequency carrier, Δf is the offset frequency, and $L(\Delta f)$ is the phase noise relative to the carrier measured over a 1Hz bandwidth. From [9], an average FoM_{VCO} of 178 dBc/Hz is chosen. The performance modes of the VCO are summarized in Table II.

TABLE II
VCO PERFORMANCES.

Mode	Pdc [mW]	$L(\Delta f)$ @ 1 MHz [dBc/Hz]
High	5.8	-114
Moderate	3.2	-110
Low	0.1	-95

A -20 dB/decade phase noise slope is assumed until a floor value 10dB inferior to the 1 MHz offset value is reached. The power consumption of other PLL components including the charge pump, filter, divider and the buffer is assumed to be 1.2 mW [8].

C. Reconfigurable ADC Model

In our model, we assume that the ADC is preceded by an anti-aliasing filter that limits the bandwidth to 10 MHz and that ADC has a fixed sampling rate f_{Sampling} of 20 MHz. An average FoM_{ADC} of 167 dB is extracted from data given in [10] assuming a FoM_{ADC} defined as

$$\text{FoM}_{\text{ADC}}[\text{dB}] = (6.02 \cdot \text{ENOB} + 1.76) + 10 \log \left(\frac{f_{\text{Sampling}}}{P_{\text{DC}}} \right) \quad (4)$$

where ENOB is the effective number of bits. Since the signal is oversampled by an approximate factor of 5, the equivalent noise figure of the ADC is given as [11]

$$\text{NF}_{\text{ADC}} = 10 \log \left(1 + \frac{V_{p-p}^2}{6kTR_s L_q^2 f_s} \right) \quad (5)$$

where V_{p-p} is the full-scale voltage, R_s is the reference source resistance, L_q is the number of quantization levels, k is the Boltzmann constant and T the temperature. For V_{p-p} of 1V, the ADC performance modes are summarized in Table III. Note that in this first level model, the additional power savings due to the corresponding dynamic range reconfiguration of the digital baseband are ignored.

TABLE III
ADC PERFOMANCE.

Mode	Pdc [nW]	ENOB [bit]	NF_{ADC} [dB]
High	1.5×10^3	9	28
Moderate	200	6	46
Low	3.5	3	64

D. VGA and antialiasing filter models

In our model, we assume that the variable gain amplifier (VGA) is controlled by an ideal automatic gain control (AGC) algorithm that automatically set the total receiver gain such that the input signal reaches the ADC full-scale voltage. The VGA IIP3 and NF are assumed to be 6 dBm and 25 dB, respectively while the filter IIP3 is fixed at 30 dBm and its NF at 20 dB. The total power consumption of the VGA and

baseband filter (I and Q paths combined) is 2 mW. This first-level model neglects potential power consumption savings that may be obtained when the VGA changes gain setting.

E. Reconfigurable Receiver Model

Assuming that the gain and noise figure values of each block are given for the correct source and load impedances, the overall NF and IIP3 of the receiver is

$$\begin{cases} \text{NF}_{\text{total}} = \text{NF}_1 + \dfrac{\text{NF}_2 - 1}{G_1} + \cdots + \dfrac{\text{NF}_k - 1}{G_1 G_2 \cdots G_{k-1}}, \\ \dfrac{1}{\text{IIP3}_{\text{total}}} = \dfrac{1}{\text{IIP3}_1} + \dfrac{G_1}{\text{IIP3}_2} + \cdots + \dfrac{G_1 G_2 \cdots G_{n-1}}{\text{IIP3}_n}, \end{cases} \quad (6)$$

where NF_i, IIP3_i and G_i are respectively the noise figure, third-order intercept point and power gain for the i^{th} block in the cascade chain. The global performance of the receiver based the models defined above is summarized in Table IV.

TABLE IV
GLOBAL RECEIVER PERFORMANCE.

Mode	Pdc [mW]	NF [dB]	IIP3 [dBm]
High	22.6	4.6	-26
Moderate	10.5	7	-27
Low	4.5	14.7	-29

III. INTERFERENCE MODELING

An ideal reconfigurable receiver continuously adapts its performance in order to avoid wasting power needlessly. At the input of the demodulator, this means that the signal to interference plus noise ratio (SINR) is ideally kept close to the minimum SNR required by the modulation scheme and the minimum acceptable bit-error-rate (BER) defined by the standard. Since the receiver's performance level is voluntarily degraded in order to save power, it is important that the SINR model used in the network simulator correctly accounts for all of the interference mechanisms that can affect the SINR in a real system. While traditional SINR models account only for co-channel interference, a practical system also suffers from adjacent channel interference, intermodulation due to nonlinearity, reciprocal mixing due to phase noise, variable noise floor, etc.

1) Adjacent and co-channel interference: Since a receiver is not infinitely selective, interferers situated in adjacent channels can leave a residual interference power given by

$$P_{\text{Adj}} = \sum_{k \neq i,j} \alpha_{i,k} \cdot P_k \quad (7)$$

where P_k is the power of the k_{th} interferer signal and $\alpha_{i,k}$ is a rejection factor that emulates the channel selectivity of receiver i. A value of $\alpha = 1$ accounts for co-channel interference.

2) Intermodulation interference: The interference resulting from intermodulation is given as [12]

$$P_{\text{IMD}_3} = \sum_{k \neq l,j} \sum_{l \neq k,j} \beta_{i_{(k,l)}} \cdot P_k P_l^2 \quad (8)$$

where P_k and P_l are the received interferers, and $\beta_{i_{(k,l)}}$ is the intermodulation rejection factor expressed as function of the receiver IIP3 and $\alpha_{i,k}$.

3) Phase noise interference: A real VCO generates undesired sideband energy that is referred to as phase noise. This phase noise down-converts adjacent channel interferers into the desired signal band, a process known as reciprocal mixing. The power of interferer signal P_{PN} due to reciprocal mixing is given as

$$P_{\text{PN}}[dB] = P_k[dB] + \{PN(\Delta f) + 10\log(BW)\}[dBm] \quad (9)$$

where P_k is the interferer power, Δf is the offset frequency, $L(\Delta f)$ is the PLL phase noise and BW is the bandwidth of the signal.

4) Global SINR model: An improved SINR model including the impairments of the receiver i is expressed as

$$\text{SINR}_{ij} = \frac{P_j}{N_i + P_{\text{Adj}} + P_{\text{IMD}_3} + P_{\text{PN}}} \quad (10)$$

where P_j is the desired received signal power from emitter j, and N_i is the noise floor of receiver i (N_i[dB] = -174 [dBm/Hz] + $10\log(BW)$ + $\text{NF}_{\text{Receiver}}$[dB]).

IV. RECONFIGURATION METRIC

The fundamental building block to be considered in the process of receiver reconfiguration is the LQE which ideally must provide an accurate estimation of the SINR under all possible channel conditions. Considerable work has been done recently with the aim of establishing accurate link quality estimators. For example, the authors in [1] have classified these techniques in two categories: hardware-based (RSSI, LQI, etc.) and software-based (packet reception ratio (PRR)).

Additionally, it is possible to distinguish between two types of reconfiguration: static – where the receiver's performance mode is determined at the outset and remains the same until the end of the packet reception, and dynamic – where the receiver's performance may change during packet reception. Dynamic reconfiguration allows the receiver to adapt to time-varying interference levels. In this paper, we limit our study to the more difficult case of dynamic reconfiguration. This requires a hardware LQE that allows "instantaneous" dynamic reconfiguration to the receiver performance. Existing receivers provide limited hardware means for estimating link quality. However, future adaptive receivers will obviously need extra components in the analog and/or digital part in order to implement the metric calculation and decision blocks.

In the following we present one possible implementation of the reconfiguration metric which specifically targets a high reactivity and low power overhead. The metric calculation and decision block (Fig.1) measures the power of the in-channel signal P_j^* as well as the residual adjacent interference power.

An estimate of the noise floor, e.g. constructed by monitoring and averaging the in-channel signal strength before or after packet reception, is also an input to the block.

$$I_{oc} = \sum_{k \neq i,j} \alpha_{i,k}|_{\alpha \neq 1} \cdot P_k \tag{11}$$

Since the sum of the in-channel noise is indistinguishable from the desired signal, the total power at the output of the digital channel filter is

$$P_j^* = P_j + N_i + \sum_{k \neq i,j} \alpha_{i,k} \cdot P_k + \sum_{k \neq l,j} \sum_{k \neq k,j} \beta_{i_{k,l}} \cdot P_k P_l^2 + P_{\text{PN}} \tag{12}$$

Since N_i and the residual adjacent channel interference can be extracted from the in-channel signal, the proposed LQE metric is

$$\text{LQE}_{\text{Reconfig}} = \frac{P_j^* - (N_i + I_{oc})}{N_i + I_{oc}} \tag{13}$$

Fig.2 shows the effect of adjacent and alternate interference on the SINR and the $\text{LQE}_{\text{Reconfig}}$ in the case where the receiver is in low performance mode and the desired signal power of -85 dBm. The figure also shows the impact of intermodulation on the SINR and the $\text{LQE}_{\text{Reconfig}}$.

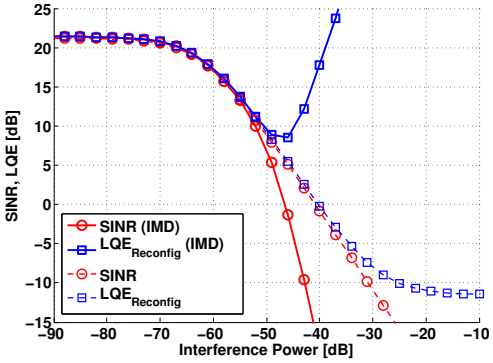

Fig. 2. Variation of the reconfiguration metric $\text{LQE}_{\text{Reconfig}}$ and the SINR as function of interference power.

In order to ensure an acceptable BER in each receiver mode, we define two thresholds: $\text{LQE}_{\text{Low}}^{th}$ corresponds to an SINR of 3dB and $\text{LQE}_{\text{High}}^{th}$ corresponds to an SINR of 9 dB.

V. Evaluation of Power Saving

During packet reception the *"metric calculation & decision"* bloc continuously calculates the metric, if the calculated $\text{LQE}_{\text{Reconfig}}$ is greater than $\text{LQE}_{\text{High}}^{th}$, the receiver performance is switched to low mode performance, otherwise, in the case where the calculated $\text{LQE}_{\text{Reconfig}}$ is below $\text{LQE}_{\text{Low}}^{th}$, the receiver performance is switched to high performance mode. However, when the $\text{LQE}_{\text{Reconfig}}$ is between $\text{LQE}_{\text{High}}^{th}$ and $\text{LQE}_{\text{Low}}^{th}$ the receiver stays in moderate mode. Fig.3 shows the variation of the receiver power consumption as function of the interference and desired signal power.

In Fig.3, it can be seen that the receiver power consumption can be reduced from 22.6 mW to 4.5 mW when there is no interference and high signal power signal power P_j^* (high $\text{LQE}_{\text{Reconfig}}$).

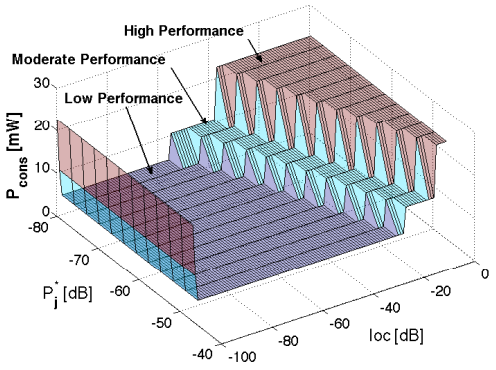

Fig. 3. Variation of receiver power consumption as function of the desired signal and interference power.

VI. Conclusion

We have presented a reconfigurable receiver model that changes its performance and power consumption according to the channel conditions. The transceiver model proposed is based on Figure of Merits of measured circuits reported in the literature. The receiver performance modes are chosen basing on a link quality estimation that provide a good approximation of the real SINR. We showed that considerable power can be saved in the case of good channel conditions. The models proposed can easily be implemented in a wireless network simulator in order to validate the value of a reconfigurable architecture according protocol models and real-world deployment scenarios.

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