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Trends and Challenges in CMOS Design for Emerging 60 GHz WPAN Applications

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1. Introduction

The extensive growth of wireless communications industry is creating a big market opportunity. Wireless operators are currently searching for new solutions which would be implemented into the existing wireless communication networks to provide the broader bandwidth, the better quality and new value-added services. In the last decade, most commercial efforts were focused on the 1-10 GHz spectrum for voice and data applications for mobile phones and portable computers (Niknejad & Hashemi, 2008). Nowadays, the interest is growing in applications that use high rate wireless communications. Multi-gigabit-per-second communication requires a very large bandwidth. The Ultra-Wide Band (UWB) technology was basically used for this issue. However, this technology has some shortcomings including problems with interference and a limited data rate. Furthermore, the 3-5 GHz spectrum is relatively crowded with many interferers appearing in the WiFi bands (Niknejad & Hashemi, 2008).

The use of millimeter wave frequency band is considered the most promising technology for broadband wireless. In 2001, the Federal Communications Commission (FCC) released a set of rules governing the use of spectrum between 57 and 66 GHz (Baldwin, 2007). Hence, a large bandwidth coupled with high allowable transmit power equals high possible data rates. Traditionally the implementation of 60 GHz radio technology required expensive technologies based on III-V compound semiconductors such as InP and GaAs (Smulders et al., 2007). The rapid progress of CMOS technology has enabled its application in millimeter wave applications. Currently, the transistors became small enough, consequently fast enough. As a result, the CMOS technology has become one of the most attractive choices in implementing 60 GHz radio due to its low cost and high level of integration (Doan et al., 2005). Despite the advantages of CMOS technology, the design of 60 GHz CMOS transceiver exhibits several challenges and difficulties that the designers must overcome.

This chapter aims to explore the potential of the 60 GHz band in the use for emergent generation multi-gigabit wireless applications. The chapter presents a quick overview of the state-of-the-art of 60 GHz radio technology and its potentials to provide for high data rate and short range wireless communications. The chapter is organized as follows. Section 2 presents an overview about 60 GHz band. The advantages are presented to highlight the performance characteristics of this band. The opportunities of the physical layer of the IEEE

802.15.3c standard for emerging WPAN applications are discussed in section 3. The tremendous opportunities available with CMOS technology in the design of 60 GHz radio is discussed in section 4. Section 5 shows an example of 60 GHz radio system link. Some challenges and trade-offs on the design issues of circuits and systems for 60 GHz band are reported in section 6. Finally, section 7 presents the conclusion and some perspectives on future directions.

2. Overview of the 60 GHz band characteristics

The quest for higher data rates and the spectrum scarcity makes designers of wireless communication systems explore higher frequency bands, such as the millimeter wave frequency band (30-300 GHz).

In 1995, the FCC has decided to open the largest contiguous bandwidth in history, 59-64 GHz for non-government unlicensed wireless communications (Van Tuy, 1996). Subsequently, this bandwidth was extended to 7 GHz, in United States in 2001, providing 5 GHz of overlap with unlicensed spectrum in Japan (59-66 GHz) and other geographical regions over the world. Table 1 shows the allocation of the international unlicensed spectrum around 60 GHz. This available spectrum can enable a huge channel bandwidth (2500 MHz) compared to other wireless communication standards.

Based on Shannon's theorem (Shannon, 1948), the maximum possible data rate of a communication channel is given by:

$$C = BW \log_2 \left(1 + \frac{S}{N} \right) \quad (1)$$

where C is the channel capacity, BW is the bandwidth of the channel, S is the total received power over the bandwidth, and N is the total noise power over the bandwidth.

The maximum possible data rate, known as channel capacity, increases with increasing channel bandwidth. Consequently, the 60 GHz band can be considered an attractive solution for high data rate wireless communications.

Region	Low frequency (GHz)	High frequency (GHz)	Bandwidth (GHz)
USA	57 GHz	64 GHz	7
Canada	57 GHz	64 GHz	7
Europe	57 GHz	66 GHz	9
Korea	57 GHz	64 GHz	7
Japan	59 GHz	66 GHz	7
Australia	59.4 GHz	62.5 GHz	3,1

Table 1. The allocation of the international unlicensed spectrum around 60 GHz in various region over the world

However, the 60 GHz spectrum is characterized by high levels of atmospheric radiofrequency (RF) energy absorption. Figure 1 shows the variation of oxygen attenuation versus frequency (FCC, 1997).

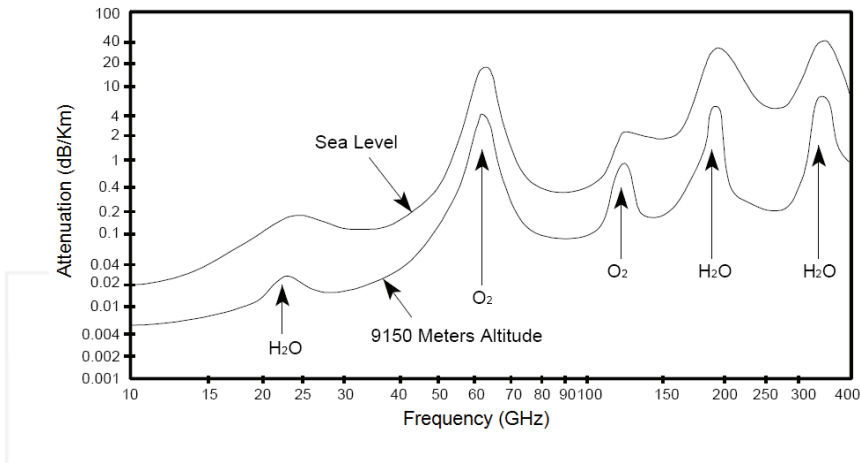


Fig. 1. The oxygen attenuation versus frequency (FCC, 1997)

The oxygen absorption has its maximum (10–15 dB/km) in the 60 GHz band. This makes the transmitted energy quickly absorbed by oxygen molecules in the atmosphere over long distances (Daniels & Heath, 2007). So that signals cannot travel far beyond their intended recipient. While this limits distances that they can cover, it also offers interference and security advantages which can make the 60 GHz band becomes an attractive alternative for high security, short-range and high-speed wireless communications (Guo et al., 2007).

In this context, the Ultra-Wide Band (UWB) technology has a long been used for short range and high data rate applications. However, this technology suffers from the immunity to interference (Guo et al., 2007). In the millimeter wave band, the oxygen absorption enables the benefit of reduced co-channel interference. Therefore, the transmitted signal from one 60 GHz transmitter is rapidly reduced in a manner that will not interfere with other links operating in the same geographic vicinity (Smulders et al., 2007). This enables dense wireless communication due to shorter frequency reuse distance.

Besides oxygen absorption, they have other parameters that degrade the performance of a 60 GHz transmission link which due to:

- Losses due to transmission channel
- Attenuation by rain
- Refraction
- Depolarization of signal

According to the Friis transmission equation (Friis, 1944), the free-space path loss (FSPL) formula is given by the following equation:

$$FSPL = \left(\frac{4\pi R}{\lambda} \right)^2 \quad (2)$$

where λ is the wavelength, and R is the distance between terminals.

Figure 2 shows the variation of FSPL versus distance with and without oxygen absorption at 60 GHz frequency. The FSPL is proportional to the square of the distance between the transmitter and receiver, as a result, the increase of this distance raises the FSPL.

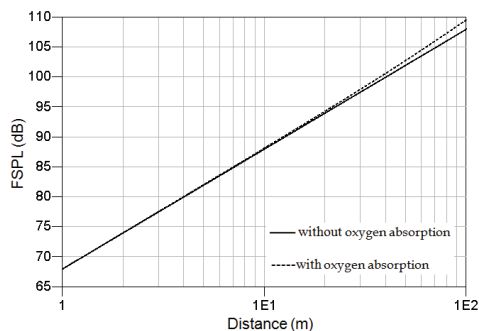


Fig. 2. The FSPL versus distance at 60 GHz

The FCC and various regulators over the world have allowed the limits on transmit power and the Equivalent Isotropic Radiated Power (EIRP) to ensure the wireless transmission in the 60 GHz band. Thus, the large unlicensed bandwidth associated with a high allowable transmit power can enable multi-gigabit wireless communications (Yong & Chong, 2007).

Actually, the millimeter wave band has several other advantages. In addition to the large spectral capacity, it can offer small antennas, and compact and light equipment (Daniels & Heath, 2007). Moreover, at 60 GHz operating frequency, the beamwidth is only equal to a few degrees and for WPAN applications an omnidirectional antenna pattern is usually desired (Lee et al., 2010).

A whole range of new applications in the area of consumer electronics devices can exploit this band for high data rate wireless applications. From uncompressed video distribution in the home, fast downloads of Gbytes of data at video kiosks, to Gbit/s wireless connections between laptops and printers (Fig. 3).



Fig. 3. Short range and high data rate millimeter wave communications with several devices

However, the design of 60 GHz wireless systems is not straightforward, and it exhibits several challenges. Indeed, the imperfections related to the blocks of a 60 GHz radio system (imperfect components, phase noise, non-linearity, etc...) can cause degradation in the overall-performance. The interior of buildings is also a multipath channel. Many obstacles (walls, partitions, ceilings, furnishings) are reflective surfaces for the waves. The existence of multiple paths is the cause of channel fading which requires a high-performance signal processing in reception (synchronization, equalization, correction of errors) especially when the data rate is significant (Daniels & Heath, 2007).

3. IEEE 802.15.3c standard for emerging WPAN applications

The IEEE 802.15.3 Task Group 3c (TG3c) was formed in March 2005. The TG3c developed a millimeter wave based alternative physical layer (PHY) for the existing 802.15.3 Wireless Personal Area Network (WPAN) Standard 802.15.3-2003. The 802.15.3c-2009 was published on September 11, 2009. This is the first standard that addresses multi-gigabit short-range wireless systems. It is aimed to support a minimum data rate of 2 Gbps over a few meters with optional data rates in excess of 3 Gbps. The 802.15.3c-2009 employs a channel plan that divides the 60 GHz spectrum into channels of approximately 2.16 GHz each. Such wide channels make it easy to achieve gigabit data rate even with relatively simple modulation and coding schemes (Yang, 2008). Three PHY modes are specified in the standard: single carrier (SC) PHY, high speed interface (HSI) orthogonal frequency division multiplexing (OFDM) PHY and audio video (AV) OFDM PHY. Table 2 shows some characteristics of these PHY modes. The existence of three PHY modes, with different characteristics, is due mainly to the possibility for supporting various applications.

	SC	HSI OFDM	AV OFDM
Modulation	BPSK, (G)MSK, QPSK, 8PSK, 16QAM	QPSK, 16QAM, 64QAM	QPSK, 16QAM
Data rate	25.3Mbps-5.1 Gbps	31.5Mbps-5.67Gbps	0.95-3.8 Gbps

Table 2. Some characteristics of the PHY modes

Actually, the SC PHY mode provides three classes of modulation and coding schemes targeting different wireless connectivity applications. Class 1 is specified to address the low-power low-cost mobile market while maintaining a relatively high data rate of up to 1.5 Gbps. Class 2 is specified to achieve data rates up to 3 Gbps. Class 3 is specified to support high performance applications with data rates in excess of 5 Gbps. However, the HSI PHY mode is designed for devices with low-latency, bidirectional high-speed data and uses OFDM. HSI PHY supports a variety of modulation and coding schemes using different frequency-domain spreading factors, modulations, and LDPC block codes. Finally, the AV PHY is implemented with two PHY modes, the high-rate PHY (HRP) and low-rate PHY (LRP), both of which use OFDM. A Common mode signaling is defined which is an SC-based $\pi/2$ binary phase shift key (BPSK) with low data rate (25 Mbps) in order to promote coexistence among these PHY modes.

4. CMOS technology for 60 GHz radio design

It is commonly believed that the promising 60 GHz radio technology has introduced new opportunities and perspectives for several wireless applications. Thus, the design of millimeter wave circuits is achieving growing interest in modem communication systems (Winkler et al., 2004). Traditionally, technologies based on III-V compound semiconductor, which achieve frequency transitions of several tens of gigahertz, were exclusively used for the implementation of millimeter wave circuits due to their superior noise characteristics and power handling at higher frequencies (Reynolds, 2004). Such technologies were mainly intended for military applications for which the cost is not very relevant (Floyd et al., 2005). Moreover, these technologies show low power efficiency and limited the digital integration.

The intensive investigations in the design of millimeter wave circuits and systems are characterized by a deep research of maximum performances with minimum costs following the targeted wireless communication standards (Hajimiri, 2007). Reducing costs come through high level integration of a maximum functions within the radio communication system. In this context, the complementary metal-oxide semiconductor (CMOS) technology based on silicon is generally the most suitable for implementing on-chip radios since the silicon remains incomparable both in terms of digital integration, production capacity and overall reliability of design and performance.

Nowadays, thanks to the large progress of lithography, CMOS processes below 130 nm, led to maximum frequency of operation (f_{\max}) comparable to those of the best processes in bipolar silicon and AsGa. Actually, the continuous progress of silicon CMOS technology has enabled its application in millimeter wave applications. The scaling of the dimensions of transistors, following the Moore's law (Moore, 1965), has the peculiar property of improving cost, performance, and power consumption. Currently, the transistors became small enough, consequently fast enough and show a very high transition frequency (more than 400 GHz) (Fig. 4). Therefore, the CMOS technology is becoming the future technology of choice in implementing millimeter wave integrated circuits due to low cost manufacturing and feasibility of the integration with digital circuits (Doan et al., 2004).

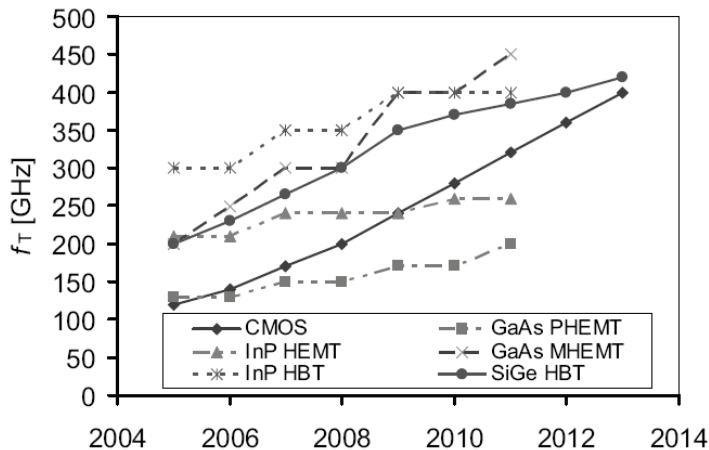


Fig. 4. The evolution of f_T by year of production comparing silicon and III-V compound semiconductor devices (Niknejad et al., 2008)

5. 60 GHz radio system link

The aim of this section is to test the performance of a 60 GHz link for WPAN applications. In order to do that, a case study of a transceiver is implemented based on performances, at 60 GHz, of its building blocks in the literature (Barakat, 2008).

Fig. 5 shows the transceiver setup with characteristics of different building blocks at 60 GHz. The used filters are ideal filters with quality factors depend on the specified frequency. This simulation schematic allows to study the link budget by given the power at each point of a link. The received power after demodulation is considered in this simulation.

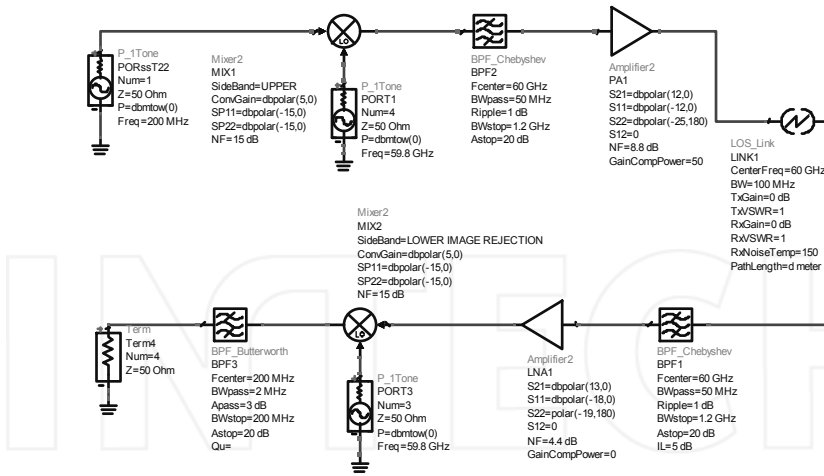


Fig. 5. The simulation setup with the characteristics of different building blocks

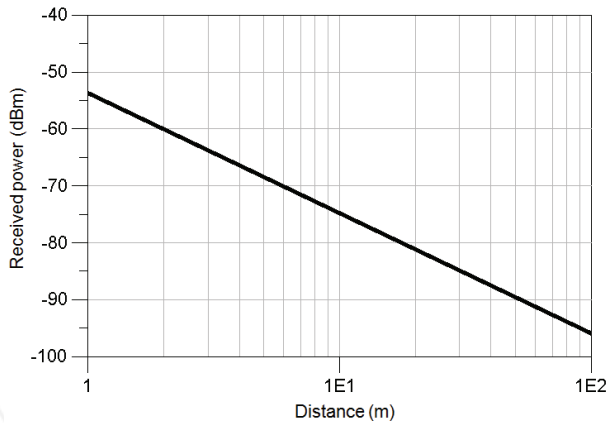


Fig. 6. The received power after demodulation at 60 GHz for a transmit power of 0 dBm vs. distance

Fig. 6 shows the variation of the received power, after demodulation at 60 GHz, in function of distance when the transmit power is equal to 0 dBm. Since, the WAPN applications in the 60 GHz band require short-range distance (10 to 100 meters); it is possible to ensure 60 GHz multi-gigabit wireless communications (Yong & Chong, 2007).

The design of 60 GHz wireless system is not straightforward and exhibits several challenges (Emami et al., 2007). In the literature, several transceiver architectures have been proposed for millimeter frequency band. Actually, the Low IF architecture requires stringent image rejection, as an adjacent channel becomes its image (Razavi, 2006). The Zero IF is referred to as “no image” but it is susceptible to flicker noise, DC offset and also suffers from

impairments of even order distortion, LO pulling and LO leakage (Reynolds et al., 2006). Therefore heterodyne structure with two down-conversion steps can be considered as interesting solution of implementing 60 GHz radio transceivers for WPAN applications (Parsa & Razavi, 2009).

6. Trends and challenges in designing 60 GHz building blocks in CMOS

The design and modeling of 60 GHz building blocks of a transceiver requires several challenges and trends. Actually, the CMOS design at millimeter wave can be characterized by two different approaches which depend on the simulation environments and the related techniques. As an example, analog RF designers prefer to use inductors rather than transmission lines which are used by microwave designers (Leenaerts et al., 2001). Indeed, these choices can have an impact on the layout since transmission lines consume a large area while spiral inductors generally occupy a smaller area (Scheir et al., 2007).

Furthermore, at millimeter wave frequencies, the design of active and passive devices and interconnects becomes more complicated, since the effects of layout parasitic elements cannot be neglected, otherwise a strong frequency down-shift will occur between simulation and measurement results (Majek et al., 2009). Consequently, the accurate modeling of active and passive devices is normally considered as the premise of the design success in millimeter wave circuits (Liang et al., 2009).

This section outlines the various design trade-offs of millimeter wave CMOS integrated circuits based on the review of the state-of-the-art. The study will focus in three of the most critical building blocks in the radio front-end: LNA (Low-Noise Amplifier), Mixer and VCO (Voltage-Controlled-Oscillator) used as a LO (Local Oscillator).

6.1 Low-Noise Amplifiers

The Low Noise Amplifier (LNA) is the most critical building blocks in transceiver since it bears the receiver noise performance according to Friis formula (Friis, 1944):

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_N - 1}{G_1 G_2 \dots G_{N-1}} \quad (3)$$

where F is the noise figure of the receiver, F_i is the noise figure of the stage number i and the G_i is the gain of the stage number i .

Indeed, the first stage of the LNA supports the noise figure of the receiver. Besides the low noise figure, high gain, good isolation, large bandwidth and low power consumption are the main parameters of a high performance LNA.

The common gate and common source topologies have a long been employed in the design of LNAs for RF, microwave and millimeter wave applications. While these simple architectures can exhibit a low noise figure, they cannot achieve the good isolation and high gain compared to a classical cascade topology (Maruhashi et al. 2008).

In the literature, several references have been reported the design of CMOS LNA in the 60 GHz band. The design reported in (Doan et al., 2005) is the first tentative 60 GHz amplifier on CMOS; this design is more a general purpose amplifier than a LNA.

A three-stage common source LNA is reported in (Kai Kang al., 2010). Fig. 7 shows the schematic of this LNA. The size of the MOSFETs is $32 \times 1 \mu\text{m} \times 90 \text{nm}$. The width of the microstrip lines is either $5 \mu\text{m}$ or $9 \mu\text{m}$ and $V_D = 1.2 \text{V}$ (Kai Kang al., 2010).

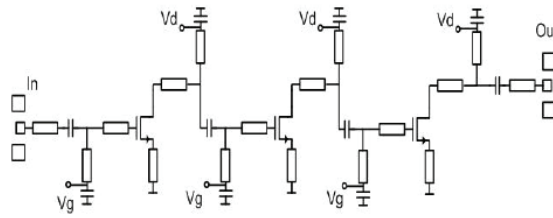


Fig. 7. The three-stage common source LNA (Kai Kang al., 2010)

This design is implemented in 90 nm CMOS process and it achieves a gain of 18.6 dB and a noise figure of 5.7 at 57 GHz. However, it consumes 24 mA from a 1.2 V supply voltage (Kai Kang al., 2010).

The cascode topology represents the most widespread circuit solution for realizing high-gain and stable low-noise amplifiers (Razavi, 2005). However, the cascode LNA needs new circuit technique to achieve good performances. One solution is the interstage matching topology. A serie inductor inserted between the common gate and the common source stages as proposed in (Tao et al., 2009). Fig. 8 shows this single-stage cascode low noise amplifier operating in the range of 57 to 64 GHz. The co-simulation performances of the LNA at 60 GHz are reported in (Tao et al., 2009). The voltage gain and noise figure are equal to 18.7 dB and 4.2 dB respectively while the DC power is equal to 4.9 mW.

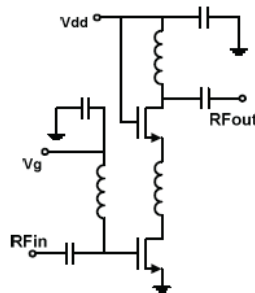


Fig. 8. The single-stage cascode LNA (Tao et al., 2009)

6.2 Mixers

The mixer is an essential component in wireless transceivers for frequency translation, which requires high conversion gain, low noise figure, and high linearity. In the literature several mixer architectures, which are suitable for operating in the millimeter wave frequencies, has been studied for WPAN Applications.

The resistive mixers show a high linearity, superior intermodulation properties and virtually zero dc power consumption. Indeed, the performance of the resistive mixers remains unaffected by the low supply voltage allowed in the deep submicron CMOS-technologies (Motlagh et al., 2006). However, these resistive mixers have a conversion loss instead of gain (Motlagh et al., 2006). The bulk-driven architecture that uses the transistor as a four terminal device can provide low voltage and low power operation for mixer design (Wang & Tsai, 2009). A bulk-driven mixer has been designed using 130 nm CMOS

technology (Wang & Tsai, 2009). In spite of having a high noise figure which is equal to 23 dB, this bulk-driven mixer exhibits a conversion gain of 1 dB and a power consumption of 3 mW at 60 GHz. The millimeter wave passive mixer followed by an IF amplifier can reach roughly the same noise figure and conversion gain as an active topology does (Razavi, 2009). However, the passive mixer suffers from a lower input impedance than does the active mixer, heavily loading the LNA (Razavi, 2008). The Gilbert-cell down-conversion mixer operating at 60 GHz has been reported in (Tsai et al. 2007). These mixers showed good isolation between RF and LO ports associated with high power consumption which make these Gilbert-cell mixers not suitable for low power and low-voltage applications (Wang & Tsai, 2009). In contrast, the double-balanced gate mixers exhibit low supply voltage and low dc consumption (Lien et al., 2010). Compared to other double-balanced mixers, these mixers show low LO power, low noise figure and high conversion gain, and they have better isolations than the single-balanced gate mixers (Lien et al., 2010). The design in (Emami et al., 2005) shows a 60-GHz quadrature balanced single-gate mixer implemented in 130 nm CMOS technology. This design can be considered as the first mixer realization in the 60 GHz range. This mixer shows a conversion loss less than 2 dB and the return loss at the RF and LO ports higher than 15 dB while consuming 2.4 mW. The input-referred 1-dB compression point is -3.5 dBm.

The dual-gate MOSFET mixer can be considered as alternative choice compared to the previous topologies (El Oualkadi et al., 2009). Fig. 9 shows the architecture of this mixer. The RF signal is applied to the gate of the transistor M_RF and the LO signal is applied to the gate of the second transistor M_LO.

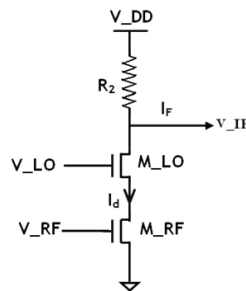


Fig. 9. The architecture of the dual-gate MOSFET mixer

The mixer architecture is composed by two transistors in cascade. The advantage of using a cascode topology is that it allows the RF input and the LO signal to be fed into two different MOSFET gates, avoiding the need for area-consuming power combiners. Since the RF and LO rejections at the IF output are not so critical due to the large spectral differences, this topology can be employed instead of Gilbert mixers and thus avoiding the use of lossy baluns (Maas, 1986). The M_RF transistor operates in the saturation region and provides a transconductance g_m , which is a function of the drain voltage of M_RF transistor controlled by the LO signal. However, the M_LO transistor operates in the linear region and used for commutation as a switch according to the LO signal.

The 60 GHz dual-gate MOSFET mixer was designed and optimized in CMOS 65 nm technology (El Oualkadi et al., 2009). The mixer shows a suitable conversion gain when considering that the supply voltage does not exceed 1.2 V with a power consumption of 8.5

mW. Table 3 shows the performance of this mixer compared to the previous published 60 GHz mixers. This dual-gate mixer shows a good compromise between simplicity and good performances.

	(Emami et al., 2005)	(Lai et al., 2006)	(Wang & Tsai, 2009)	(El Oualkadi et al, 2009)	(Lien et al., 2010)
Approach	Single-gate	Cascode	Bulk-driven	Dual-gate	Double-balanced
Process	130nm CMOS	90nm CMOS	130nm CMOS	65nm CMOS	130nm CMOS
Freq (GHz)	54-61	60	51-61	60	
Conversion Gain (dB)	-1 @ 60 GHz	-1.2	1 @ 60 GHz	0.4	-3~0
Input P_{1dB} (dBm)	-3.5	0.2	-19	1.264	-8
Supply Voltage (V)	1.2	-	1	1.2	-
Power consumption (mW)	2.4	29.4	3	8.5	14

Table 3. Performance comparisons of some millimeter wave mixers reported in the state-of-the-art

6.3 Oscillators

A key building block in radio transceiver is the VCO which is employed as a LO for assuring the modulation/demodulation. The implementation of VCOs in CMOS technology is justly felt as one of the major challenges that must be overcome in the design of integrated 60 GHz WPAN transceivers (Regimbal et al., 2009). Indeed, the limited transistor speeds and long interconnects causes some critical issues related to the generation of I and Q phases of the LO at 60 GHz. The quadrature operation typically degrades the phase noise considerably (Razavi, 2005). While, the division of LO frequency poses a problem, since; the design of high-speed dividers requires many challenges at 60 GHz (Razavi, 2009). Besides these challenges, a number of performance requirements have to be met to make a VCO suitable for 60 GHz WPAN applications. Most importantly, low phase noise is required to avoid corrupting the mixer-converted signal by close interfering tones. Low power consumption and tenability are also two important aspects that define the performance of a VCO (Razavi, 2000).

The ring oscillators and passive RC-CR networks are two of the most commonly used solutions for quadrature generation. While ring oscillators are widely used for digital-based applications, passive networks suffer from high loss and inaccuracy. The LC cross-coupled oscillators and Colpitts oscillators are the most suitable for RF and millimeter applications due to their excellent phase noise performance (Kim et al., 2008). However, the use of several inductors in the LC VCOs leads to difficulties in the layout. Indeed, the substrate loss affects directly the quality factors of inductors and varactors in the millimeter wave range (Liang et al., 2009). Therefore, the trade-offs between the phase noise, the tuning range, and the power dissipation become much more severe (Razavi, 2009).

The millimeter wave CMOS oscillators proposed in the literature commonly used a cross coupled transistor pair with different resonator structures (Farahabadi et al., 2009).

An example of a LC VCO based on cross coupled topology is proposed in (Borremans et al., 2008). This design implemented in 130 nm CMOS shows interesting performances at 60 GHz. The measured phase noise is below -90 dBc/Hz at 1 MHz offset with a power consumption of 3.9 mW at 1 V. The tuning range exceeds 10 %, for a tuning voltage restricted from ground to the supply (Borremans et al., 2008). Such performances can allow this VCO to be an interesting solution for WPAN applications.

To realize the direct downconversion operation, a 60 GHz receiver requires a VCO with quadrature phase generation. A VCO using an injection-coupled topology is used in (Sakian et al. 2009) to generate quadrature 60 GHz outputs. Fig. 10 shows the schematic of this VCO.

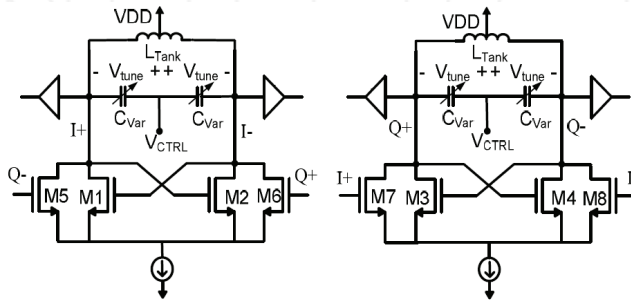


Fig. 10. The two LC-VCOs coupled in anti-phase to provide I-Q outputs (Sakian et al. 2009)

The required negative conductance is generated by the cross-coupled pairs M1-M2 and M3-M4. The coupling transistors M5-M8 inject the output signals of one cross-coupled pair to the input of the other to produce anti-phase coupling required for quadrature generation (Sakian et al. 2009).

The measurements show a tuning range of 5.6 GHz (57.5 to 63.1 GHz), a phase noise of -95.3 dBc/Hz at 1 MHz offset and a power consumption of 36 mW. Despite the additional challenges and limitations imposed by the quadrature topology, the obtained performances are comparable to state of the art single-phase VCOs, (Sakian et al. 2009).

7. Conclusion

During the recent years, the 60 GHz band has gained increased academic and commercial interest mainly due to the availability of a large unlicensed spectrum in the vicinity of 60 GHz. Nowadays, thanks to the development of the IEEE 802.15.3c standard for WPAN, various commercial applications have been emerged. Thus, the 60 GHz band is considered as an attracting solution for broadband wireless in particularly for short range and high data rate applications.

The implementation of new 60 GHz wireless applications is strictly related to the development of high performance 60 GHz radio transceivers. This implies that the designers of circuits and systems must overcome several challenges and trade-offs which occurring when working in the millimeter wave spectrum (Hajimiri, 2007).

The CMOS technology which is the dominating technology for most wireless products below 10 GHz, is characterized by reliability, maturity, low manufacturing cost and low

power consumption compared to traditional semiconductor technologies based on III-V compound materials such as SiGe and GaAs. In addition, CMOS is the most suitable technology for designing system-on-chip, since it enables integration of the analog RF circuits with the digital signal processing and baseband circuits in the lowest possible chip area, which leads to a lower cost and more compact solution. With the enormous worldwide effort to scale to lower gate-lengths, CMOS technology is pushing further into the millimeter wave region with maximum frequency of oscillation exceeding 300 GHz promising increasing performance in the future (Niknejad, 2008).

Today, the interest on designing millimeter wave CMOS circuits and systems is growing rapidly offering a fertile ground for innovation. CMOS technology is becoming the strong candidate for implementing low cost and less power consuming 60 GHz WPAN transceivers which are expected to boost wireless communication data rates to the order of multi-gigabit-per-second.

Actually, if several efforts have been done that ameliorate the challenges in millimeter wave design many questions still remain (Razavi, 2009). Therefore, various areas of investigation will certainly be the subject of deep research in the next coming years. For example:

- At the device level, several efforts should be done in the accurately modeling of both active and passive devices in the millimeter wave band. The objective is to have scalable models which would allow an efficient design of the building blocks.
- At the circuit level, some building blocks require new design techniques in order to improve the targeted performance at 60 GHz, like power amplifiers and switches. The integration of antennas still remains as a big challenge to promote the single on-chip transceivers.
- At the system level, new methodologies for simulation of large transceivers and their layouts should be developed. Issues related to packaging must be solved to facilitate coupling among various building blocks through the power lines and the substrate.

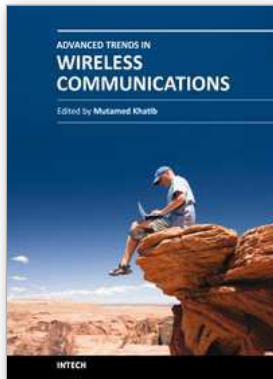
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Physical limitations on wireless communication channels impose huge challenges to reliable communication. Bandwidth limitations, propagation loss, noise and interference make the wireless channel a narrow pipe that does not readily accommodate rapid flow of data. Thus, researches aim to design systems that are suitable to operate in such channels, in order to have high performance quality of service. Also, the mobility of the communication systems requires further investigations to reduce the complexity and the power consumption of the receiver. This book aims to provide highlights of the current research in the field of wireless communications. The subjects discussed are very valuable to communication researchers rather than researchers in the wireless related areas. The book chapters cover a wide range of wireless communication topics.

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