CMOS RF down-conversion mixer design for low-power wireless communications

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Abstract

This paper aims to study the design of a low-power single-balanced mixer for down-conversion in wireless RF receivers. The proposed circuit is designed to work at a radiofrequency of 1.9 GHz using CMOS 0.18 µm technology. The obtained results show a conversion gain equal to 7 dB and low power consumption of 3.86 mW at 1.8 V supply voltage. The single side band noise figure performance was founded to be 8 dB. These results show a good potential of this CMOS mixer and justify its use for low-power wireless communications.

Keywords: Analog design, RF mixer, conversion gain, wireless communications, CMOS technology.

1. Introduction

The rapid evolution of wireless communication requires increasingly higher performance which raises the complexity of systems used for these applications. This requires the development of new communication systems that will have to meet very strict criteria imposed by this mutation. However, this trend is characterized by a strong demand for new solutions fully integrated with low-cost and low power consumption. Traditionally, wireless systems are built with different technologies, GaAs and SiGe for the radiofrequency part (RF) and CMOS for the baseband part (BB) as shown in Figure 1. The SiGe or GaAs technologies are used for their relatively high transition frequencies and low noise level. However, their manufacturing costs are high. Further more, they are incompatible with the digital building blocks [1].

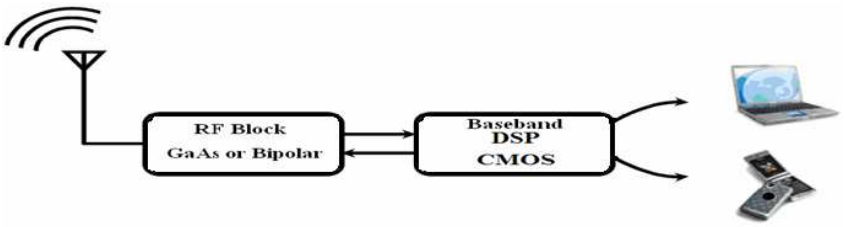

Figure 1 : Bidirectionnel communication system

On the other hand, the use of CMOS technology, to achieve high integration level, has significant advantages for the design of RF integrated circuits. Indeed, in recent years the huge efforts, provided by the microelectronics industry to reduce the size of transistors allow the integration of RF building blocks in CMOS technology. This integration is intended to reduce the cost, the size and the power consumption while increasing the functionality of the system; furthermore, it allows the full integration of both the analog and the digital building blocks on a single chip. Indeed, both the full integration and the low-voltage design,

particularly in high-frequency applications, require the research and the use of architectures able to pursue the current development of wireless communications systems.

The mixer is an important building block in each communication system whose impact is critical on the performance of other blocks. Indeed, to retrieve the desired signal, it is necessary to perform a frequency conversion by a mixer which allows a time multiplication of two signals, the first one (called RF signal) comes from the receiver antenna after has been filtered and amplified, and the other signal (called LO signal) comes for a local oscillator (Figure 2), the result is a transposition of a high or a low intermediate frequency (IF) with a minimum of a magnitude loss and a minimal noise figure. However, in fact, this conversion process causes a series of difficulties which affect the overall performances of the mixer (gain, noise, linearity, isolation, consumption and cost).

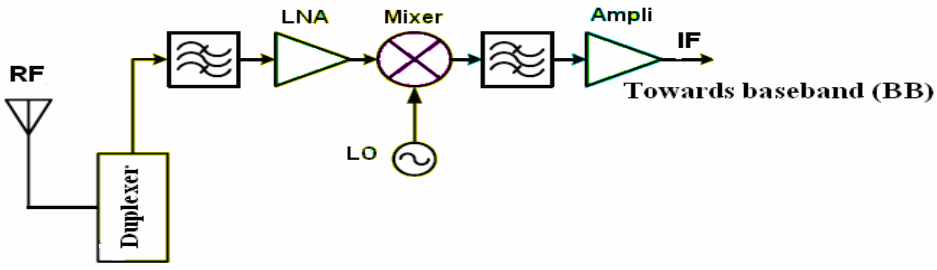

Figure 2 : RF receiver building blocks

This paper aims to study the design of an integrated single-balanced mixer in CMOS 0.18 µm for low-power down-conversion in RF reception. The main goal is to optimize the performance of the mixer in order to make it useful for applications in wireless communications around an RF frequency equal to 1.9 GHz. To do this, we began our study by searching both the optimal design values of the mixer components in CMOS 0.18 µm and the correct bias circuit in order to improve its performance in terms of the conversion gain, the 1-dB compression point and the 3rd order interception point.

2. Architecture of the proposed mixer

A mixer is an ideal analog multiplier with three ports. Although the multiplication is a simple mathematical operation, it is difficult (if not impossible) to achieve in an ideal manner [2], since in practice the mixing operation is performed using non-linear components. Also, as shown in figure 2, the mixer is located between a low-noise amplifier (LNA) that receives the RF signal and a channel filter that ensures the signal reception in the desired baseband. Therefore, the choice of CMOS technology in this design is required to ensure both a good gain of the whole system and an excellent matching between the input and output of the mixer circuit.

Figure 3 shows the architecture of the proposed mixer which is a single balanced mixer (SBM). In this design, the RF and LO frequencies are fixed at 1.9 GHz and at 1.8 GHz which offers an intermediate frequency of 100 MHz. This IF value can meet the requirements of current communication wireless standards which typically operate around the 1 GHz frequency (such as GSM, IS695, PDC) [3] [4] [5].

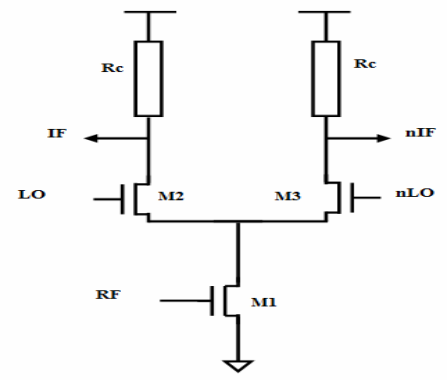

Figure 3 : Architecture of a single balanced mixer

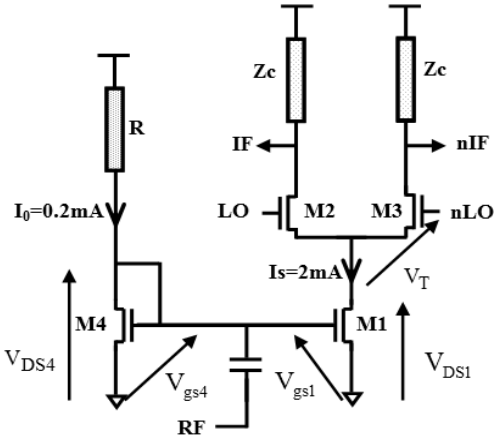

Figure 4 : Biased circuit of the proposed mixer

Moreover, an intermediate frequency of 100 MHz is also very sufficient for cancelling both interferences and problems of image frequency rejection [6], [7].

3. Mixer circuit design

3.1. Bias circuit of the mixer

Figure 4 shows the biased circuit of the proposed mixer; this circuit can set the static operating point keeping the current mirror transistors M_1 and M_4 in the saturation mode. We started by looking for the optimal values of W and L, respectively, the width and length of the NMOS transistors used. Then we run simulations while setting the current I_0 to 0.2 mA with a ratio of 10 between the two NMOS M_1 and M_4 to recopy the current I_S (0.2 × 10 = 2 mA) by tuning the value of the resistor R while keeping the voltage V_{DD} = 1.8 V.

The relation between I_0 ,$V_{GS}(M_4)$ and V_{DD} is given by :

$$I_0 = \frac{V_{DD} - V_{GS4}}{R} \quad (1)$$

At this stage, the effect of channel modulation may arise. Indeed, as shown in figures 5a and 5b, for variations in the length L there is an inverse relationship between the current I_{DS} and V_{DS} in accordance with the following :

$$I_{DS} = \mu_n C_{ox} \frac{W}{2.L}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \quad (2)$$

where C_{ox} is the surface capacity of the grid-channel MOS transistor, V_T is the threshold voltage and μ_n is the mobility of carriers.

To solve this issue, the lengths of the M_1 and M_4 MOS transistors have been increased.

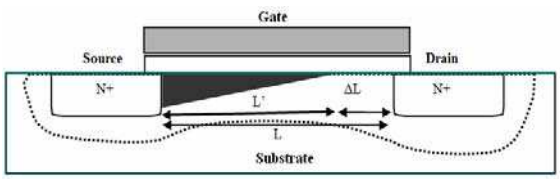

Figure 5.a : MOS transistor

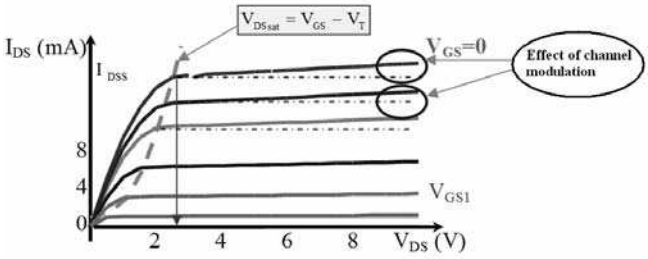

Figure 5.b : Effect of channel modulation

The saturation condition of transistor M_1 is defined by

$$V_{DSM1} > (V_{GSM1}-V_T) \quad (3)$$

and as

$$V_{DCM2} = V_{GSM2} + V_{DSM1}. \quad (4)$$

Or $V_{DCRF} = V_{DSM1}$ so $V_{DSM1} > (V_{DCRF} - V_T)$, by replacing (4) in the last inequality, the saturation condition in common mode of LO signal LO becomes

$$V_{DCRF} - V_T + V_{GSM2} < V_{DCM2} \quad (5)$$

3.2. Conversion Gain of the mixer

The proposed architecture is a single balanced architecture with the two transistors of the differential pair in switching mode; therefore the current output is controlled by the state of the signal generated by the local oscillator which is given by :

$$I_{out} = I_S(t).sign[V_{LO}(t)], \quad (6)$$

then, we can obtain

$$I_{out}(t) = \left\{I_0 + g_{m\_rf} V_{RF}\cos(\omega_{RF}.t)\right\}\frac{4}{\pi}\left\{\cos(\omega_{OL}.t) - \frac{1}{3}\cos(3\omega_{OL}.t) + \frac{1}{5}\cos(5\omega_{OL}.t) + ...\right\}$$

$$= \left\{\frac{4I_0}{\pi}\cos(\omega_{OL}.t) + \frac{2}{\pi}g_{m\_rf}V_{RF}\left[\cos\left((\omega_{RF} - \omega_{OL}).t\right) - \cos\left((\omega_{RF} + \omega_{OL}).t\right)\right] + ...\right\}$$

since $V_{out}(t) = Z_c.I_{out}(t)$,

then, we can write

$$V_{out}(t) = \left\{\frac{4I_0}{\pi}Z_c.\cos(\omega_{OL}.t) + \frac{2}{\pi}Z_c.g_{m\_rf}V_{RF}\left[\cos\left((\omega_{RF} - \omega_{OL}).t\right) - \cos\left((\omega_{RF} + \omega_{OL}).t\right)\right] + ...\right\}$$

where the term $sign[V_{OL}(t)] = \frac{4}{\pi}\left\{\cos(\omega_{OL}.t) - \frac{1}{3}\cos(3\omega_{OL}.t) + \frac{1}{5}\cos(5\omega_{OL}.t)...\right\}$ is the Fourier transform of a square signal.

We have $I_s(t) = I_0 + g_{m\_rf}V_{RF}\cos(\omega_{RF}.t)$.

The conversion gain is given by $G_{conv} = \frac{\left|V_{out}(t)\right|_{à(\omega_{RF}-\omega_{OL})}}{\left|V_{RF}(t)\right|_{à(\omega_{RF})}} = \frac{2}{\pi}g_{m\_rf}Z_c$ (7)

In a first step, we started the theoretical calculations and simulations using a resistive load $R_c = Z_c$, thus:

$$G_{conv} = \frac{2}{\pi}g_{m\_rf}R_c \quad (8)$$

which yields a theoretical value of G_{conv} = 20.12 dB and simulated G_{conv} = 14.39 dB.

This difference between the two gains requires taking into account the resistance of the differential pair r_{DS} which is in parallel with R_c, the gain relationship becomes then:

$$G_{conv} = \frac{2}{\pi}g_m(R_c // r_{DS}) \quad (9)$$

and in this case we found :

Theoretical G_{conv} = 14.43 dB and simulated G_{conv} = 14.39 dB.

This simulation shows the importance of taking into account all the parameters that could affect the results.

Note that the differential output generates a signal containing two other frequencies:

$f_{RF} - f_{LO}$ et $f_{RF} + f_{LO}$ hence the need to use a capacitor C to filter the HF : $f_{RF} + f_{LO}$. The gain relationship becomes then:

$$G_{conv} = \frac{2}{\pi} g_m (R_c // r_{DS} // C) \quad (10)$$

this gives: theoretical G_{conv} = 7.2 dB and simulated G_{conv} = 7.4 dB.

Certainly adding this capacity decreases the performances of the mixer in terms of voltage gain, but it helps to have a good filtered output signal.

4. Performances of the mixer design

As mentioned above, the conversion gain depends mainly on the bias resistor Rc as shown in the following table:

Rc (Ω)	Conv Gain (dB)	NF (dB)
200	7	8
400	4	9
100	3	8

Table 1 : Variation of the conversion gain & the noise factor with R_c values

The conversion gain and the noise factor are optimal for a value of Rc = 200 Ω. This is found with the following sizes of NMOS used:

L = 0.18 µm: Gate length of all transistors.

W = 100 µm: Gate width of M_1, M_2, M_3 and W_4 = 80 µm Gate width of M_4.

A DC simulation, using the values mentioned above, can provide the power consumption of 3.86 mW (V_{DD} = 1.8 V and I_S = 2.145 mA).

- **Results of transient simulation:**

Figure 6 shows the IF output signal whose frequency is about 100 MHz, such an output signal is in fact the modulation of the carrier RF and the IF signal that can be obtained after a proper filtering of other frequency harmonics.

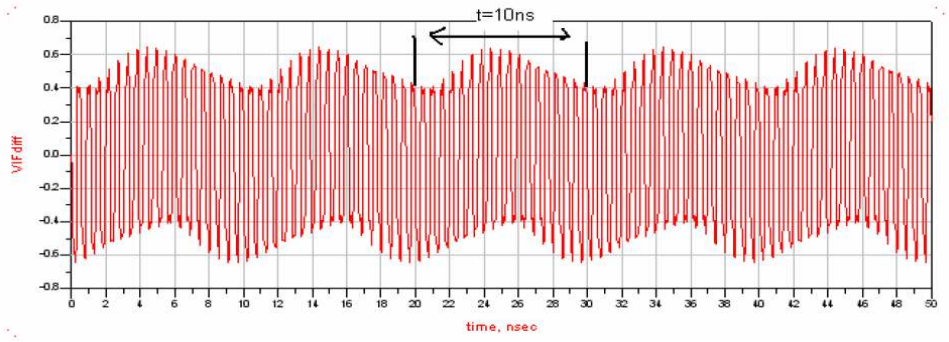

Figure 6 : IF output signal as a function of time.

- **Results in the frequency domain:**

Figure 7 shows a linear region where the output power is directly proportional to the input power and a decreasing region from -10 dBm resulted in the non-linearity of the mixer circuit. These results are obtained by tuning the input power from -50 dBm to 0 dBm.

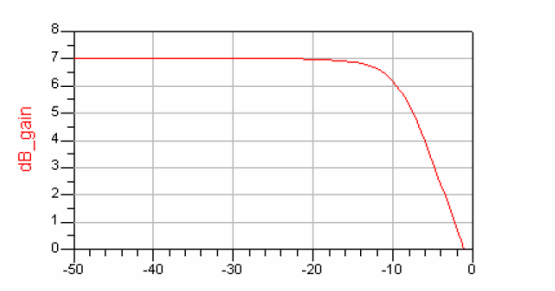

Figure 7 : Gain versus RF input power

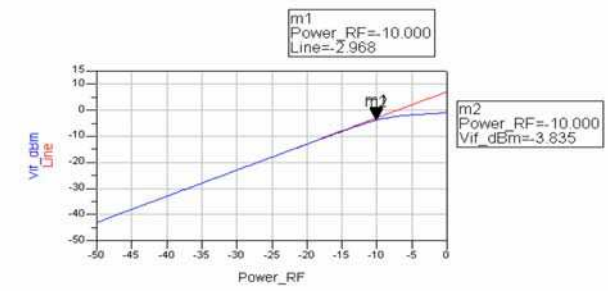

Figure 8 : 1-dB compression point

Figure 8 shows the simulation of 1-dB compression point which is equal to -10 dBm. To evaluate the distortion in the mixer circuit, the third input intercept point (IIP3) was simulated. From figure 9, the resulted IIP3 is roughly equal to -5 dBm, indeed by considering the input signals : f1 = 1.8 GHz and 2.f1 - f2 = 1.7 GHz, and an input power equal to -10 dBm, then :

$$IIP3 = \frac{IM3}{2} + Power\_RF \quad [8] \qquad IIP3 = \frac{10,7}{2} - 10 \approx -5\,dBm$$

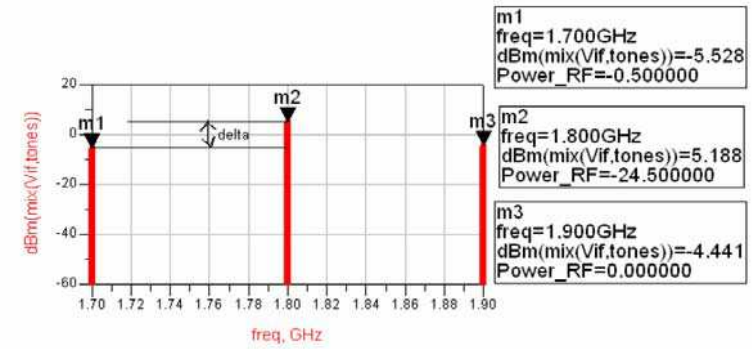

Figure 9 : Third order input intercept point (IIP3)

The performances of the proposed mixer are compared with the state-of-the-art (table 2). It seems that proposed design shows good performances in term of conversion gain and power consumption value, compared to other previously reported designs. However, the IIP3 and the 1-dB compression points are still at a reasonable level.

Ref	Supply Voltage (Volts)	Freq. RF (GHz)	CG [dB]	IIP_3 (dBm)	P-1dB (dBm)	Noise Figure (dB)	Tech. (µm)	Power Consum.(mW)
[9]	2	0.9	1.1	-3.3	-15.4	-	0.35	7.2
[10]	1.5	2.4	3.3	5.46	-8.98	14.87	0.18	5.6
[11]	1.8	2.44	-2.6	12.81	5.07	13.67	0.25	13.3
[12]	1.8	3.168-3.693	7.5-10.1	-	-	8.8-12.5		13.24
This work	1.8	1.9	7	-5	-10	8	0.18	3.8

Table 2: Performance Comparison of recent mixers

4. Conclusion:

The proposed study has demonstrated the design of a low power single balanced mixer in CMOS 0.18 µm technology. The designed mixer shows a suitable gain when considering that the supply voltage does not exceed 1.8 V with a very low power consumption of 3.8 mW, a noise figure of 8 dB, a 1-dB compression point of -10 dBm and an IIP 3 of -5 dBm. These performances allow both a low-size and a low-cost integration of the proposed mixer on a single chip which makes this design very suitable for low-power wireless communication applications in the band around a RF frequency of 1.9 GHz.

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