Design of a Modified Ultra-Wide Band Low-Noise Amplifier (UWB.LNA) Topology with Good Linearity in CMOS 65 nm Technology

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Abstract

The Low-Noise Amplifier (LNA) is the first and the important building block in a radiofrequency (RF) receiver since it must lead the signal from a receiving antenna at a level that can be properly addressed by the down-conversion architecture without adding noise.

This paper describes a modified LNA architecture for Ultra-Wide Band (UWB) applications using a cascade inductive source degeneration topology. The proposed architecture was designed using CMOS 65 nm technology to operate in a broad frequency band from 0.8 GHz to 2.4 GHz which includes a large number of standards and RF applications. The designed UWB LNA shows a 14.35 dB power gain with a noise figure of 1.4 dB for power consumption of 29 mW, a 1-dB compression point ranging from -5 to 3 dBm, a IP3 ranging from 5 to 14 dBm, and an input return loss below -10 dBm.

Keywords

S parameters, UWB LNA, inductive source degeneration, conversion gain, linearity, noise.

1. Introduction

CMOS LNAs are slowly replacing GaAs and bipolar circuits, due to rapidly improving CMOS technology that benefits greatly from transistor scaling. The source-degenerated transistor topology is widely used in numerous designs of large band LNAs and also has applications in mixers and voltage-controlled oscillators (VCOs).

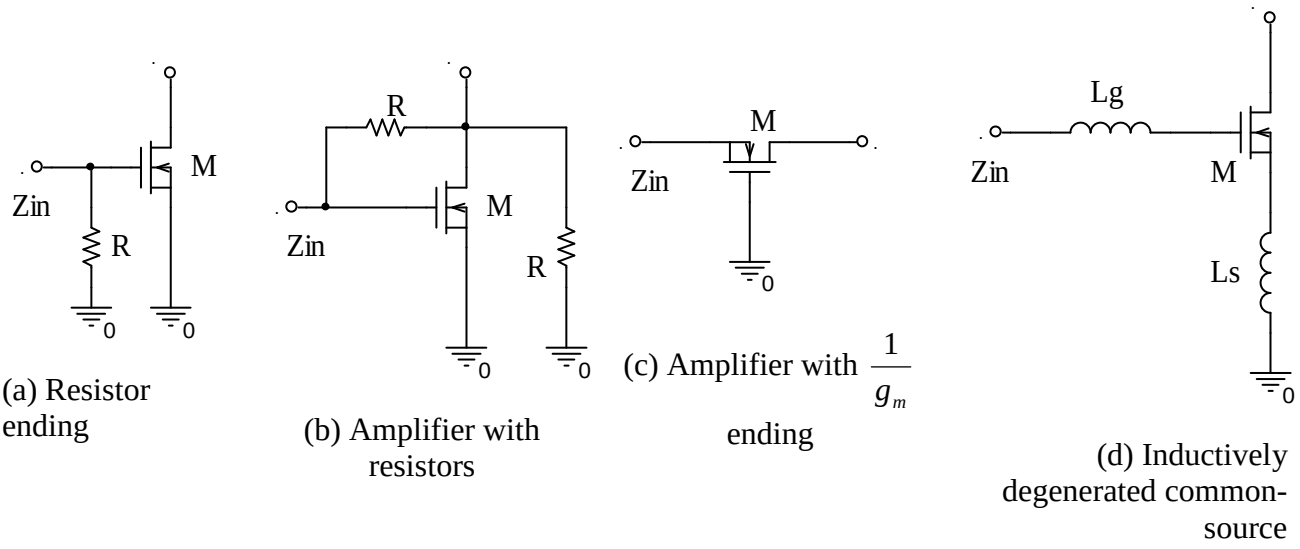
In the second part of this work, we deal, in general, inductive degeneration of LNA but in the third section we introduce an input filter while maintaining a broadband (Figure 5) and we

eventually interpreted source noises and how to optimize over several papers including the most recent like [8] which decreased the noise taking into account a certain capacity nodal Cx representing all parasitic capacitances between the two transistors cascade. As against in our work, we chose an output resonant filter with inductors mostly very low values to reduce further the noise.

The fourth part, by the Figure 10, we proposed our LNA architecture using two filters and the transistors with sizes appropriate to have a high transconductance and possibly gain still at reasonable level while ensuring a minimum of noise along our frequency range 0.8 GHz to 2.42 GHz.

2. Review of the LNA architectures using inductive source degeneration topology

The LNAs are classified into four categories. They are defined by the type of the input impedance showed at the input building block. Indeed, the compromise between the noise figure and the gain is essentially resolved by matching the LNA input. Figure 1 shows various LNA topologies commonly encountered in the bibliography [1] [2].



(a) Resistor ending

(b) Amplifier with resistors

(c) Amplifier with $\frac{1}{g_m}$ ending

(d) Inductively degenerated common-source

Figure 1: Different topologies of LNAs.

In this paper, a LNA architecture using inductive source degeneration topology is proposed and designed. As has been illustrated in several publications [3.4.7.8.9.], this architecture using inductive source degeneration gives a perfect matching without adding noise to the system and without imposing any restrictions on the g_m conductance. This perfect matching can be obtained by using two inductors: the source inductor L_S and the gate inductor L_g, as shown in Figure 2.

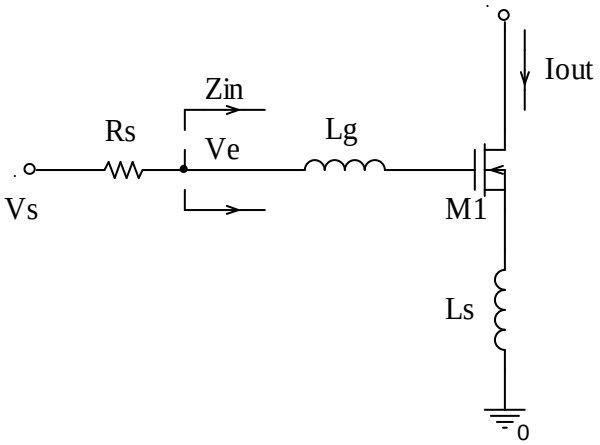


Figure 2: LNA architecture using inductive source degeneration topology

From Figure 2, the input impedance of the LNA is defined by $Z_{in} = \frac{Ve}{i_e}$ (1)

By replacing the transistor M_1 by its equivalent small signal circuit and taking into account the no quasi-static resistor of the gate transistor, the obtained equivalent circuit is shown in Figure 3:

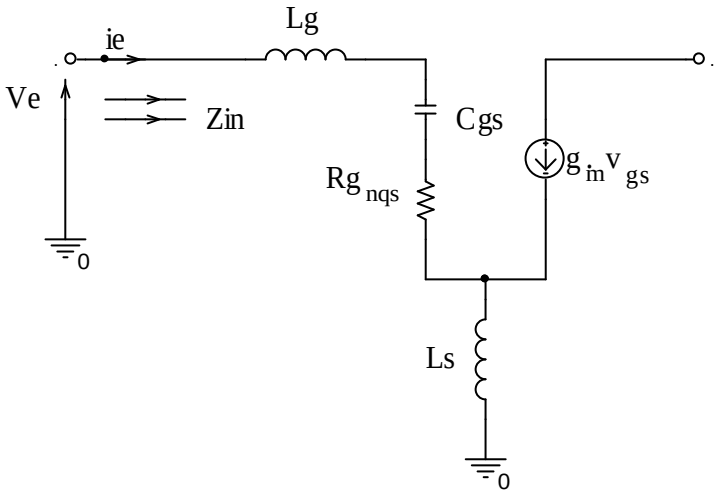


Figure 3: Equivalent circuit of LNA taking into account the $R_{g_{nqs}}$ resistor

In our frequency range a small signal analysis remains appropriate while neglecting the C_{gd} capacitor of the transistor M_1, this gives:

$$V_e = jL_g\omega i_e + \frac{1}{jC_{gs}\omega} i_e + R_{g_{nqs}} i_e + jL_s\omega\left(i_e + g_m V_{gs}\right) \quad (2)$$

$$\text{as : } V_{gs} = \frac{1}{jC_{gs}\omega} i_e \text{ , then : } \qquad Z_{in} = j\omega\left(L_g + L_s\right) + \frac{1}{j\omega C_{gs}} + \omega_T L_s + R_{g_{nqs}} \quad (3)$$

where $\omega_T = \frac{g_m}{C_{gs}}$.

At the resonant frequency, the capacitive effect cancels the inductive effect; the input impedance can be given by:

$$Z_{in}\left(\omega_R\right) = R_{eq} = \omega_T L_s + R_{g_{nqs}} \quad (4)$$

where: $\omega_R = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}}$ is the resonance frequency. In fact, the L.C resonator improves the gain of the LNA. Then, as can be shown at the input of the circuit (figure 3), the quality factor is given by:

$$Q = \frac{1}{C_{gs}\omega_R R_{eq}} \quad (5)$$

At the resonance frequency, the voltage magnitude across C_{gs} is Q multiplied by the voltage across the input, which has the effect of increasing the effective transconductance G_m of the circuit:

$$G_m = Q.g_m \quad (6)$$

Typically this Q factor reduces the noise returned by the input while increasing the gain. But the biggest handicap of this topology remains its application narrowband and bad isolation.

In Figure 4, a cascode stage is added to reduce both the interaction between the input and output and the reverse gain (form output to the input). This reduction has the effect of increasing the stability of the amplifier [2].

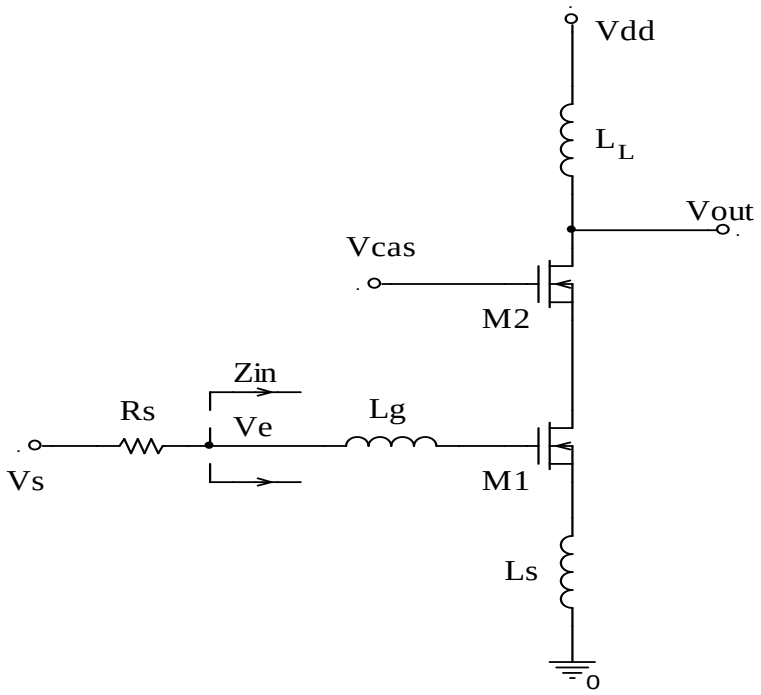


Figure 4: LNA using a cascode inductive source degeneration topology

Moreover, the cascode topology reduces the effect of the capacitor C_{gd} of M_1 by presenting a low-impedance at the drain of M_1. The output inductor L_L is chosen to resonate at the frequency of the input signal with the output capacitor.

By using this topology, we could have a wider and a smoother frequency response by aligning the resonance at the input with that of the output, which also has the effect of achieving a high gain.

3. Theoretical study of the proposed UWB LNA

In the literature, a large number of the LNA architectures are narrowband and are optimized to work for a single frequency [17], [18], [19], [20], [21]. In the proposed architecture, as shown in Figure 5, an extension of the inductive source degeneration topology is adopted to achieve a broad frequency band matching impedance.

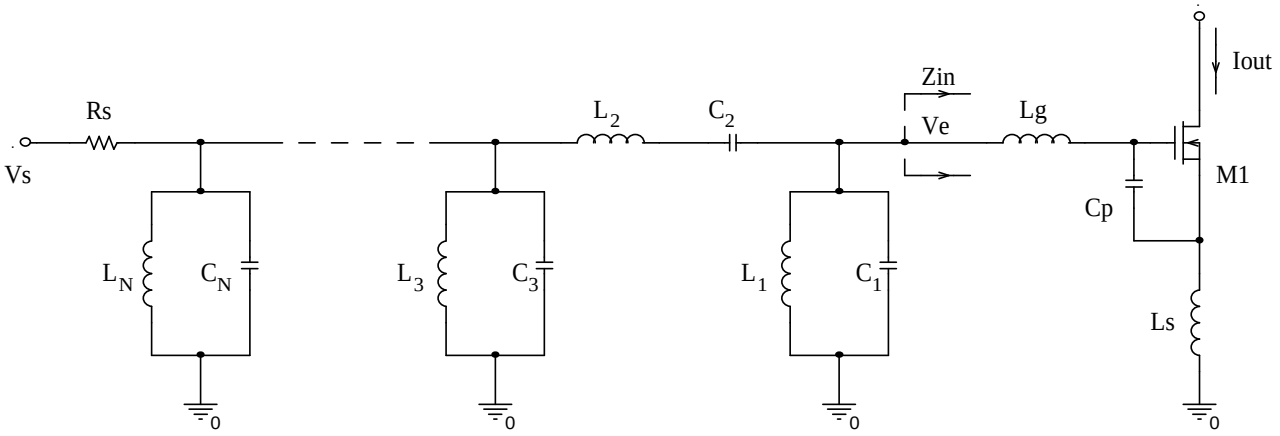


Figure 5: UWB LNA with an inductive source degeneration topology

The equation (3) can be written:

$$Z_{in} = j\omega L_t + \frac{1}{j\omega C_t} + \frac{g_m L_s}{C_t} = j\omega L_t + \frac{1}{j\omega C_t} + R_T \qquad (7)$$

where $C_t = C_p + C_{gs}$, $L_t = L_g + L_s$ and $R_T = \frac{g_m L_s}{C_t}$, the capacitor C_p has been added to increase the degree of freedom of the system, this could increases the total capacity between the gate and the source of M_1.

By combining L_i , C_i et Z_{in} (Figure 5), the architecture will be equivalent, as shown in Figure 6, to a passband filter with a output load R_T.

To ensure the design of an UWB LNA and to facilitate the implementation of inductors, a compromise must be made between the choice of the number of LC elements and the values of inductors [3], [4].

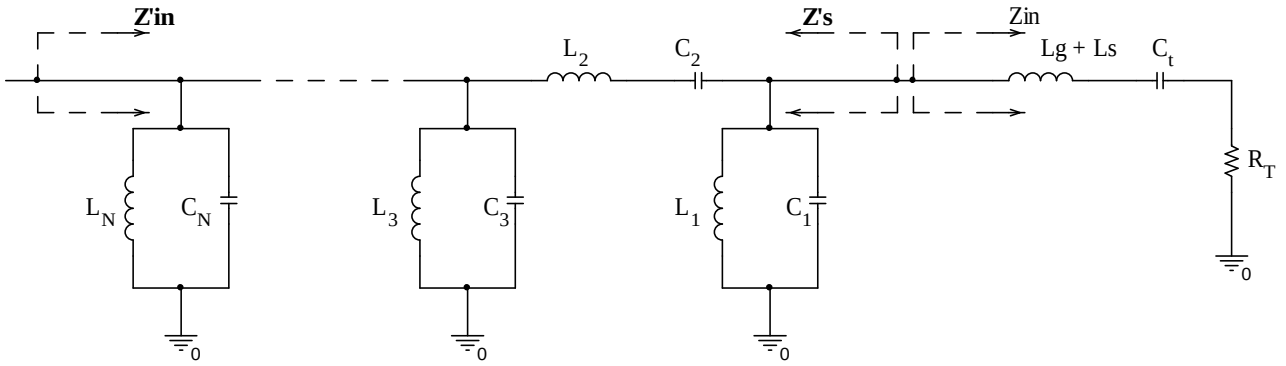


Figure 6: Input building block of the LNA

3.1 Gain calculation

The gain of the cascode LNA in Figure 4 is equal to the multiplication product of the amplification due to the transistor M_1 and that produced by the transistor M_2.

The transistor M_2 is mounted on a common base, known by the amplification of $\frac{1}{g_m}$. Then, this topology makes a good impedance matching to 50 Ω, its gain is given by:

$$A_{V_{M2}} = g_{m_{M2}}.Z_{load_{M2}} \tag{8}$$

The transfer function of the filter in Figure 6 is:

$$TF_{pb}(j\omega) = \frac{V_{R_T}}{V_{in}} \tag{9}$$

Therefore the input current i_{in} is:

$$i_{in} = TF_{pb}(j\omega).\frac{V_{in}}{R_T} \tag{10}$$

The voltage Vgs of M_1 can be found directly by multiplying the current i_{in} by the impedance across the source-gate of M_1:

$$V_{gs} = \frac{i_{in}}{j\omega C_t} = \frac{V_{in}TF_{pb}(j\omega)}{j\omega R_T C_t} \tag{11}$$

Using the equation (6), the effective transconductance of M_1 is given by:

$$G_{m_{M1}}(j\omega) = g_{m_{M1}}\frac{V_{gs}}{V_{in}} = \frac{g_{m_{M1}}.TF_{pb}(j\omega)}{j\omega R_T C_t} \tag{12}$$

At the resonance frequency, the Q factor of the circuit in figure 6 is similar to that found in equation (5):

$$Q = \frac{1}{C_t \omega_R R_t} \tag{13}$$

then $\left|G_{m_{M1}}\right| = g_{m_{M1}}.Q.\left|TF_{pb}(j\omega)\right|$ (14)

The advantage of this circuit is its effective transconductance which is depended to the quality factor Q, which will allow to increase its value.

The voltage amplification of M_1 is:

$$A_{V_{M1}} = -G_{m_{M1}}.Z_{load_{M1}} \quad (15)$$

However, M_2 is mounted on a common base, therefore, $Z_{load_{M1}} = \frac{1}{g_{m_{M2}}}$ represents its input impedance. So the voltage amplification of the LNA cascode is:

$A_V = A_{V_{M1}}.A_{V_{M2}} = -\frac{G_{m_{M1}}}{g_{m_{M2}}}.g_{m_{M2}}.Z_{load_{M2}}$, then :

$$A_V = -G_{m_{M1}}.Z_{load_{M2}} \quad (16)$$

3.2 Noise analysis

In this topology, two types of noise may persist, one comes from the quality factor of the input network, and the other comes from both the gate source noise and the drain source noise of M_1. To study the effect of noise coming from the transistor, we will follow an analysis similar to that made in reference [3].

The input transistor with source degeneration including its gate and drain noises are shown in Figure 7.a. These two sources of noise, as shown in Figure 7.b, may be replaced by a voltage source and a current source at the input:

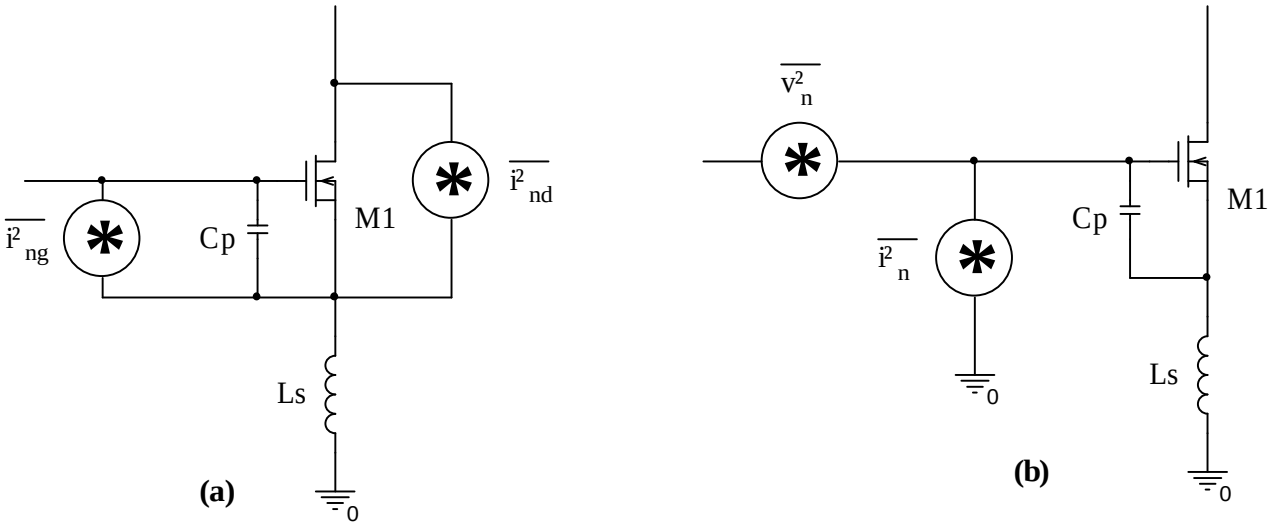


Figure 7: Models of noise in transistor M_1 with source degeneration

These sources have expressions like:

$$i_n = i_{ng} + \frac{j\omega C_t}{g_m} i_{nd} \quad \text{and} \quad v_n = j\omega L_s i_{nd} + \left(1 - L_s C_t \omega^2\right)\frac{i_{nd}}{g_m} = \frac{i_{nd}}{g_m} + j\omega L_s i_n$$

Their spectral densities can be given by:

$\overline{i_{nd}^2} = 4K_B T\gamma g_{d0}\Delta f$ and $\overline{i_{ng}^2} = 4K_B T\delta \frac{\omega^2 C_{gs}^2}{5g_{d0}}\Delta f$ correlated with a coefficient:

$c = \frac{\overline{i_{ng}.i_{nd}^*}}{\sqrt{i_{ng}^2.i_{nd}^2}} \approx -0.395j$ with g_{d0} is the drain-source conductance at V_{ds} = 0V.

The value of the technological parameter γ is typically 2 to 3, because of heating due to the intense electric field in short channels of CMOS transistors.

$\delta = 2.\gamma$ is the noisy coefficient of the gate.

Indeed, there is a correlation between the noise generator current and voltage thus:

$i_n = i_c + i_u$, where i_c is the correlated part with v_n and i_u is the correlated part with i_n, then:

$i_c = Y_c.v_n$, Y_c is the admittance of correlation.

However, the noise figure is given [5]:

$$F = \frac{\overline{i_s^2} + \overline{\left|i_n + Y_s v_n\right|^2}}{\overline{i_s^2}} \tag{17}$$

With i_s and Y_s are respectively the current and the admittance of source. Thus:

$$F = \frac{\overline{i_s^2} + \overline{\left|i_u + (Y_s + Y_c)v_n\right|^2}}{\overline{i_s^2}} = 1 + \frac{\overline{i_u^2} + \left|Y_s + Y_c\right|^2 \overline{v_n^2}}{\overline{i_s^2}} \tag{18}$$

This last expression shows that the noise is caused by three independent sources whose resistance and the admittances defined by:

$$R_n = \frac{v_n^2}{4K_B T\Delta f}\ , \quad G_u = \frac{i_u^2}{4K_B T\Delta f} \quad \text{and} \quad G_s = \frac{i_s^2}{4K_B T\Delta f}. \tag{19}$$

(18) and (19) imply : $F = 1 + \frac{G_u + \left|Y_s + Y_c\right|^2 R_n}{G_s} = 1 + \frac{G_u + \left[(G_c + G_s)^2 + (B_c + B_s)^2\right]R_n}{G_s}$ (20)

where $Y_c = G_c + j\,B_c$ and $Y_s = G_s + jB_s$. To design an optimal source which allows to generate the minimum of noise, it is important to derive the equation (20) according to its conductance G_s and its susceptance "reactance" Bs and to put the derivative to zero, the optimal values are the following:

$$\begin{cases} B_s = -B_c = B_{opt} \\ G_s = \sqrt{G_c^2 + \dfrac{G_u}{R_n}} = G_{opt} \end{cases} \tag{21}$$

This gives a minimum of noise : $F_{\min} = 1 + 2R_n\left(G_{opt} + G_c\right)$.

If we replace this in the general equation (20) of the noise, we get:

$$F = F_{\min} + \frac{R_n}{G_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right] \tag{22}$$

The expression (22) is a circle of center (G_{opt} , B_{opt}) and radius $\frac{G_s}{R_n}\left(F - F_{\min}\right)$, when F tends towards its minimum, this circle coincides with the center, but when the noise source generates a variable factor F, it will have a contour which is no longer a circle but a conical.

In the case of our circuit and considering: $\rho = \frac{C_{gs}}{C_t}$, $\chi = \sqrt{\frac{\delta}{5\gamma}}$ and $\alpha = \frac{g_m}{g_{d0}}$ (considerable factor for the short channels), the admittance of correlation between i_n and v_n and is: [3]

$$Y_c = \frac{i_c}{v_n} = G_c + j.B_c = \frac{jC_t\omega}{\dfrac{1 + |c|\rho\alpha\chi}{1 + 2|c|\rho\alpha\chi + \rho^2\alpha^2\chi^2} - L_sC_t\omega^2} \tag{23}$$

$G_{opt} = \sqrt{G_c^2 + \frac{G_u}{R_n}} = \sqrt{\frac{G_u}{R_n}}$, in references [6] and [7] a similar calculation gives:

$$G_{opt} = \frac{C_t\omega\left(1 + 2|c|\rho\alpha\chi + \rho^2\alpha^2\chi^2\right)}{\rho\alpha\chi\sqrt{1 - |c|}^2} \tag{24}$$

$$B_{opt} = -B_c = \frac{C_t\omega}{L_sC_t\omega^2 - \dfrac{1 + |c|\rho\alpha\chi}{1 + 2|c|\rho\alpha\chi + \rho^2\alpha^2\chi^2}} \tag{25}$$

as $G_u = \frac{\alpha^2 g_{d0}.\left(1 + 2|c|\rho\alpha\chi + \rho^2\alpha^2\chi^2\right)}{\gamma.\left(\rho^2\alpha^2\chi^2\left(1 - |c|^2\right)\right)}$ and $R_n = \frac{\alpha^2 g_{d\grave{a}}}{\gamma.C_t^2.\omega^2\left(1 + 2|c|\rho\alpha\chi + \rho^2\alpha^2\chi^2\right)}$

Like in reference [4] the optimal source which will generate less noise must verifies the following relation $L_sC_t\omega^2 = 1$

Then: $F(\omega) = 1 + \frac{1}{G_uR_s} + \frac{R_s}{R_n} = 1 + \frac{P(\omega)}{g_{m_{M1}}R_s}.\frac{\gamma}{\alpha}$ (26)

$$\text{Where } P(\omega)=\frac{\rho^2\alpha^2\chi^2\left(1-|c|^2\right)}{1+2|c|\rho\alpha\chi+\rho^2\alpha^2\chi^2}+R_s^2C_t^2\omega^2\left(1+2|c|\rho\alpha\chi+\rho^2\alpha^2\chi^2\right) \quad (27)$$

In fact, such analysis was made only for M_1 but the cascode stage generates also a noise source which is due to the "presence" of a parasite Nodal capacitor C_x at the drain of M_2 [8]. In our proposed design which uses a CMOS 65 nm technology, the noise due to C_x can be neglected compared to the noise of the amplifier stage based on M_1.

4. Design of the proposed UWB LNA (0.8-2.4 GHz)

The proposed UWB LNA design, using a cascade inductive source degeneration topology, is shown in Figure 8. This modified architecture contains a second order passband filter at the input. This passband filter allows achieving the desired frequency band with inductors whose values below 7 nH which permits to reach a stable gain. The modified architecture includes also a bias circuit which can be demonstrated thereafter.

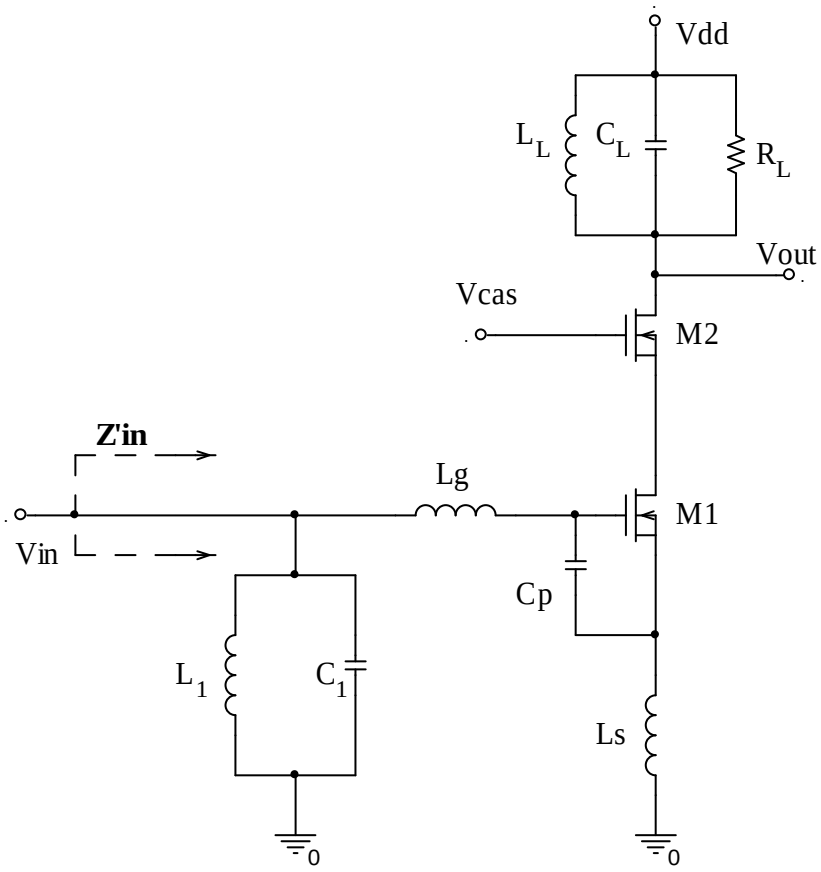


Figure 8: UWB LNA with a second order passband filter

The transistor M_1 is designed so as to have a high $g_{m_{M1}}$ to ensure a satisfactory amplification with a minimal noise, while the transistor M_2 represents a point of a low impedance to minimize the effect of the capacitor C_{gd} and to increase the isolation of the circuit.

The output of the circuit is a parallel RLC should resonate, as we will see in paragraph ($\oint$4.2.*c*), at a high frequency than the maximum of the useful frequency band. The choice of this circuit as output network to replace the "shunt peaking" method [7] comes from the reasonable value of inductance in the band 0.8-2.4GHz.

4.1. Design of the input building block (passband filter)

Figure 9 shows the passband filter which uses four poles.

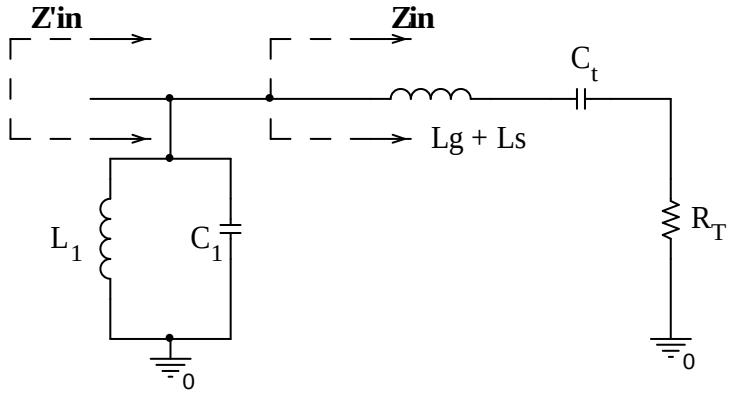


Figure 9: Equivalent circuit of the input passband filter

The calculation of the transfer function of such a filter gives:

$$\frac{V_{R_T}}{V_e} = \frac{\frac{R_T}{R} L_1 C_t . p^2}{L_1 C_1 L_t C_t . p^4 + \left(R_T C_t L_1 C_1 + \frac{L_1 L_t C_t}{R} \right) . p^3 + \left(L_1 C_1 + L_t C_t + \frac{R_T L_1 C_t}{R} \right) . p^2 + \left(R_T C_t + \frac{L_1}{R} \right) . p + 1} \quad (28)$$

V_e is the voltage across the source which has an intern resistor R = 50 Ω and p = jω is the Laplace operator.

The equation (28) can be expressed by:

$$FT_{pb}(p) = \frac{\left(\frac{\Delta\omega}{\omega_0^2} \right)^2 . p^2}{\frac{1}{\omega_0^4} . p^4 + \frac{2.\Delta\omega}{\omega_0^4} . p^3 + \left(\frac{2}{\omega_0^2} + \left(\frac{\Delta\omega}{\omega_0^2} \right)^2 \right) . p^2 + 2 . \frac{\Delta\omega}{\omega_0^2} . p + 1} \quad (29)$$

ω_0 is the central frequency of the filter and $\Delta\omega$ is the passband of the filter (difference between the high and low cutoff frequencies).

By identification, we can obtain the system of equations (30) which will allow calculating the elements of the filter.

$$\begin{cases} L_1 C_1 L_t C_t = \dfrac{1}{\omega_0^4} & (30.a) \\ R_T C_t L_1 C_1 + \dfrac{L_1 L_t C_t}{R} = \dfrac{2.\Delta\omega}{\omega_0^4} & (30.b) \\ L_1 C_1 + L_t C_t + \dfrac{R_T L_1 C_t}{R} = \dfrac{2}{\omega_0^2} + \left(\dfrac{\Delta\omega}{\omega_0^2}\right)^2 & (30.c) \\ R_T C_t + \dfrac{L_1}{R} = 2.\dfrac{\Delta\omega}{\omega_0^2} & (30.d) \\ \dfrac{R_T L_1 C_t}{R} = \left(\dfrac{\Delta\omega}{\omega_0^2}\right)^2 & (30.e) \end{cases} \quad (30)$$

(30.c) – (30.e) $\Rightarrow$ $L_1 C_1 + L_t C_t = \dfrac{2}{\omega_0^2}$, considering $L_1 C_1 L_t C_t = \dfrac{1}{\omega_0^4}$ then:

$$L_1 C_1 = L_t C_t = \frac{1}{\omega_0^2} \quad (31)$$

By substituting (31) in (30.b), we get:

$$R_T C_t + \frac{L_1}{R} = 2.\frac{\Delta\omega}{\omega_0^2} \quad (32)$$

(32) and (30.e) imply:

$$R_T C_t = \frac{L_1}{R} = \frac{\Delta\omega}{\omega_0^2} \quad (33)$$

We have three equations (31), (32) and (33) linearly independent and five unknown, a choice must be made to set two unknowns and therefore find the values of others. Indeed, the values of R_T and R (the source resistor) have been set to 50 Ω, this could achieve a good impedance matching. What gives:

$$\begin{cases} L_1 = 6.49nH \\ L_t = 4.97nH \end{cases} \text{ and } \begin{cases} C_t = 2.6\,pF \\ C_1 = 1.99\,pF \end{cases} \text{ considering } L_t = L_g + L_s \text{ and } C_t = C_p + C_{gs}$$

R_T is equal to $\dfrac{g_{m_{M1}}.L_s}{C_t}$ then :

$$L_s = \frac{R_T C_t}{g_{m_{M1}}} \tag{34}$$

To set the values of Ls and Cp, we have configured the size of the transistor M1 in order to deduce the values of $g_{m_{M1}}$ and Cgs .

4.2. Sizes of M_1 and M_2

a. Transistor M_1

Considering the useful frequency band (0.8 GHz - 2.4 GHz) and the technology adopted (CMOS 65nm), we can write:

$$i_{D1} = \frac{g_{m_{M1}}}{2}\left(V_{gs_1} - V_T\right) \tag{35}$$

Where i_{D1} is the current drain of M_1 and V_T is its threshold voltage conduction.

$$g_{m_{M1}} = \mu_n . C_{OX} \frac{W}{L}\left(V_{gs_1} - V_T\right) \tag{36}$$

Where C_{OX} is the surface capacitor of the gate-channel of M_1, μ_n is the mobility of carriers; L and W are respectively the gate length and the channel width of the M_1 transistor.

From the reference [10] and by considering the CMOS 65 nm technology with a voltage supply V_{DD} equals to 1.8 V, we can have: $\mu_n = 0.0218 m^2/V.s$ and $C_{OX} = 18.6\times10^{-15} F/\mu m^2$.

The current i_{D1} is fixed equal to 16 mA to minimize the power consumption lower than a threshold of 30 mW.

To minimize the variation effect of V_T according to the temperature, a series of simulation have been realized. The result is that, for a difference of potential $V_{gs1} - V_T$ approximately equal to 0.16 V the quotient $\frac{W}{L}$ is sufficiently higher. This gives, from relation (35), a suitable transconductance $g_{m_{M1}}$ which is roughly equal to 200 mA/V.

By replacing the value of $g_{m_{M1}}$ in (36) we obtain. $\frac{W}{L} = 3082.77$.

By considering L = 0.1 µm this gives $W \approx 308.2$ µm.

$C_{gs1} = \frac{2}{3}.C_{OX}.W.L$ then C_{gs1} = 0.382 pF.

$C_p = C_t - C_{gs1}$ = 2.22 pF. From equation (34) L_s = 650 pF, then $L_g = L_t - L_s$ = 4.32 nH.

b. Transistor M_2

The size of the transistor M_2 has been chosen equal to that of M_1 to improve its isolation and ensure the stability of the circuit while minimizing the effect of capacitor C_{gd}.

c. Design of the output building block

In the relation (16) $Z_{load_{M2}}$ is a RLC parallel circuit, as illustrated on Figure 8, its components must be sized according to the total gain of the circuit.

$$Z_{load_{M2}} = \frac{L_L.P}{L_L C_L.p^2 + \frac{L_L}{R_L}.p + 1} \tag{37}$$

$$\begin{cases}(12)\\(16)\\(37)\end{cases} \quad \Rightarrow \quad A_V = \left(- g_{m_{M1}}.\frac{L_L.P}{L_L C_L.p^2 + \frac{L_L}{R_L}.p + 1} \right).\left(\frac{1}{R_T C_t p} \right).TF_{pb}(p) \tag{38}$$

Knowing that $R_T = \frac{g_{m_{M1}} L_s}{C_t}$ then the total gain A_V writes as:

$$A_V = -\frac{L_L}{L_s}.\frac{1}{L_L C_L.p^2 + \frac{L_L}{R_L}.p + 1}.TF_{pb}(p) \tag{39}$$

L_s is set equal to 4.32 nH, to increase the gain A_V we can adjust the value of L_L but an excessive value may deteriorate the frequency response of the gain. This may occur if the cutoff frequency of the lowpass filter, produced by the RLC parallel circuit, becomes lower than the high cutoff frequency of the passband filter.

A compromise must be made, a cutoff pulsation ω_c of the RLC network roughly equal to 3 GHz has been choosing. Then:

$$\begin{cases} L_L C_L = \frac{1}{\omega_c^2} \\ \frac{L_L}{R_L} = \frac{2.\zeta}{\omega_c} \end{cases} \tag{40}$$

where ζ is the damping coefficient which must be less than $\sqrt{2}$ to ensure a resonance at the cutoff frequency. We have considering that $2.\zeta = 1$ and $R_L = 50\ \Omega$ to ensure a perfect impedance matching. Then:

$L_L = 2.65$ nH and $C_L = 1.06$ pF.

4.3. Full schematic of the proposed UWB LNA

In figure 10, the bias circuit is a current mirror cascode, with transistors M_{b1} and M_{b2} identical to those of the LNA.

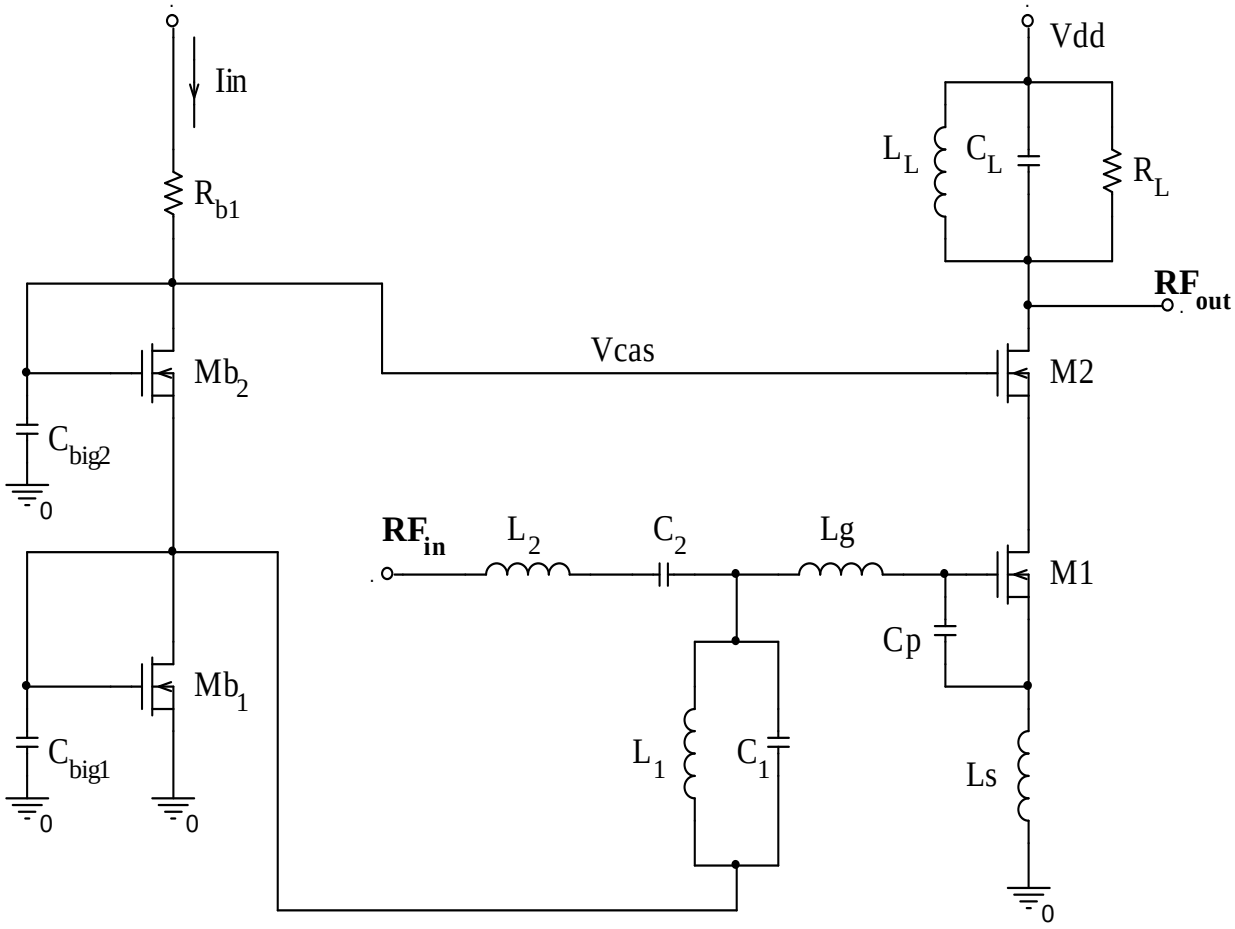


Figure 10: Full schematic of the circuit (LNA and the bias circuit)

The values of the components founded, by theoretical calculation, don't really reach the performance needed. Indeed, the power gain is below 10 dB and the matching at the input is above than -10 dB.

After several simulations, optimal results are found and illustrated in Table 1.

	L_1(nH)	C_1(pF)	L_g(nH)	L_S(pH)	C_p(pF)	C_{gs}(pF)	L_L(nH)	C_L(pF)	R_L(Ω)
Theoretical value	6.49	1.99	4.32	650	2.22	0.382	2.65	1.06	50
Adjusted value	4.97	2	4.277	700	1.673	0.382	4	1	350

Table 1 : Theoretical and adjusted values of input and output of the LNA network

For the isolation of RF signal and the circuit, a LC circuit has been added at the input of the passband filter which has the same values as L_t and C_t in order to not affect the transfer function of the input filter.

The table 2 shows a performance comparison with the results obtained in recent publications.

Paper	Tech	S11[dB]	Gmax [dB]	B[GHz]	N.F[dB]	IIP3 [dBm]	ICP [dBm]	P_{diss} [mW]
[11]	0.18µm CMOS	<-10	17.8	2.4~ 3.3	3.5~5	-13	-17	39.6
[12]	TCMC0.18µm	<-10	17.5	0.86~ 0.96	4.1	5.4~14.3	-4.5	15.5
[13]	0.18µm CMOS	<-8.7	13.1	3.1~12.2	2.7~4.9	--	--	13.9
[14]	90 nm CMOS	-10	14.6		<5.5	--	--	24
[15]	0.13µm CMOS	-15	12		8.8	--	--	54
[16]	65nm	-16.84	10.02		8.68	--	--	18.5
This Work	65 nm CMOS	<-10	14.35	0.8~2.4	1.4	5 à 14	-5 à 3	29

Table 2: Comparison of the UWB LNA performance with recent publications

5. Design results and discussions

5.1 Gain of the UWB LNA

The figure 11 shows the gain versus the input frequency for various input powers ranging from -40 dBm to -5 dBm. It is shown that the gain has a form similar to a passband filter amplified by approximately 14.35 dB.

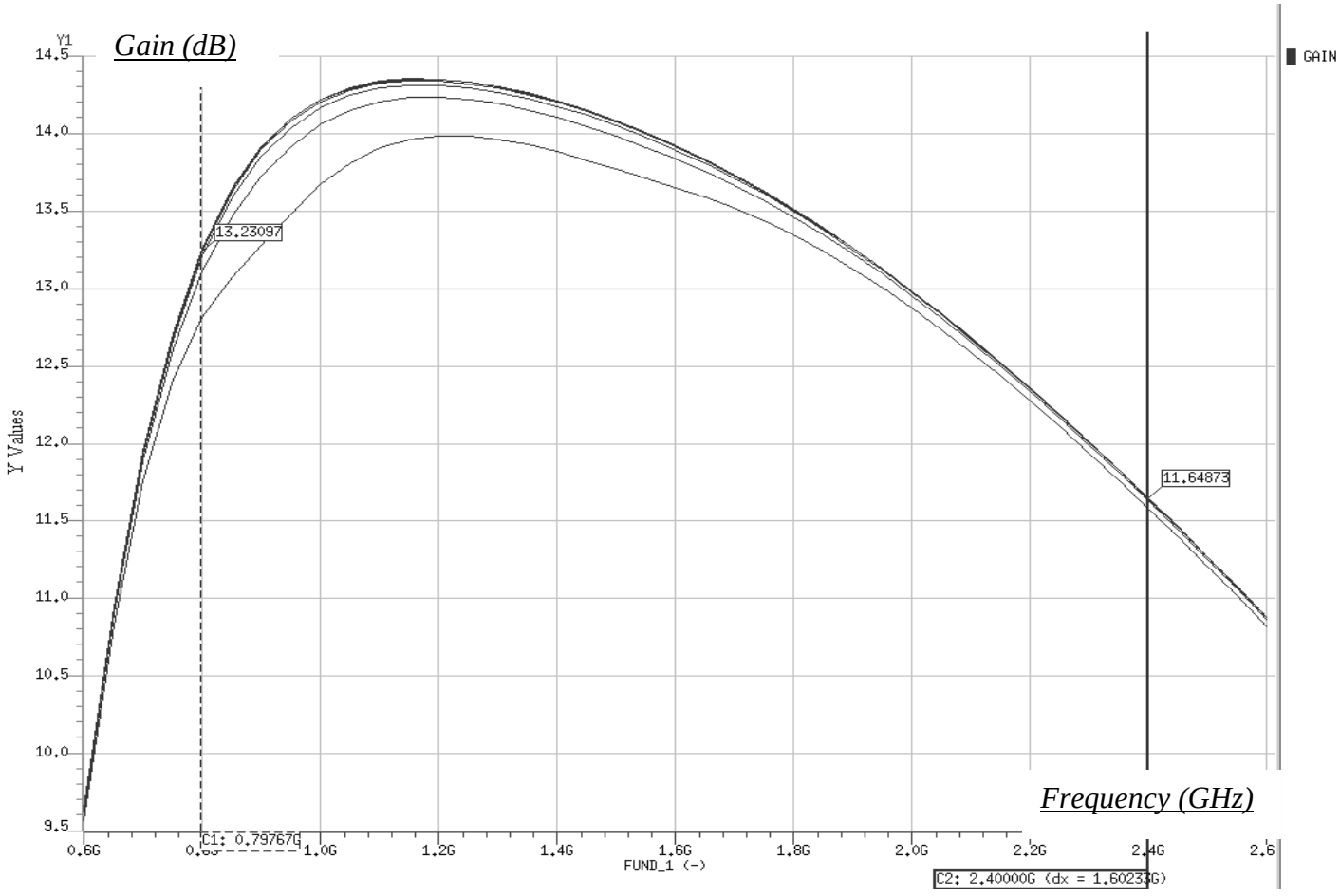


Figure 11: Gain versus frequency for different values of the power input

5.2 Non-linearity of the UWB LNA

As has been shown, the gain decreases depending on the input power. This can explain the non-linearity of the system illustrated by figures 12 and 13.

Figure 12 shows that the compression of the gain comes from the saturation of the output power.

The 1-dB compression point (for which the gain decreases by 1 dB compared to its maximum value) is located at 1.6 GHz around an input power roughly equal to 0 dBm.

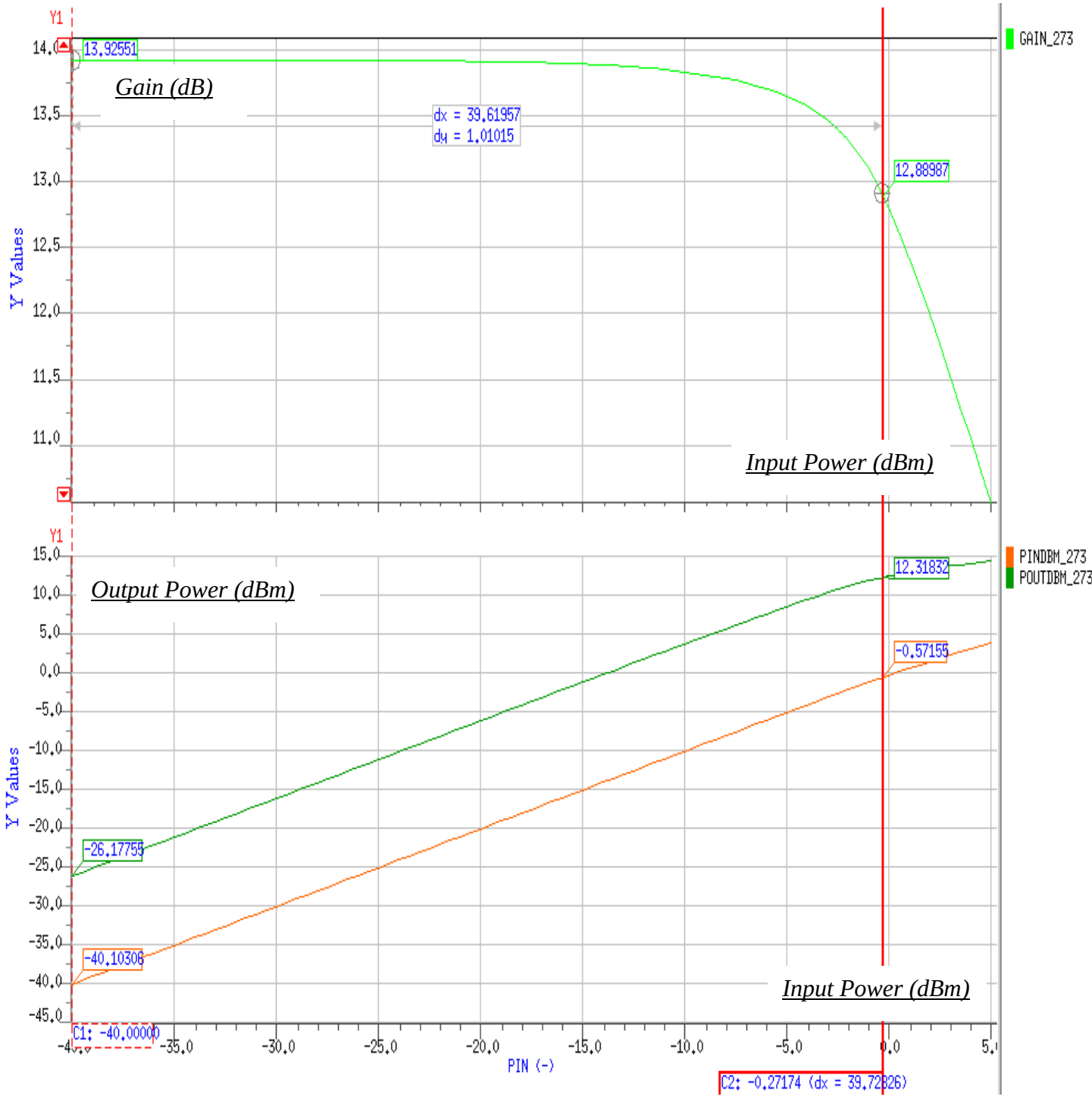


Figure 12: Gain and output power versus input power

To illustrate the behavior of the 1-dB compression point. Different 1-dB compression points have been simulated for various frequencies. The results are shown in figure 13.

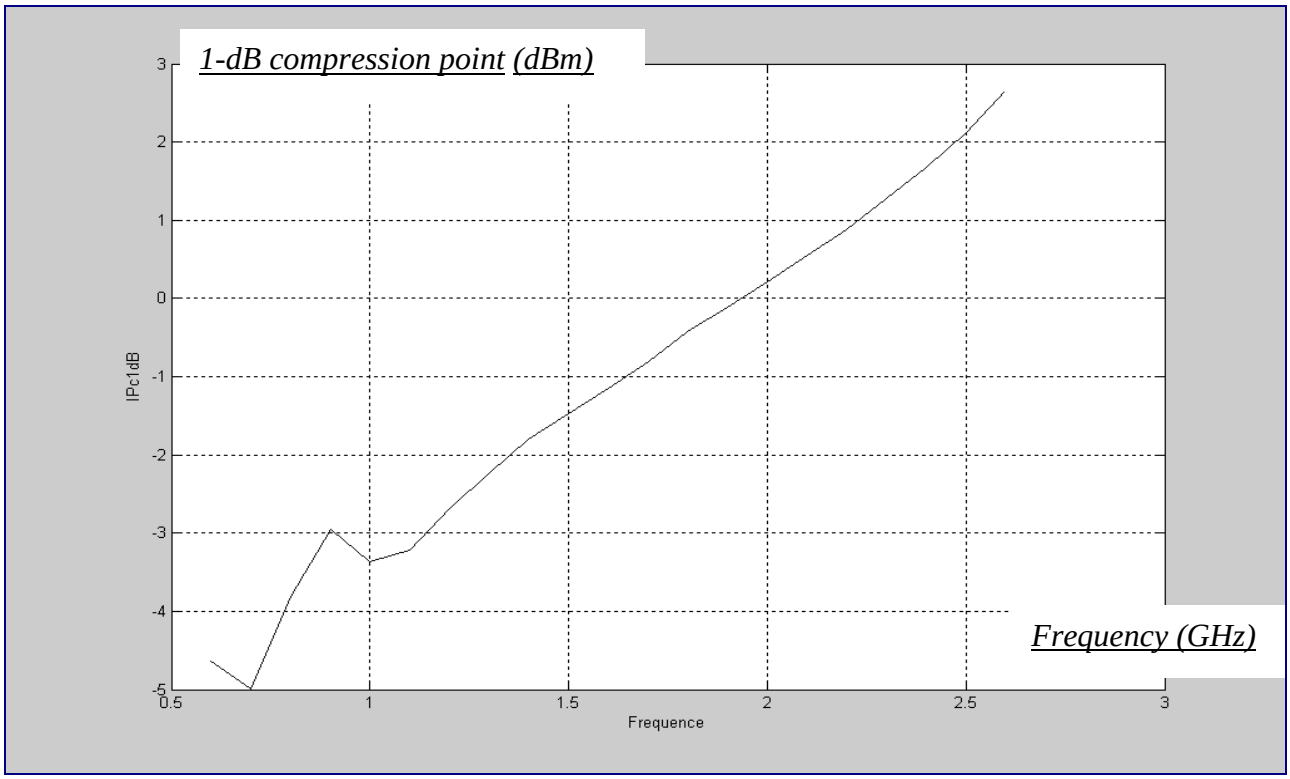


Figure 13: 1-dB compression point versus frequency

Then, the 1-dB compression point (ICP) does not depend exclusively on the input RF power but also on the RF frequency. For our frequency range [0.8 GHz, 2.4 GHz], the ICP varies between -3 and 3 dBm.

Figure 14 shows both the 3rd order interception and the 3rd intermodulation points versus frequency for different values of the input power.

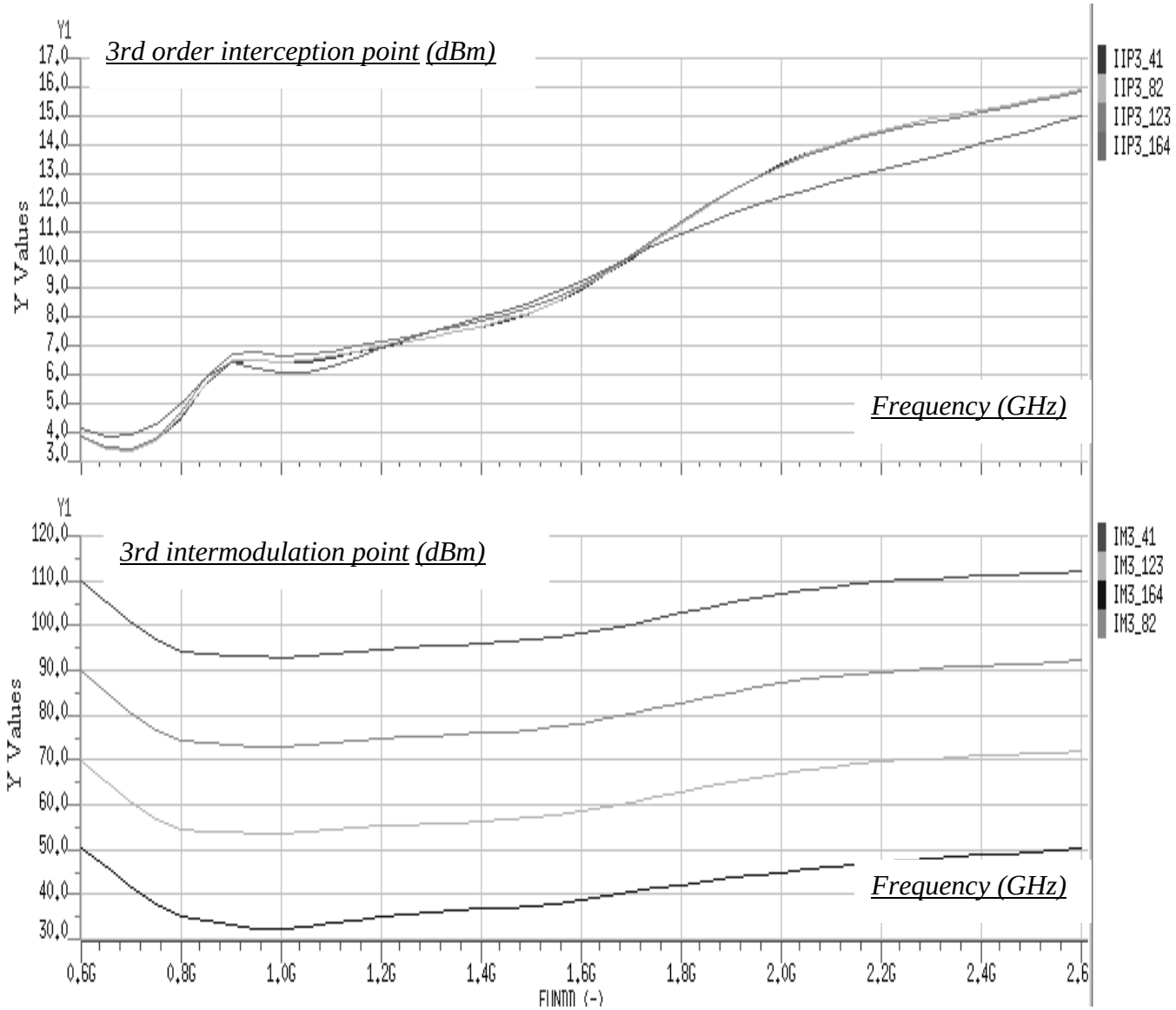


Figure 14: IIP3 and IM3 versus frequency

From these results, a very good linearity values have been achieved. This shows the high level of linearity of this designed UWB LNA.

5.3 S parameters

These parameters give an idea in term of both the gain of the circuit (S_{21}) and insertion loss between the input and the output ports of the circuit.

As illustrated in Figure 15, the S_{11} and S_{21} parameters are simulated for frequencies ranging from 0.6 to 2.6 GHz and for input powers ranging from -40 dBm to 0 dBm

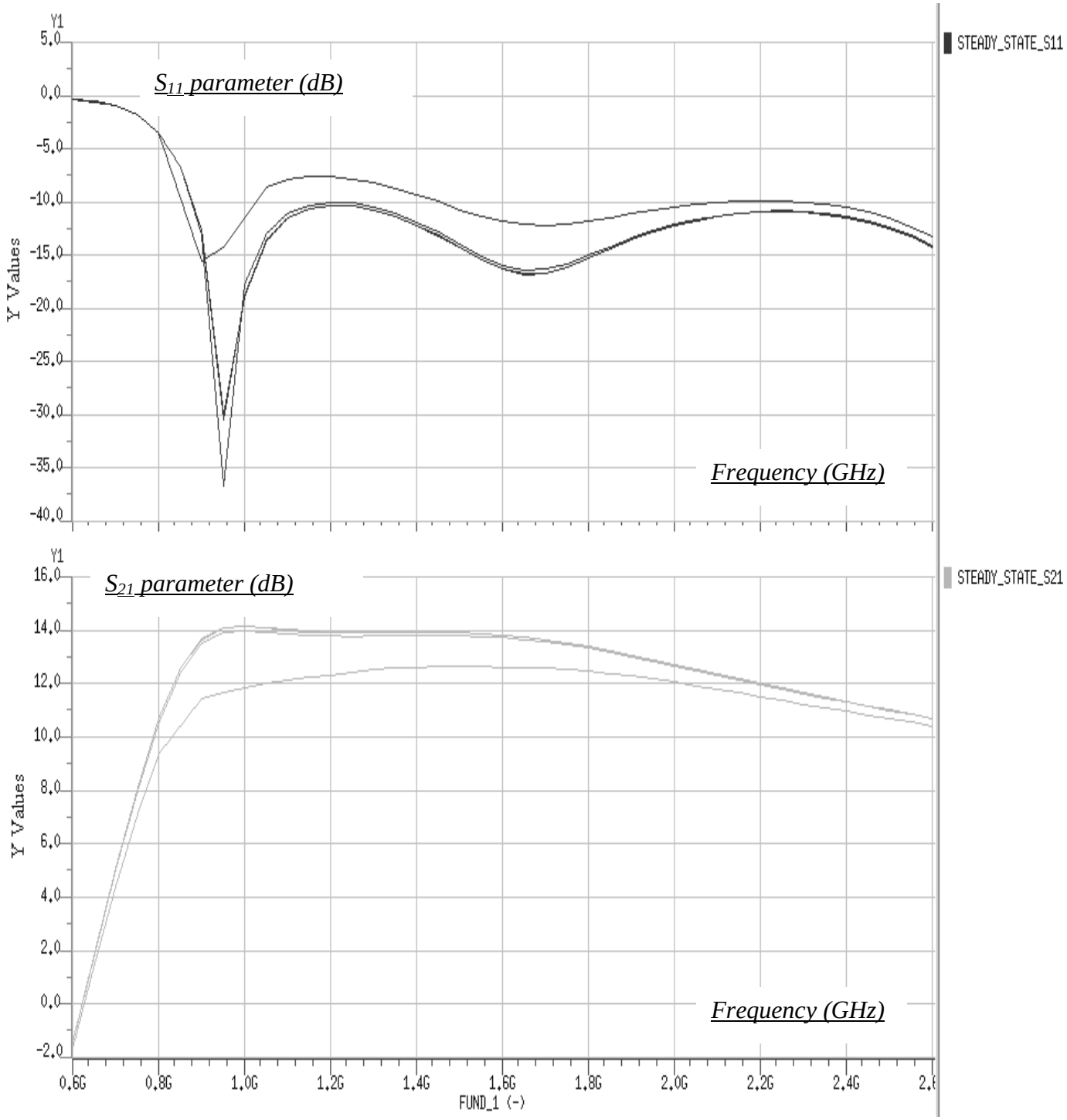


Figure 15: S_{11} and S_{21} parameters versus frequency

It is shown that the S_{11} parameter is largely below -10 dB for all frequencies in the band and for input powers below-10 dBm. However, the S_{21} parameter, which reflects the performance of the system in terms of gain, is above 11 dB.

5.4 Noise

Figure 16 shows the noise figure of the UWB LNA over the frequency band from 0.6 to 2.6 GHz with various input power values ranging from -40 dBm to -10 dBm.

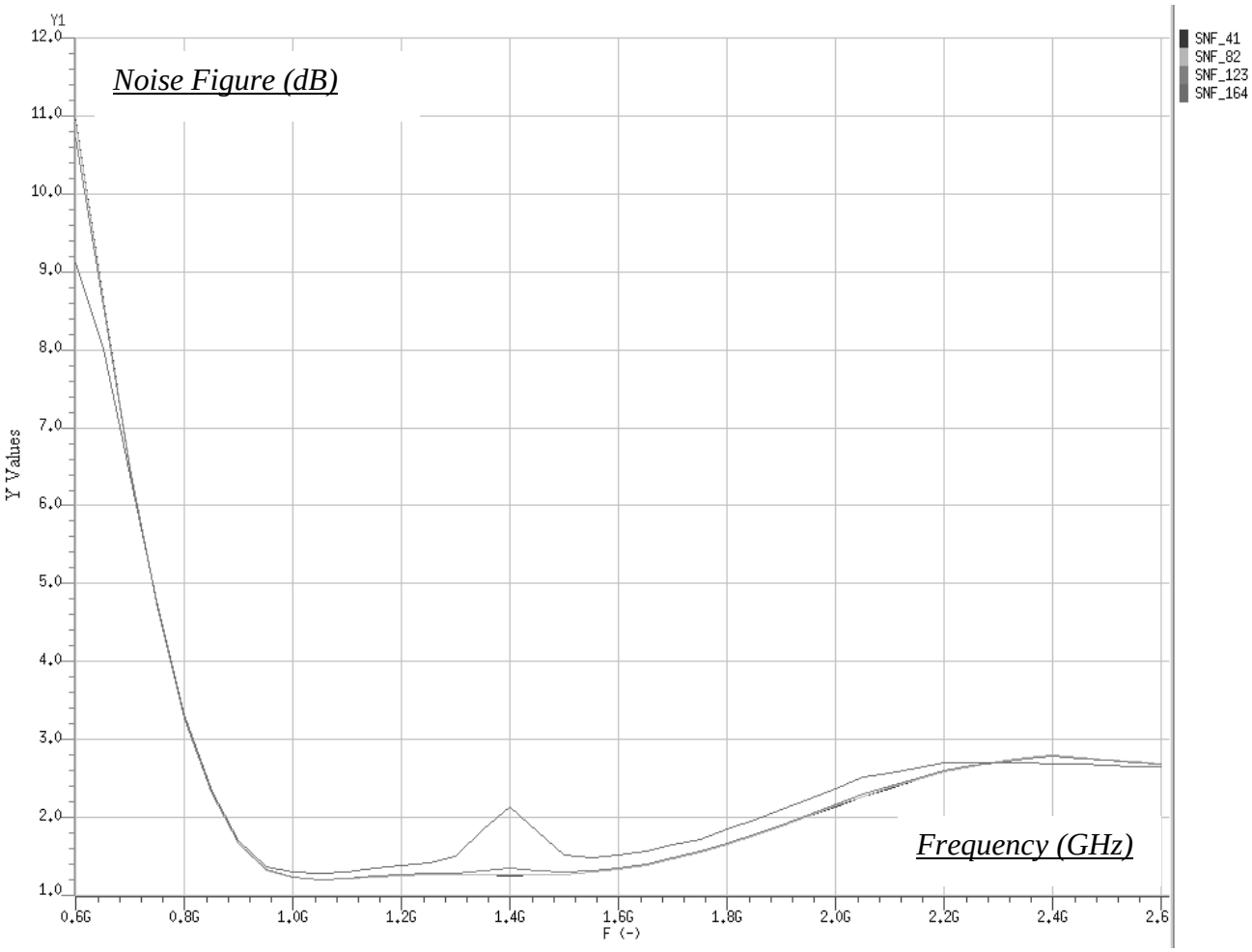


Figure 16: Noise figure versus frequency

It is shown that the noise figure is roughly the same for different values of input power, only for -10 dBm an unusual peak is observed for 1.4 GHz frequency. Typically for low-frequencies the 1/f noise is dominant, however, for the medium frequencies a minimum noise is obtained. But the noise increases slowly when the frequency increases. the high frequencies show much noise than in the previous band but it still satisfactory because $(C_{gs}\omega)^2 << 1$ over the frequency band studied.

Finally, we have found that a low noise is obtained through a large g_m, a large I_d involves a large α. What is in conformity with the noise analysis made in paragraph 3.

5. Conclusion

A modified LNA architecture for UWB applications has been studied and designed using CMOS 65 nm technology. The proposed architecture uses a cascade inductive source degeneration topology and could operate in a broad frequency band from 0.8 GHz to 2.4 GHz. The obtained results of this design show good performances. Indeed, this circuit shows a good gain, a 1-dB compression point and a 3-order interception point very large over the frequency band of operation which justifies the excellent linearity of this topology. The designed UWB LNA shows a noise

figure equals to 1.4 dB and a good isolation lower than -10 dB with an acceptable power consumption which not exceeds 29 mW.

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