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CMOS RF Switched Capacitor Bandpass Filter Tuned by Ring VCO

Ahmed El Oualkadi, Jean-Marie Paillot, Hervé Guegnaud, and Rachid Allam

Abstract **A new RF switched capacitor bandpass filter and its command circuit made up of a ring voltage controlled oscillator with 'XOR' gates are proposed. Implemented in a standard 0.35 μm CMOS technology, this circuit is intended to be used in a subset of professional mobile phone applications [380-520 MHz]. Experiments carried out on a prototype show a tunable center frequency range of 260 MHz [240-500 MHz], with a quality factor that can be as high as 300.**

Keywords **Analog IC, Tunable filters, Switched capacitors, High-Q, Ring VCO.**

1. Introduction

The growth in wireless communications systems, such as cellular telephony, demands continuous efforts towards the improvement of radio frequency (RF) performances of integrated filter devices. For few years, switched capacitor structures have been widely used for the design of stable, accurate and high-Q filters for operating frequencies below the megahertz range [1, 2]. An attractive feature of these filters is the possibility to be implemented by using a low-cost CMOS technology, which guarantees a great increase in their operating frequency range [3, 4].

However, the main advantage of switched capacitors filters over the passive ones is their center frequency which is easily tunable over a broadband of frequencies by an internal or external command circuit. In addition to this, they can be fully integrated in silicon, unlike surface acoustic wave (SAW) filters which are generally off-chip [5].

The critical limitation of switched capacitors filters is related to the construction of the RF command circuit. In this paper, an original solution is proposed, which uses a ring voltage controlled oscillator (VCO) associated with 'XOR' gates to command the switches. The new association of such command circuit and the switched capacitor filter provides broadband tuning in the RF range, allowing to sweep different channels with a high quality factor. This kind of filters could be a very attractive solution for the design of zero IF (intermediate frequency) receivers used in radio communication systems.

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2. Switched capacitor filter

2.1 General principle

The behavior of the proposed filter can be explained by the theoretical approach of the N-path filters. Several papers [6, 3, 2] have already described this kind of filters.

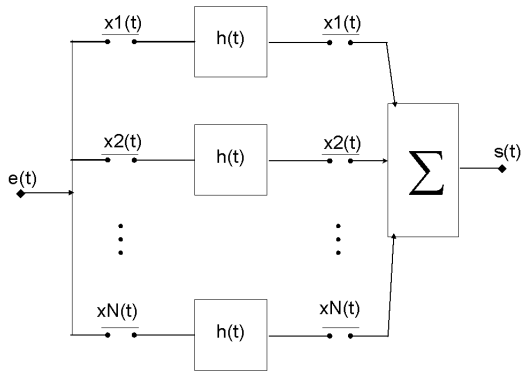

Fig. 1. General structure of N-path filter (Sampling filter).

The schematic of an N-path filter is shown in Fig. 1. The N cells of this sampling filter are successively activated by command signals applied to the switches. These cells are identical first-order RC low-pass filters. Their transfer function and the impulse response are respectively noted H(f) and h(t).

In a first approach, the command signals of the switches are considered to be Dirac's impulses δ(t) spaced by a To period. Then, the total transfer function Hs(f) of the filter is the result of the transfer function of the elementary RC low-pass filter transposed around the switching frequency (F_0=1/T_0) and all their harmonic components (Fig. 2). Consequently, this sampling filter can be used for clock recovering [7, 8] by filtering the harmonic components. It can be also used as bandpass filter centered around the

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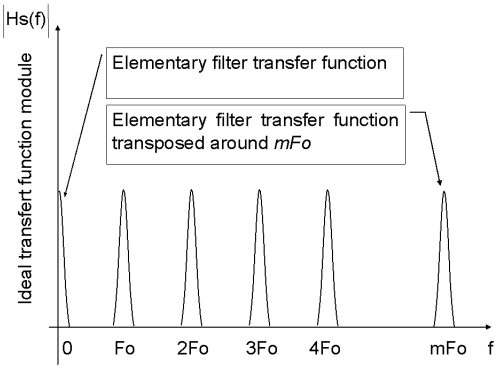

Fig. 2. Theoretical transfer function obtained with command Dirac's impulses.

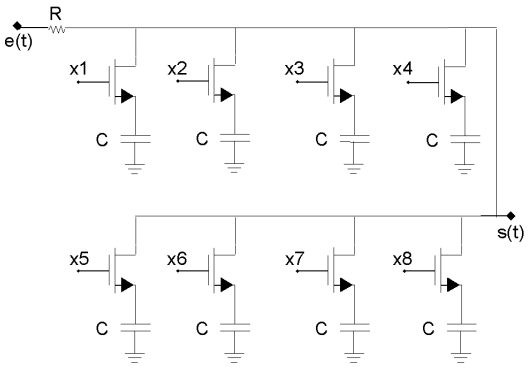

Fig. 3. Switched capacitor filter schematic, with eight switched capacitors.

fundamental switching frequency F_0. This application will be discussed in the present paper.

2.2 Switched capacitor filter design

Due to the complexity of the previous architecture (Fig. 1) at very high frequencies and particularly to the difficulty of performing an ideal switching, the proposed filter has the configuration shown in Fig. 3. This simplified structure presents, under some conditions, properties identical to the proprieties of the N-path filter [9].

The switches are implemented by using NMOS transistors sequentially controlled in ON-OFF states. Thus, they are successively closed with a switching period T_0, during a time T_0/N.

Concerning the general principle, the number of cells could be odd or even, and the choice of cells number could be discussed according to filtering requirements of targeted applications. To limit chip complexity a number of eight cells (N=8) is chosen for this study. This number seems to be a good trade-off between selectivity (in first approximation [10], $Q=\pi.N.R.C.F_0$) and chip complexity.

The switching transistors size is critical and should be optimized. Indeed, the transposed transfer characteristic is not only due to the RC components, but integrates the parasitic resistance R_{on}. This resistance provides a zero in the elementary transfer characteristic which generates the 'floor' of the filter. Consequently, a large width gate of switched transistor insures a low R_{on} resistance and a significant parasitic capacitance C_{ds}. Such a choice limits the filter bandwidth and attenuates the dynamic range of the filter. With a small width gate, the C_{ds} value is negligible but the R_{on} resistance value is important. Under these conditions, the dynamic range is still degraded by the increase of the 'floor' of the transfer characteristic. Transistors used in this design are channel N MOSFETs composed of six fingers with an elementary gate width of 25 μm and a length of 0.35 μm. These transistors present a resistance R_{on} of 30 Ω and a drain-source capacitance C_{ds} of 0.06 pF, to give an optimal dynamic range.

3. Filter command circuit

3.1 General principle

The main role of the command circuit is to generate the switching signals to commutate the capacitors. The classical command circuit was generally implemented using a shift register. That solution, which required a clock frequency equal to the center frequency of the filter multiplied by the number of cells to commutate, was exclusively used at low frequencies. Therefore, a new command circuit is proposed. It consists of a ring voltage controlled oscillator with 'XOR' gates.

First let us consider a ring VCO consisted of N differential delay cells (Fig. 4).

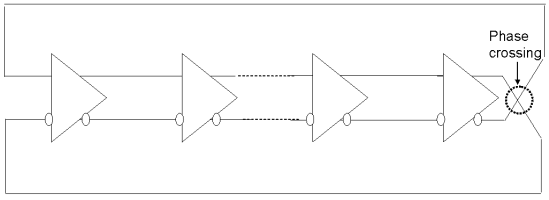

Fig. 4. Ring VCO with N differential delay cells.

If a phase crossing is made in the loop, then the ideal input and output signals of one cell are shown in Fig. 5. An 'XOR' gate between the input and the output, allows to get the required impulses for which the period and duration are respectively equal to To and To/N. Then the N command signals of the filter are obtained by placing N 'XOR' gates between each delay cells.

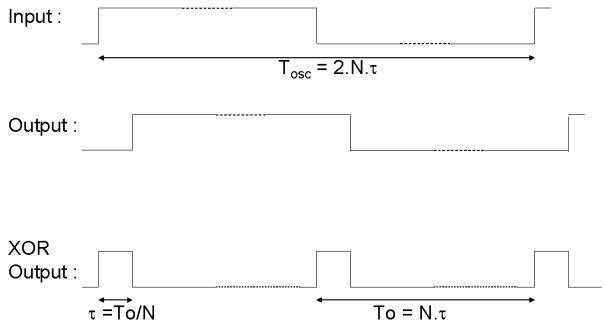

Fig. 5. Theoretical command signals obtained at the 'XOR' gates ouputs.

This proposed solution for generating the command signals is completely independent of the choice of the cells number. Then, it can be applied whatever this number (odd or even), and it must be equal to the switched capacitors number of the filter.

3.2 Filter command circuit design

To command the proposed switched capacitor filter (Fig. 3), a command circuit with eight cell is sufficient. Fig. 6 shows the proposed command circuit, the ring VCO comprises eight identical differential delay cells. Each cell is based on two NMOS transistors composing a differential amplifier (Fig. 7), to provide both the gain and the delay required for the oscillation phenomena.

The total delay cumulated with the eight cells is equal to $2.T_0$, and imposes a $F_0/2$ oscillation frequency. The delay generated by one cell depends on the time-constant $R_p.C_p$. The C_p capacitance is due to the 0.35 pF capacitor placed between drain and source of each PMOS transistor. The R_p resistance corresponds to the differential resistive load, which is obtained by PMOS transistors working in triode operation region. The oscillation frequency is tuned by controlling both the common current source and the bias point of the PMOS transistors which modify the R_p value, between 800 Ω and 1.5 KΩ.

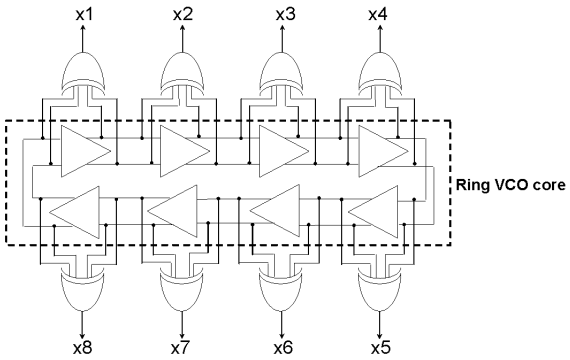

Fig. 6. Command circuit consisting of ring VCO with 'XOR' gates.

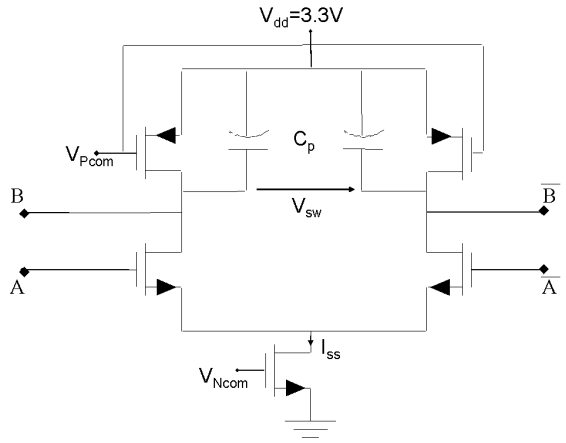

Fig. 7. Delay cell with NMOS differential amplifier.

According to the general principle, the ring VCO period with N=8 delay stages is roughly 2.N times the delay per stage. This translates to a center frequency of :

$$F_{osc} \approx \frac{1}{2.N.\tau} \approx \frac{1}{2.N.C_p.V_{sw}}$$

The PMOS gate bias voltage controlled the full I_{ss} current flowing through the load device R_p, with a drain to source voltage of V_{sw} is seen across it (Fig. 7).

$$F_{osc} \approx \frac{1}{2.N.C_p.R_p}$$

Fortunately, differential delay cells with PMOS active loads are easily tuneable over a wide range of frequencies. Knowing the main characteristics of the

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CMOS technology, it is possible to determine the frequency range [11].

This oscillation frequency range is limited at low frequency by the large swing of V_{sw} voltage. This swing voltage must stay in the linear region to avoid the saturation effects which would generate some distortions.

Interestingly, the maximum output frequency has the same technology dependence as the unity current gain frequency of the individual devices, f_T. Consequently, the maximum oscillation frequency is limited by the loop gain which theoretically must be higher than 1.

Fig. 8-a shows the architecture used for the 'XOR' gates. To generate the $F_0/2$ frequency the ring VCO requires eight differential amplifier delay cells providing the delayed output signals (0^o-180^o).

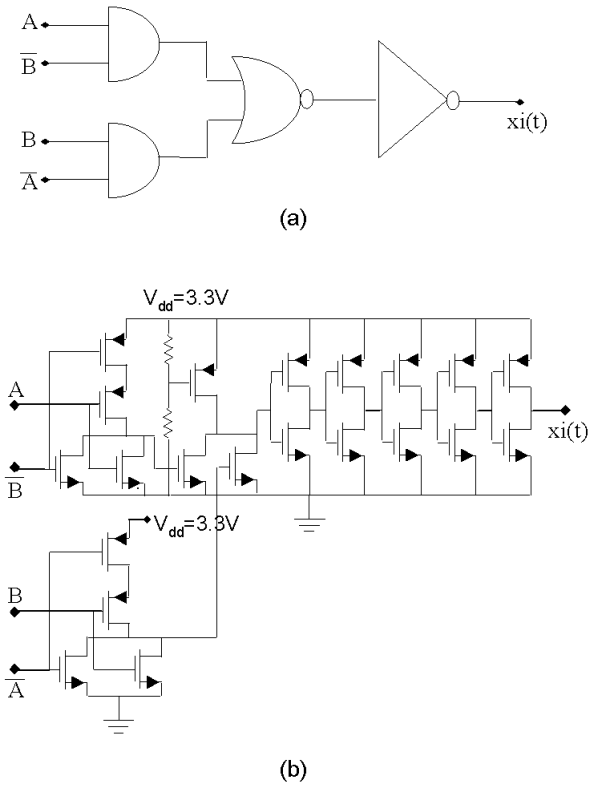

Fig. 8. 'XOR' gate, (a) architecture of the 'XOR' gate, (b) electrical schematic of 'XOR' gate.

Moreover, in order to respect the symmetry of the ring VCO delay cells, the input 'XOR' gates are identical and consequently present the same input impedance, which is equal to 63 KΩ at 500 MHz switching frequency. The delay cells loads should be smaller than the 'XOR' gates input impedance values not to modify the elementary time-constant. The 'XOR' gates generate command impulses from the delay cells inputs and outputs. This is achieved by using NMOS transistors of 1x1x0.35 μm^2 gate size. Nevertheless, the low gate size of these transistors cannot provide the necessary current to drive the switching transistors, which have a gate width of 6x25 μm for a length of 0.35 μm. Consequently, a buffer consisting of five stages is implemented to ensure the switching (Fig. 8-b).

4. Simulation results

The performances of this switched capacitor filter are simulated by using the Agilent ADS software [12], which uses the conversion matrices formalism [13]. This nonlinear analysis method has proved to be the most rigorous and effective in term of CPU time [14]. Its application for the behavioral analysis of this filter is an original approach. The schematic models of the electrical components used in the simulation have been provided by Alcatel, Bruxelles, which fabricated the prototype.

4.1 Characteristics of the ring VCO with 'XOR' gates

The gate sizes of NMOS and PMOS transistors of the ring VCO are optimized to be respectively equal to 4x6x0.35 μm^2 and 3x4x0.35 μm^2. Consequently, the ring VCO output frequency F_{osc} is adjustable between 160 MHz and 270 MHz (Fig. 9) by controlling the current source of the delay cells between 0.65 mA and 1.06 mA.

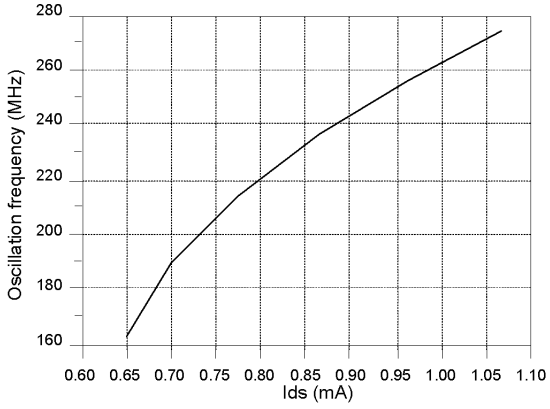

Fig. 9. Simulated oscillation frequency versus bias current of the ring VCO.

For the ring VCO design, a special attention was given to the temporal waveform signals in order to limit the time jitter [15]. In these conditions, the phase noise obtained is roughly -111 dBc/Hz at 1-MHz of the offset frequency (Fig. 10). According to targeted applications, it would be interesting to associate this VCO with a phase locked loop (PLL) to reduce the phase noise.

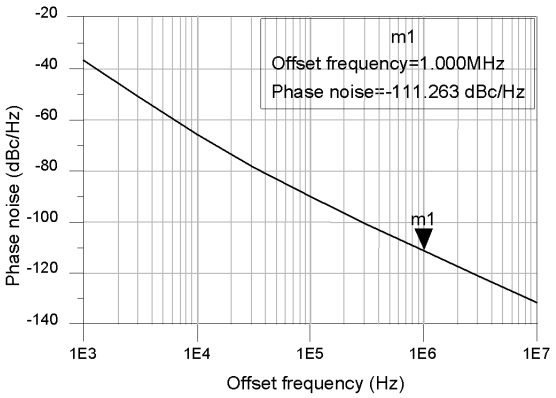

Fig. 10. Simulated phase noise spectrum of the ring VCO.

Fig. 11 presents the command signal waveforms x1(t), x2(t) and x3(t) respectively applied to the first, second and third switches for a switching frequency equal to 500 MHz. The impulse magnitude is higher than 3 Volts, allowing to get a low R_{on} value of the switch. The design of the switches is done so as to avoid the insertion losses generated by impulses overlap (i.e. the intersection level between two successive impulses lower than the threshold voltage of the switches).

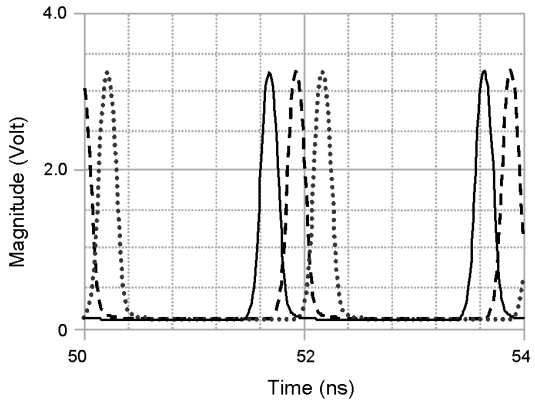

Fig. 11. Simulated command signals for three successive switches.

4.2 Characteristics of the switched capacitor filter

The dynamic range of the transfer characteristic and the noise figure of the filter are improved by replacing the input resistor of the filter by an inductor. For this new configuration the insertion losses are decreased and consequently the dynamic range is enhanced.

Table 1. Simulations Results.

Parameters	
Voltage supply (Volt)	3.3
Current consumption (mA)	26
Tuning frequency range (MHz)	320-500
-3 dB Frequency bandwidth @ F_0 (MHz)	0.9
Quality factor	355-550
Insertion loss @ F_0 (dB)	2.5
Dynamic range (dB)	25.5
1 dB input compression point @ F_0 (dBm)	-5
Noise figure @ F_0 (dB)	7

The main simulation results for this new design configuration at a switching frequency equal to 500 MHz are summarized in Table 1. For these simulations of the whole circuit, all parasitic effects particularly the parasitic elements of the inductor are taken into account. This filter presents an adjustable center frequency between 320 and 500 MHz with a constant bandwidth of 0.9 MHz. This assures a quality factor range between 355 and 550 according to the center frequency.

The current consumption of the whole circuit is relatively high but has not been optimized. Then, the total consumption is less than 26 mA, which are divided up as follows: 8 mA for the ring VCO, 18 mA for the Xor gates and the buffers. In the future, this current consumption must be decreased to assume all the interest of this circuit. This can be performed with the use of an higher f_T technology.

5. Experimental results

To validate the proposed design approach, a prototype was fabricated using a standard 0.35 μm silicon CMOS technology. The choice of this technology is justified by the application of this switched capacitor filter in the field of low-cost wireless communications. External networks allow input/output 50 Ω matching. When the command circuit is tuned off, all the switches are inactive (OFF), and the measured S_{21} parameter presents a resonance due to the external matching networks, this is the reference response in the Fig. 12. This one is compared with the measured transfer characteristic centered at a switching frequency closed to 300 MHz.

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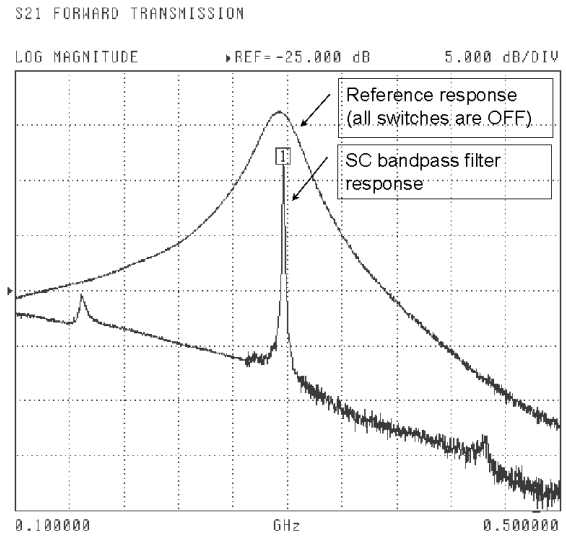

Fig. 12. Measured frequency response around a switching frequency closed to 300 MHz.

The measured results at both 300 MHz and 500 MHz switching frequencies are summarized in Table 2. The obtained results with this prototype show a tunable center frequency band of 260 MHz [240-500 MHz].

Table 2. Measured Results.

Parameters	@ 300 MHz	@ 500 MHz
Voltage supply (Volt)	3.3	3.3
Current consumption (mA)	26	27
-3 dB Frequency bandwidth @ F_0 (MHz)	0.970	3.4
Quality factor	310	140
Insertion loss @ F_0 (dB)	4	1
Dynamic range (dB)	18	12
1 dB input compression point @ F_0 (dBm)	-9	-9

Measurements at 300 MHz demonstrate interesting performances; the bandwidth is equal to 0.97 MHz (0.9 MHz simulation result), and the quality factor is roughly 310. However, the quality factor is reduced for the higher switching frequencies; thus, a quality factor of 140 is obtained for a switching frequency close to 500 MHz.

The difference observed between the simulation and measured results is due to the lack of accuracy the models present at high frequency harmonics of the switching signals.

For higher frequencies applications, a CMOS technology with a higher f_T (frequency transition) will be suitable to improve the performance of this circuit.

To improve the dynamic range, two approaches should be investigated. It will be performed either to increase the gain in the bandwidth or to decrease the "floor" at the outside. The gain could be improved by using a faster technology with an higher f_T, which would provide a wider band behaviour. Thus, it would be easier to generate rectangular switching commands to limit losses. It must be also mentioned that the use of a such technology could optimize the command circuit structure. Moreover the floor depends on the R_{on} switches resistance, which can be reduce by increasing the switching transistors size. If this increase is realized without changing the technology, then the C_{gs} value becomes too important and degrades the switching commands. However, if a higher f_T technology is used this increase allows to reduce R_{on} and the floor, while C_{gs} becomes less important.

6. Conclusion

A new circuit based on the association of a switched capacitor bandpass filter and its command circuit has been presented. This filter device is tunable over a broadband in the RF range by using a ring voltage controlled oscillator in 0.35 μm CMOS. Moreover, it is fully integrated and presents a high selectivity over the tunable frequency band. Commonly, such performances are not simultaneously present in one device.

The obtained simulation and measurement results demonstrate the validity of the proposed design approach. These results are comparable with those of SAW filters. This circuit could be used in the field of low-cost wireless communications as a subset of professional mobile phone.

Acknowledgement

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