New high-Q discrete-time LC bandpass filter design with center frequency broadband tuning

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Abstract Discrete-time switched-capacitor filters have been in wide-spread used for a few years, for the realization of stable, accurate and high quality filters. This paper describes the design of a new 8-path pseudo switched-capacitor LC bandpass filter and its command circuit made up by a ring voltage controlled oscillator (VCO) with 'XOR' gates. The proposed architecture presents the possibility of tuning over a frequency broadband allowing to sweep different channels with a high quality factor. This circuit is intended to replace the surface acoustic wave (SAW) filters in broadband wireless applications. Experimental results carried out on a prototype show quality factors up to 200, and a tunable center frequency range of 300 MHz [250–550 MHz].

Keywords CMOS analog circuits · High-Q · Bandpass tunable filters · Switched-capacitor · Broadband

1. Introduction

Recent years have seen the rapid proliferation of wireless applications circuits and systems. Wireless transceivers are an increasingly important commercial application [1, 2]. The current transceiver solutions often use low cost CMOS for digital and baseband circuitry, while reserving silicon bipolar or GaAs for critical radio frequency (RF) circuits. While this is good for optimizing the performance of individual subsystems, it is costly and makes full transceiver integration very difficult. Discrete passive components commonly used in today's transceivers (e.g. SAW filters and high-Q resonators) enable excellent filtering and ease generation of spectral pure signals, but they are often bulky and expensive. In addition, while the fixed frequency characteristics of these components are ideal for single-standard transceivers, they are inflexible and generally not as well suited for systems requiring multi-standard/multi-mode adaptation. In this context, promising perspectives can be profiled for the discrete-time switched-capacitor filters [3]. These filters present very interesting advantages in particular a very high selectivity associated with the possibility of adjustment of the center frequency by an internal or external clock signal. This characteristic is more significant for the integrated circuits, for which the tuning of the center frequency by a clock signal permits either to compensate the dispersions due to the technology used, or to filter various channels with the same filter. In the present paper emphasis has been given to study the performances of a high-Q 8-path pseudo switched-capacitor LC bandpass filter. It has been studied to prove the feasibility of this monolithic and tuned filter for frequency broadband wireless applications. To command the proposed filter a solution based on a ring VCO associated with 'XOR' gates has been proposed [4]. This solution provides the possibility of tuning within a frequency broadband, sweeping different channels with high Q-factors.

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2. Proposed filter description

The behavior of the pseudo switched-capacitor filters can be explained by the theoretical approach of N-path filters. Several papers [5–7] have already described this kind of filters.

In [8] a simplified structure of this filter has been proposed. This straightforward architecture (Fig. 1) presents under well defined conditions, properties identical to these of the N-path filter [8].

This classical architecture uses a first-order RC low-pass filter as basic cell. The switches are successively closed with a switching period To, during a time To/*N*. When, the command signals of the switches are considered to be Dirac's impulses $\delta(t)$ spaced by a To period, then, in the frequency domain, the output signal $S(f)$ can be written as function of the input signal $E(f)$:

$$S(f) = H_s(f) \cdot E_s(f) \tag{1}$$

where, $H_s(f) = \sum_{m=-\infty}^{+\infty} h(\text{m.To}).\exp(-2.\pi.j.f.m.\text{To})$ is the Fourier transform of the basic cell impulse response sampled at To period, and, $E_s(f) = \sum_{q=-\infty}^{+\infty} e(\frac{q.\text{To}}{N}).\exp(-2.\pi.j.f.\frac{q.\text{To}}{N})$ is the Fourier transform of the input signal e(t) sampled at To/*N* period.

Equation (1) shows that the total transfer function $H_s(f)$ of the classical pseudo switched-capacitor filter is the result of the transfer function of the basic cell (1 rt order low-pass filter) transposed around the center frequency ($Fo = 1/\text{To}$) and all their harmonic components.

The Q-factor of this filter (Fig. 1) can be written as $Q = \pi.\text{N.R.C.Fo}$. This relation shows that the filter selectivity depends directly on the number of cells (N) and the resistor value, which is taken usually equal to 1 KΩ; to have good trade-off between selectivity and dynamic range. However, the noise figure generated mainly by this input resistor seemed to be a penalizing element.

In this paper, we present a novel pseudo switched-capacitor LC filter, with an original architecture obtained by modifying the basic cell of a classical structure (Fig. 1). Thus, the first-order RC low-pass filter used for the classical basic cell is replaced by a second-order LC low-pass filter (Fig. 2). The low value resistor R_L simulates the inductor losses.

Let's consider only the basic cell, thus, when the switch $x_1(t)$ is ON, it presents a resistor value equal to R_{on}. In this case, the damping factor of this basic cell (second-order LC low-pass filter) can be written as:

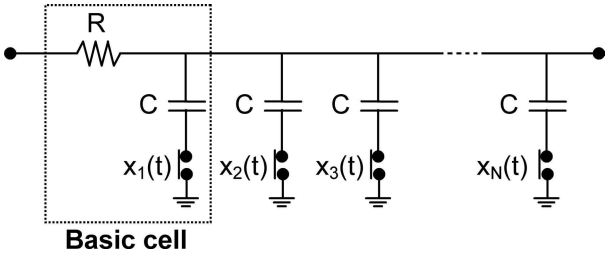

Fig. 1 Classical filter architecture with *N* pseudo switched-capacitors

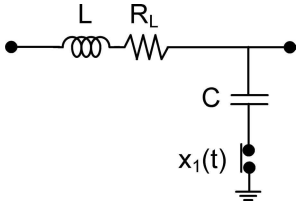

Fig. 2 Basic cell formed by a second-order LC low-pass filter

$$\xi = \frac{R_L + R_{on}}{2}\sqrt{\frac{C}{L}} \tag{2}$$

From (2), the quality factor of the new basic cell depends mainly on the inductor value L. Then, to obtain a high Q-factor it appears evident that the inductor value should be as higher as possible. Therefore, a trade-off must be made between the inductor value and the possibility of its integration.

The main advantages to change the basic cell are both to reduce the thermal noise figure due to the input resistor and to enhance the quality factor. Moreover, this new configuration will allow a good dynamic range due to the second order filter behavior.

Figure 3 shows the proposed filter architecture with basic cell formed by second-order LC low-pass filter. A trade-off has been found concerning the number of branches of pseudo switched capacitors. Indeed, if a significant number of branches would permit to improve the filter performances (high-Q), in the other hand it would lead quickly to an excessive complexity of the design [4]. The number of eight branches chosen for this study seems to be a good trade-off between the Q-factor and chip complexity.

Simulations realized with this novel architecture, show the same transfer characteristic behavior of the classical pseudo switched-capacitor filter (Fig. 1). Then, the proposed filter

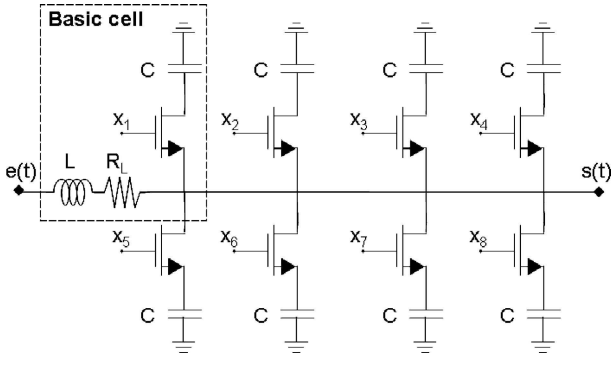

Fig. 3 Architecture of the proposed filter, with eight branches

(Fig. 3) can be used for clock recovering by filtering the harmonic components. It can also be employed as bandpass filter centered around F_0. This last application will be discussed in this paper.

3. Command circuit description

The main role of the command circuit is to generate the switching signals to commutate the capacitors. The classical command circuit was generally implemented using a shift register. This solution, which requires a clock frequency equal to the center frequency of the filter multiplied by the number of capacitors to commutate, is exclusively used at low frequencies. Therefore, a novel command circuit is proposed. It consists of a ring voltage controlled oscillator with 'XOR' gates (Fig. 4).

The ring VCO comprises eight identical differential delay cells. Each cell is based on one NMOS transistors differential amplifier (Fig. 5), to provide both the gain and the delay required for the oscillation phenomena.

The total delay cumulated with the eight cells is equal to 2.To, and leads to Fo/2 oscillation frequency. The delay generated by one cell depends of the time-constant Rp.Cp.

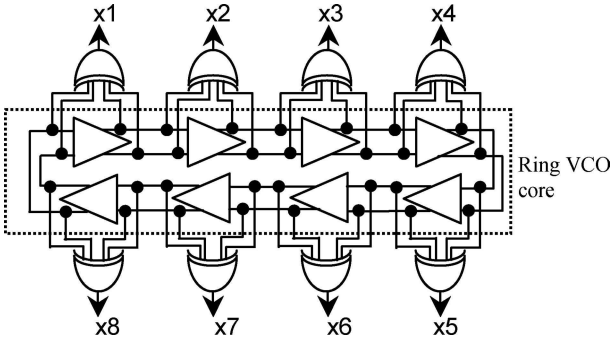

Fig. 4 Command circuit consisting of ring VCO with 'XOR' gates

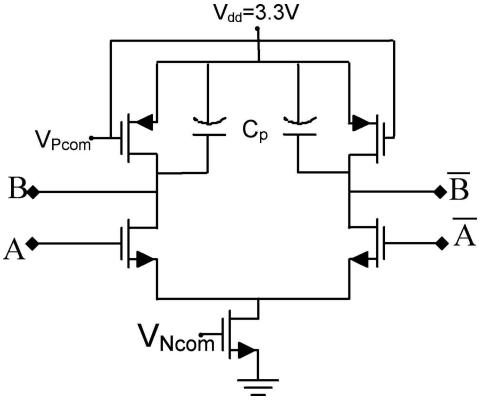

Fig. 5 Delay cell with NMOS differential amplifier.

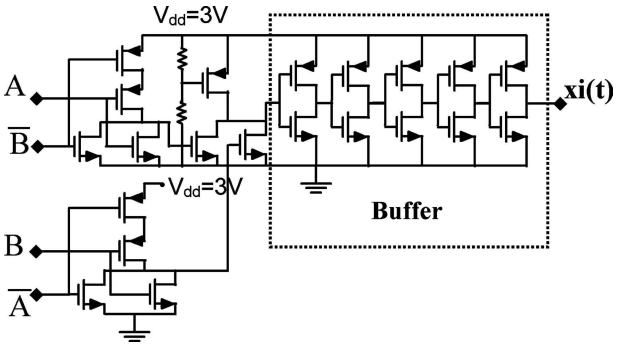

Fig. 6 architecture of the 'XOR' gate

The Cp capacitance is due to the 0.35 pF capacitor placed between drain and source of each PMOS transistor. The *R*p resistance corresponds to the differential resistive load, which is obtained by PMOS transistors working in triode region. The oscillation frequency is tuned by controlling both the common current source and the bias point of the PMOS transistors which modify the *R*p value between 800 Ω and 1.5 KΩ.

Figure 6 shows the architecture used for the 'XOR' gates. For generating the Fo/2 frequency the ring VCO requires eight differential amplifier delay cells providing the delayed output signals (0°–180°).

Moreover, in order to respect the symmetry of the ring VCO delay cells, the input 'XOR' gates are identical and consequently present the same input impedance, which is equal to 63 KΩ at 500 MHz switching frequency. The 'XOR' gates input impedance values must be higher than the delay cells loads for not modifying the elementary time-constant.

The 'XOR' gates generate command impulses from the delay cells inputs and outputs. This is achieved by using NMOS transistors of $1 \times 1 \times 0.35\ \mu m^2$ gate size. Nevertheless, the low gate size of these transistors cannot provide the necessary current to drive the switching transistors, which have a gate width of $6 \times 25\ \mu m$ for a length of $0.35\ \mu m$. Consequently, a buffer consisting of five stages was implemented to ensure the switching (Fig. 6).

4. Circuit design and simulation results

4.1. Command circuit design

The gate sizes of NMOS and PMOS transistors of the ring VCO are optimized to be respectively equal to $4 \times 6 \times 0.35\ \mu m^2$ and $3 \times 4 \times 0.35\ \mu m^2$. Consequently, the ring VCO output frequency (Fosc) is adjustable between 160 and 275 MHz (Fig. 7). This could be achieved by controlling the current of the delay cells. To ensure the oscillation phenomena, the current limits are set to 0.65 and 1.06 mA by each delay cell.

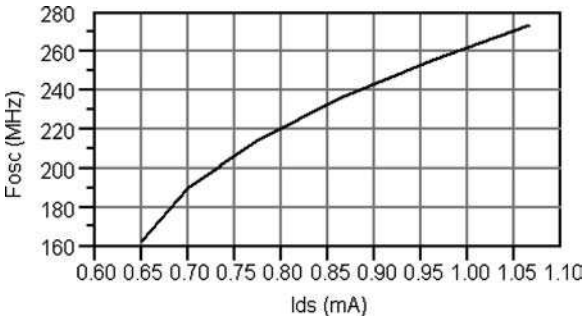

Fig. 7 Simulated oscillation frequency versus bias current of the ring VCO

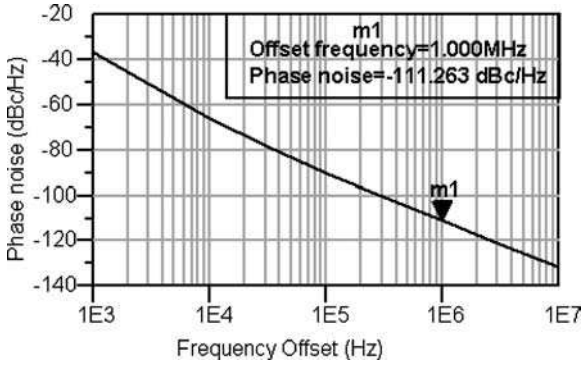

Fig. 8 Simulated phase noise spectrum of the ring VCO

Figure 8 shows the simulated phase noise spectrum of the ring VCO. During the ring VCO design, a special attention was given to its temporal waveform signals [9] in order to limit the jitter and hence the spectral power of phase noise at roughly –111.26 dBc/Hz at 1-MHz offset frequency from the carrier.

With this phase noise value, it is possible to calculate the jitter of the ring VCO. It appears evident that this jitter must be lower than the command impulse duration which is equal to 250 ps, with 500 MHz center frequency and eight branches.

Since, the phase noise at 1-MHz offset from the carrier frequency is in the $1/f^2$ region. The jitter is generated by the conversion of a white Gaussian cyclostationnary process. Hence, the cycle-to-cycle jitter σ_{CTC} is defined by the following expression [10]

$$\sigma_{CTC} = \sqrt{\frac{1}{F} \cdot \frac{\Delta F}{F}} . 10^{-L\{\Delta F\}/20} \tag{3}$$

where, F, ΔF and $L\{\Delta F\}$ are respectively the oscillation frequency, offset frequency from the carrier and noise power spectral density.

Then, the calculated cycle-to-cycle jitter is equal to 0.2 ps. Such a value is negligible as compared to the impulse duration (250 ps).

Figure 9 presents the command signal waveforms $x1(t)$, $x2(t)$ and $x3(t)$ respectively applied to the first, second and third switches for a switching frequency equal to 500 MHz. The impulse magnitude is higher than 3 Volts, allowing to get a low R_{on} value of the switch. During this design, it was necessary to avoid losses generated by the overlap of command impulses. Indeed, this overlap generates a no ideal transfer which is the origin of important insertion losses. Therefore, it is necessary that the level of the intersection between two successive impulses remains lower than the voltage value of commutation.

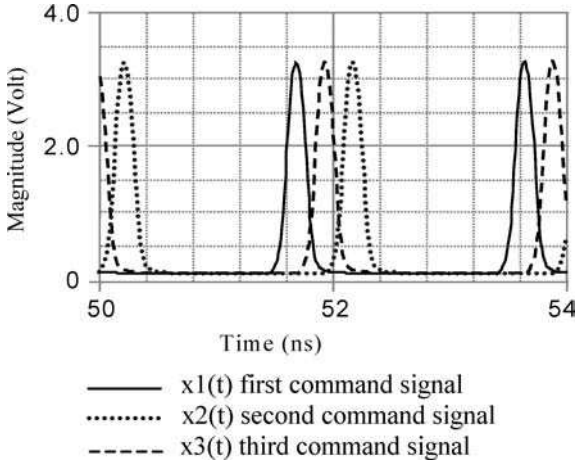

Fig. 9 Simulated command signals for three successive switches

4.2. Filter design

The filter switches were produced with N channel MOSFETs transistors, which are switching sequentially between the ON and OFF modes.

The first critical design limitation is the choice of the switching transistors size. Indeed, a compromise must be found considering the following factors:

- A significant transistors gate size would ensure a low R_{on} resistor but the associated parasitic capacitor Cds would be significant. Under these conditions, the filter bandwidth would be limited by the cumulated effect of all these parasitic capacities involving attenuation on the whole transfer characteristic, and thus decreasing the filter dynamic range.
- A too small transistors gate size would also involve a reduction of the filter dynamic by the raising of transfer characteristic (floor). Indeed, if R_{on} value is significant than the compensation of the attenuation is done at low frequencies. Consequently, the frequency which the phenomenon of "the floor" appears is reduced, which decreasing the dynamic range.

Transistors used in this design are channel N MOSFETs composed of six fingers with an elementary gate width of

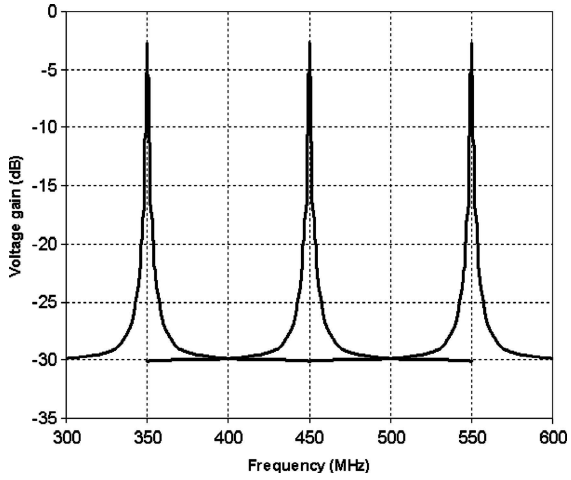

Fig. 10 Simulated voltage gain versus frequency for different switching frequencies

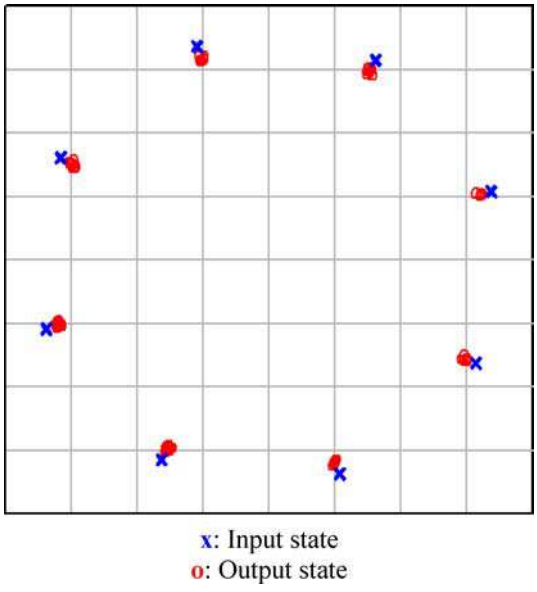

Fig. 11 Constellation diagram at the input and output of tuned LC pseudo switched capacitor filter

25 μm and a length of 0.35 μm. These transistors present a resistance R_{on} of 30 Ω and a drain-source capacitance C_{ds} of 0.06 pF, to give an optimal dynamic range.

Figure 10 shows the simulated voltage gain versus frequency for the proposed filter ($L = 20$ nH, $C = 50$ pF). For these global circuit simulations, all the parasitic effects are taken into account. An optimal dynamic range of 27 dB is obtained which is comprised between a –3 dB voltage gain in the band and a –30 dB in the rejection band. This new filter design presents an adjustable simulated center frequency ranging between 320 and 550 MHz with a 900 kHz bandwidth and a simulated quality factor value higher than 350 within the tunable frequency band.

Table 1 Simulated normalized EVM values

EVM (RMS) correlated noise	EVM (RMS) uncorrelated noise
1.314%	9.526%

A special attention was given to study the effect of time jitter, and to predict possible degradations which can be generated by the filter. Actually, the time jitter introduces a random variation of the instantaneous frequency and consequently a degradation of the command signals shapes. According to the correlation of these signals the effect on the constellation and consequently the EVM (Error Vector Magnitude) is different. The behavior of the proposed filter has been simulated when its input signal is changed to a digitally modulating signal of type $\pi/4$–DQPSK (Differential Quadriphase Shift Keying) modulation.

Figure 11 shows the obtained output constellation compared with the ideal one in case of correlated command sources generated by the ring VCO. These constellations are obtained at a switching frequency equal to 500 MHz, using a $\pi/4$–DQPSK digital modulation with a symbol rate equal to 24.3 KHz, by applying the same simulated phase noise value on command signals ($-$ 111 dBc/Hz at 1-MHz of the carrier frequency).

Expressed in percentage (%), the EVM (Error Vector Magnitude) is a parameter which makes it possible to quantify the effect of the additive noise on the deformation of the transmitted signal constellation. Table 1 shows that the RMS value of the EVM does not exceed 1.5% if the noise is correlated.

While this value is close to 10% in the case when the command signals are uncorrelated by using independent switching command sources. From this result, it appears important to have only one source that provides all command signals, which confirms our choice of this ring VCO to command the filter.

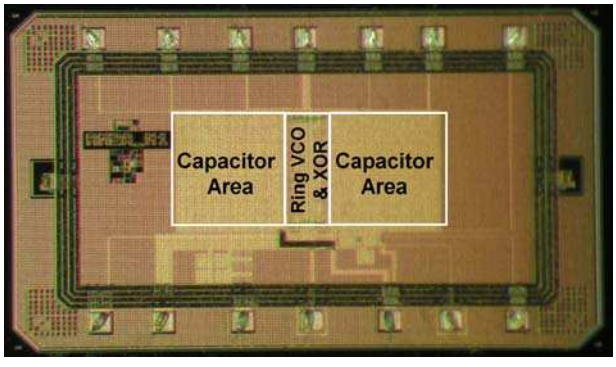

Fig. 12 Micro-photograph of the 8-path pseudo switched-capacitor LC bandpass filter and its command circuit

Table 2. Measured results

Parameters	@ 250 MHz	@ 550 MHz
Voltage supply (Volt)	3.3	3.3
Current consummation (mA)	14	15
− 3 dB frequency bandwidth (MHz)	0.970	1.9
Quality factor	275	289
Insertion loss (dB)	4	1
Dynamic range (dB)	20	18
Input 1 dB compression point (dBm)	− 9	− 9
Noise Figure (dB)	6.5	7

5. Experimental results

To validate the proposed design approach, a circuit demonstrator composed by an 8-path pseudo switched-capacitor LC bandpass filter with its command circuit was fabricated using a standard 0.35 μm silicon CMOS technology. The values of the inductor (L) and the capacitor (C) are respectively equal to 20 nH and 50 pF. The corresponding chip Micro-photograph is shown in Fig. 12, and the chip area is 1.1×1.75 mm^2. An external inductor is used since this frequency implies the choice of a large inductor that cannot be integrated.

Figure 13 shows the measured voltage gains versus frequency closed to switching frequency Fo equal to 300 MHz (Fig. 13a) and 444 MHz (Fig. 13b), for 8-path pseudo switched-capacitor LC bandpass filter. The achieved results with this prototype show a tunable center frequency band of 300 MHz (250–550 MHz).

The −3 dB bandwidth measured at 444 MHz is about 1.7 MHz, thus a quality factor value approximately equal to 260. The measured results at two different center frequencies are synthesized in the Table 2. The achieved measurements are very interesting, in particular the center frequency, which can be controlled over a frequency broadband with an internal clock signal, and the high selectivity that can be achieved. These results can be improved by using a technology with high f_T for higher frequencies applications which make available the possibility of using an integrated inductor.

6. Conclusion

A new design of an 8-path pseudo switched-capacitor LC bandpass filter and its command circuit has been proposed. The design and the implementation of the whole circuit in standard 0.35 μm CMOS technology have been described. This novel architecture presents a high performance compared to the classical one particularly in the noise factor and dynamic range. The experimental results demonstrate the validity of the proposed design approach and confirm the interest of these original circuits. This circuit could substitute SAW filters in broadband wireless applications.

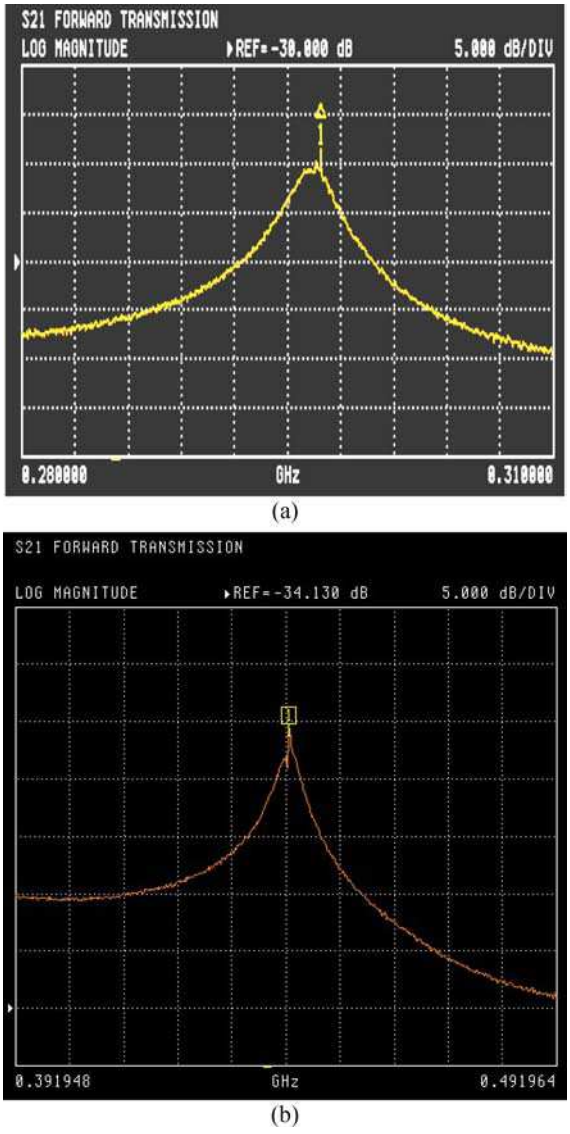

Fig. 13 Measured voltage gains versus frequency for switching frequency closed to (a) 300 MHz (b) 444 MHz

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Jean-Marie Paillot received a Ph.D in Electronics form the University of Limoges, in 1990. His thesis on the design of non-linear analog circuits and the study of the noise spectral of integrated oscillators was prepared at the Institute of Research for Optical Communications and Microwaves, Limoges. After graduation, he joined the Electronics Laboratory of PHILIPS Microwave, at Limeil, as R&D engineer in charge of the design of analogical and numerical microwave monolithic integrated circuits. Since October 1992, J.M. Paillot is at the University Institute of Technology, Angoulême, where he currently is Professor of Electronics Engineering. In charge of several contracts with industry, and author of papers published in scientific journals, J.M. Paillot is at present interested in phase noise reduction techniques for microwave oscillators, as well as in the research and development of switched capacitor filters in RF domain.

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