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ALGORITHMS HARDWARE IMPLEMENTATION FOR ULTRASONIC DATA PROCESSING IN SHM SYSTEM

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ABSTRACT

Nowadays, devices that monitor the health of structures consume a lot of power and need a lot of time to acquire, process, and send the information about the structure to the main processing unit. To decrease this time, fast electronic devices are starting to be used to accelerate this processing. In this paper some hardware algorithms implemented in an electronic logic programming device are described. The goal of this implementation is accelerate the process and diminish the information that has to be send. By reaching this goal, the time the processor needs for treating all the information is reduced and so the power consumption is reduced too.

KEYWORDS: *hardware algorithms, FPGA, beamforming, signal characterization.*

INTRODUCTION

Are on-board SHM Systems a real possibility? This question is the topic of discussion among the airlines and scientific research community. Many challenges must be overcome to achieve on-board monitoring of the overall structure of the aircraft: select sensors and more precise techniques, finding efficient algorithms, reducing the weight of equipment, design a specific communication [1], reduce power consumption... In general, the large amount of structures that comprise an aircraft constrains the performance and increases the complexity of the SHM systems [2].

The main problem is the large amount of data that occurs at the completion of a SHM test. For example, a SHM system based in piezoelectric transducers [3] with a beamforming transmission test consists of 200 to 400 simple tests. Each of those single tests consists of sending some ultrasonic waves and receiving the return of the waves. If the device sample to 10 Msps or more, the amount of generated data after doing the complete test stays around 500 Mbyte of data. If the aircraft, for example, includes 1,000 SHM systems, the collected information would be too much to be saved in a unique Central Computer.

Using a distributed system is another possibility. Each SHM system must perform the processing of the data and send to the Central Computer only the result of the test. But it is necessary to have a high throughput in each SHM systems. The embedded processor may take several minutes to process such amount of information. During this time the processor should be using electric power and cannot enter low power state.

This is where the solution of a hardware algorithm comes very useful, and the Field Programmable Gate Array (FPGA) inside a SHM System gives the possibility to implement a high performance solution. A FPGA is an electronic Programmable Logic Devices (PLD) with concurrent high speed operation. With this proposal the FPGA could process the data in around 1 or 2 seconds, so the device will be in low power mode the rest of the time and it will not consume power to the aircraft. The main aim is to develop a complete hardware algorithm that will detect the

damages in the different structures and reduce the information that the device has to keep or to send to the Central Computer of the aircraft.

An architecture for data processing SHM systems is presented in figure 1. This SHM system is based in piezoelectric transducers. The signal generator produces sinusoidal waves sent to the piezoelectric transducers, which use those signals to send ultrasonic signals through the structure. Those waves rebound and are sampled by the Data Acquisition Unit and sent to the Processor Unit. What is proposed in this paper is including a Hardware Processor Unit before the Processor Unit.

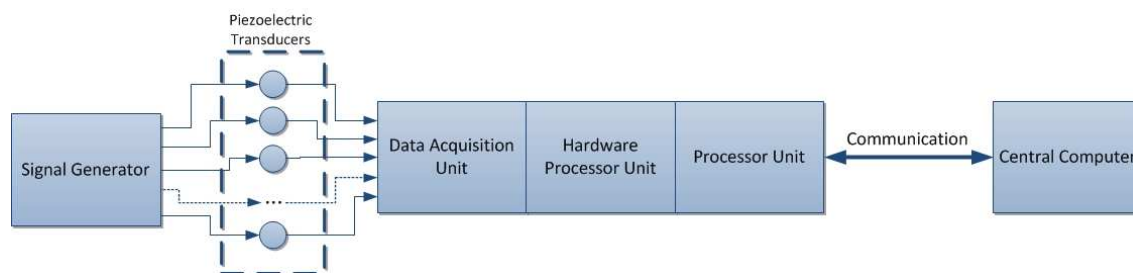


Figure 1. An architecture for high speed SHM inspection.

Usually an algorithm for detection of damage is processed by a complex processor based in program flow. In this proposed the algorithm is processed with two processors: a data flow processor and a simplex processor based in program flow. The first part of the algorithm, depending on the data position of the data, could be processed with hardware devices to reduce the operation time. The second part of the algorithm will be done by a high speed processor.

In this paper, two different types of algorithms and techniques are going to be presented: Beamforming Techniques and Signal Characterization.

1 BEAMFORMING TECHNIQUES

One of the most used methods for SHM is using beamforming techniques. Beamforming is a technique used in arrays of sensors for transmission and reception [4]. In this case it will be based on an array of piezoelectric transducers. There are several ways of placing the piezoelectric transducers [5], but the most simple but efficient way of placing them is in a linear array. There are two beamforming methods: transmission and reception modes.

1.1 Transmission beamforming

The most basic technique that can be implemented for studying a structure is a transmission beamforming. This technique is presented in figure 2.

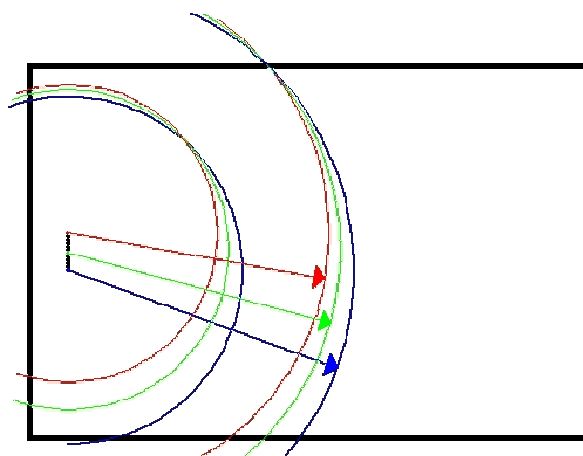


Figure 2. A structure and the waves send delayed for a transmission beamforming test.

Basically this means that the ultrasound waves sent by the piezoelectric transducers will be delayed so that all that signals reach a specific point in that structure at the same time. The waves that appear in figure 2 are sent by three different piezoelectric transducers, with some delay. That is why the blue circle representing the wave has a larger radius than the other two, but they reach at the same time to the point of study in the border of the structure. As all the waves reach that point together, the influence of each of those waves will be added to the rest of them, reaching a maximum in that point. Then, the added wave rebounds and returns to the piezoelectric transducers again so it can be sampled and stored in memory.

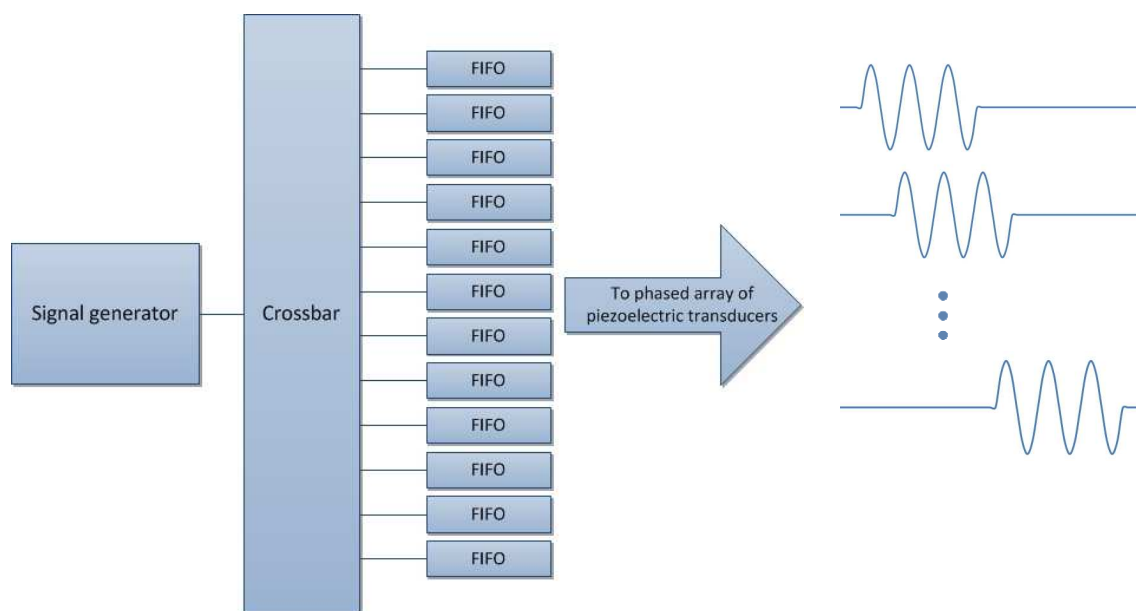


Figure 3. Basic transmission beamforming technique.

The signal generator generates a wave and the crossbar assign the order in which they have to be delayed. After that, those signals go through a system of FIFOs which allow to delay each of the signals a different time, so all the signals converge in a single point, which is the point of study in that moment.

The main problem of this technique is that the signal from the nearest piezoelectric transducer to the point to study has to be delayed n samples, but the signal from the farthest channel has to be delayed the number of transducers multiplied by n samples. Because of that, this algorithm spends a lot of memory of the FPGA it is implemented in.

To solve that problem, another configuration is presented for the same technique.

As the signal passed to each of the piezoelectric transducers is the same but delayed, the configuration described in figure 4 can be implemented. The signal the crossbar passes in the first position will be delayed n times, because it only goes through one of the FIFOs, but the signal the crossbar passes in last place goes through twelve (the number of transducers in this example is twelve) FIFOs, so the same algorithm from figure 3 can be implemented, but using approximately six times less memory.

Looking at figure 2, if the point of study is in the superior half of the structure, like the one in the example shown in the figure is, the closest piezoelectric transducer will be the first one, counting from above. However, if the point of study is in the inferior half of the structure, the closest piezoelectric transducer will be the last one. That crossbar changes the order of the channels to solve this issue.

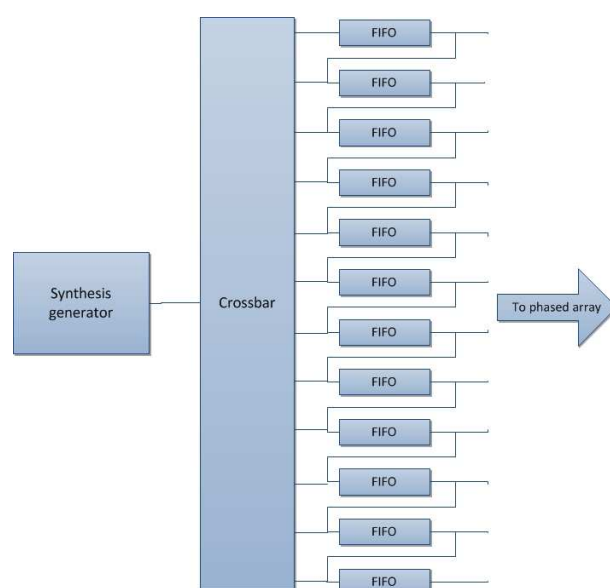


Figure 4. Memory optimized transmission beamforming algorithm.

The Crossbar implemented in the beamforming techniques allows to choose which signals go before and which go after. In figure 5 some of the possible implementations are shown.

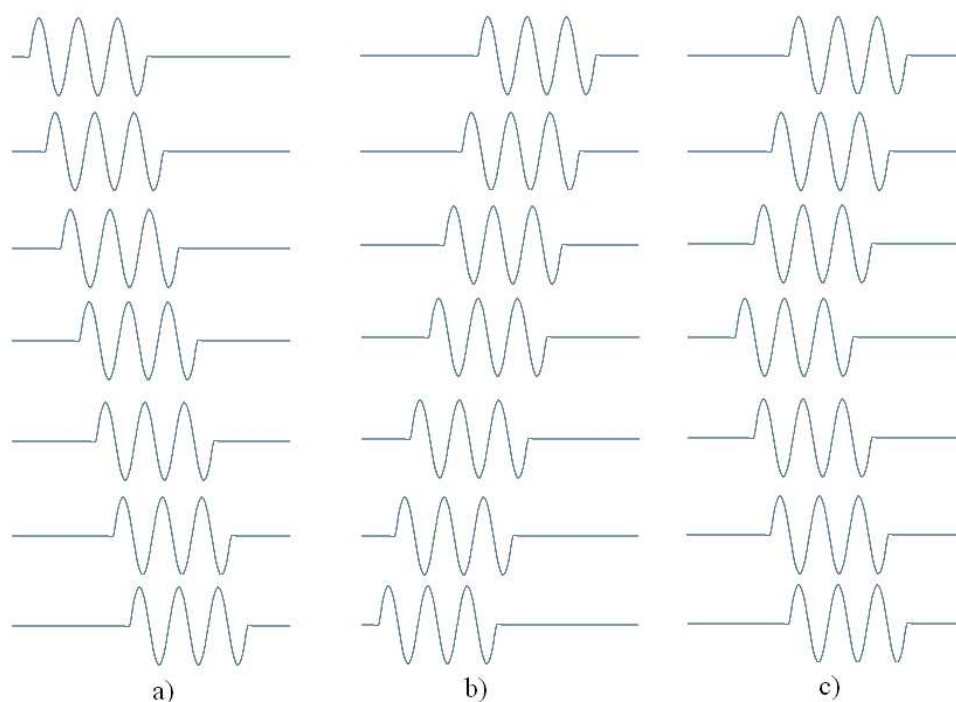


Figure 5. a) Upper half beamforming b) Lower half beamforming c) Focusing technique.

The first configuration in figure 5 shows how the signals will be sent to the different piezoelectric transducers when the point of study is in the superior half of the structure. The second configuration shows the same but if the point of study is in the inferior half of the structure. The third configuration belongs to a focusing technique.

1.2 Reception beamforming

Other technique that can be implemented is the reception beamforming. It is the same technique presented before, but focusing on the reception of the ultrasonic signals instead of the transmission. The twelve signals are received from the phased array of piezoelectric transducers and the signals are delayed when they arrive so each of the channels going to the processing unit has the rebounds of the ultrasonic waves in the same sample. Before going to the processor the signals are added into one signal, so the maximums and minimums the rebounds produce are higher and lower respectively in the unified signal (figure 6).

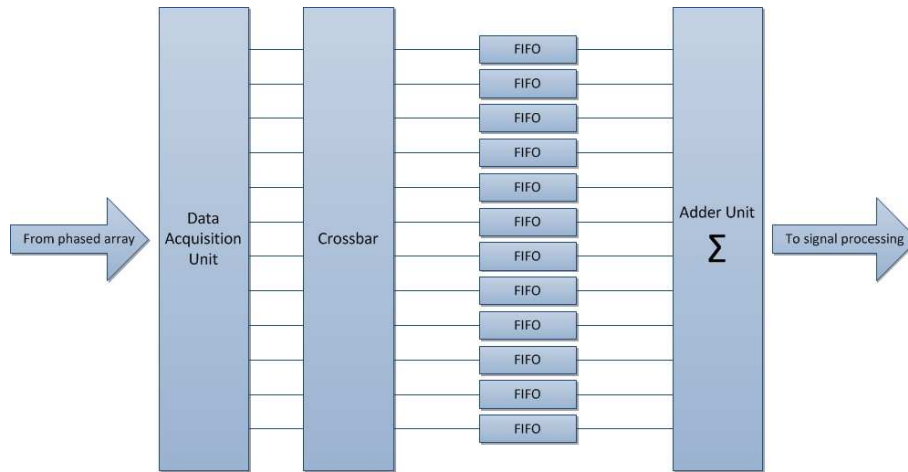


Figure 6. Basic reception beamforming technique.

As this configuration is similar to the basic transmission algorithm, it has the same problem. The bottom channel will need twelve times the retard of the first one, so a lot of memory will be needed. Because of this problem, another configuration was implemented (figure 7). The partial adder allows reduced the size of memories in each stage.

This last optimized algorithm used half of the memory from the prior algorithm, so it will fit perfectly in the FPGA used in the SHM device. All the process is completed during the acquisition time. The main processor has the processed signals with the higher rebounds before beginning the second part of the algorithm.

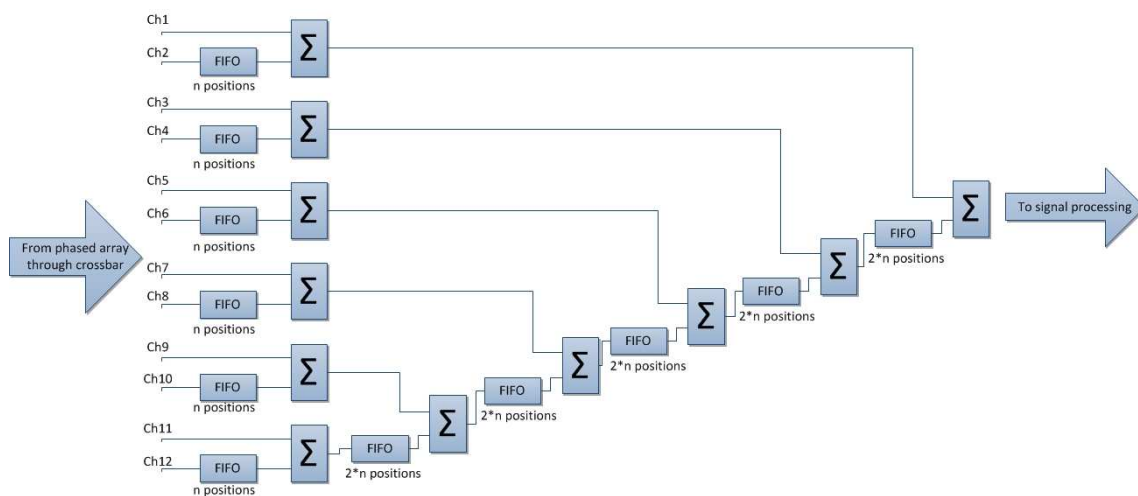


Figure 7. Memory optimized reception beamforming algorithm.

2 SIGNAL CHARACTERIZATION

The other type of algorithms presented in this paper focus on the characterization of the ultrasonic waves received in the piezoelectric transducers. As the device has a high sample rate, when a single experiment takes place, around 25000 samples are taken, so the processing unit has to treat all that information and takes a lot of time to do it. One of the solutions to that problem is find relevant data in all that information that can be treated the same way the raw information was processed.

As the important information the device has to determine is the rebounds of the ultrasonic waves in the structure, the algorithm should focus on the maximums and minimums of the signal, ignoring the noise produced by the other piezoelectric transducers. The algorithm proposed ignores the data below a configurable limit, so the noise below that limit will not count as a maximum or minimum. It also counts only one maximum and minimum between two sign changes, and resets the values after storing the previous ones when a sign change is detected.

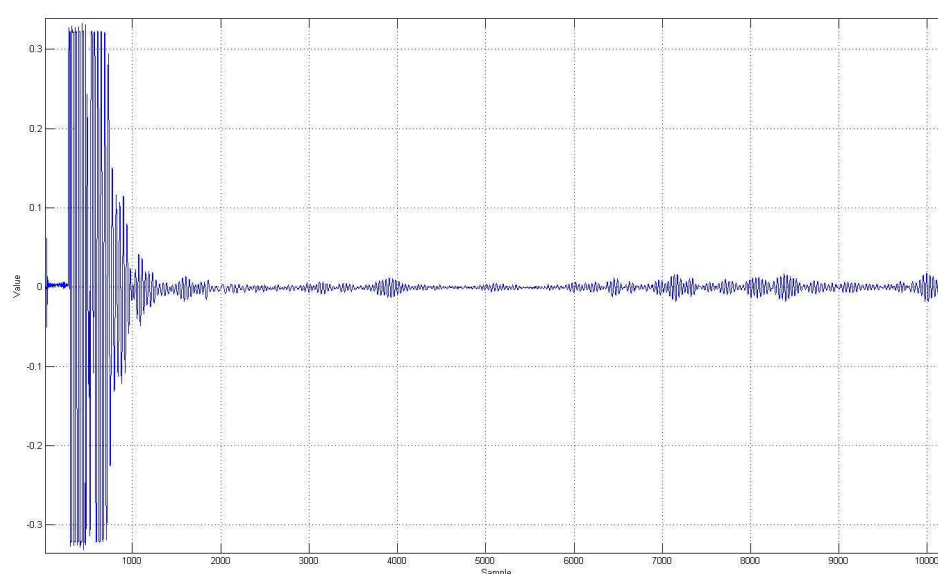


Figure 8. Raw information from one of the channels.

In figure 8 it can be seen how the device captures data from one of the channels. The complete chart will show around 25000 samples, so this chart is reduced by a half more or less because the complete chart is too large. The first 1000 samples show the sinusoidal waves the piezoelectric transducers need to send the ultrasonic waves through the structure. After that, the rest of the samples represent noise and the rebounds of the waves in the structure.

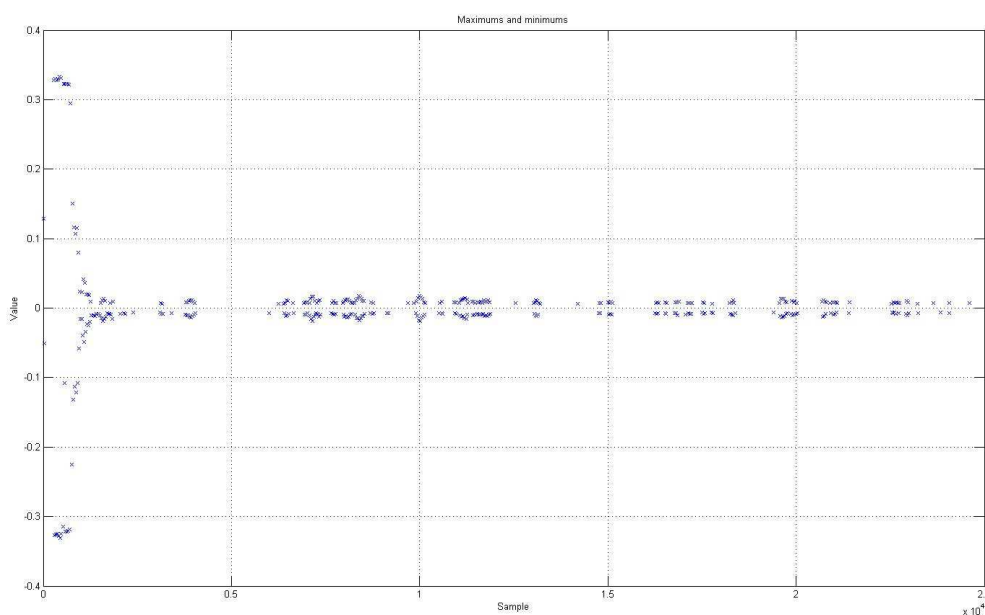


Figure 9. Data chart after the algorithm.

In figure 9 only the maximums and minimums appear, so the amount of information is lower. It has been estimated that the 25000 previous samples are reduced to the range of 500 maximums and minimums after passing through the hardware accelerator, so it is easier for the processor to store or processes that information. With this algorithm, the processor only receives a characterization of the signal consisting in the maximums and the minimums of the complete signal and its positioning through time. With this data, the frequency of the maximums and minimums can be calculated.

CONCLUSION

The main characteristic for an embedded device in a structure for SHM is to be low power consuming and efficient in its functions. It is because the time to processing the information has to be the lowest possible so it can stay in low power mode the longest time possible.

With the huge amount of data having to be processed, the time the device is consuming power is too high. With the algorithms presented in this paper the device will reduce the time it is in full power mode from minutes to seconds each time it has to perform a test, so it can stay in low power mode more time than it was before the hardware accelerators are implemented.

With these new improvements, the device will be much more efficient and could be installed in different structures without worrying how much it will cost to have it working all the time. These techniques give a little approach to embedded SHM systems.

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