Fine-Grain Reconfigurable Logic Cells Based on Double-Gate MOSFETs

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This work presents a new style of gate-level reconfigurable cells based on the double-gate (DG) MOSFET device. The proposed dynamic- and static-logic cells demonstrate significant gate area reductions compared to conventional CMOS lookup table (LUT) techniques (between 80-95%) while configuration memory requirements are also reduced (up to 60%). Simulation results show that it can be used either in low power reconfigurable applications (up to 90% power reduction is possible) or for speeds comparable to those of CMOS-LUTs.

Introduction

The necessary structuring of the projected tens of billions of elementary, unreliable, nanometric devices to achieve the computing capacities necessary for future software applications will lead to the emergence of reconfigurable platforms as the principal computing fabric before the end of the next decade. The reconfigurable approach allows volume manufacturing and reduces the impact of the evolution of mask costs, projected to move above the $10M mark in 2010 [1]; can efficiently cover a broad range of applications while exceeding performance levels of programmable systems; and couples naturally to fault-tolerant design techniques for robust architectures.

Gate-level, or fine-grain, reconfigurability enables benefits in terms of silicon real estate, since it makes it possible to reduce the number of logic cells necessary to implement a given switching function (in comparison to the implementation of these functions with conventional logic). It also makes it possible to simplify the interconnect network, reducing area and the parasitic capacitances due to routing. It can thus be expected to reduce dynamic power dissipation and improve speed. These two performance metrics are often the weak points of the various types of reconfigurable circuits (FPGA, coarse-grain reconfigurable systems) compared to "full-custom" solutions.

While CMOS device scaling has led to increasingly better performances, higher packing density and lower cost per device, short channel effects have become difficult to control [1]. To pursue performance improvement in conventional planar bulk CMOS devices, channel doping will have to be increased with scaling to almost impossibly high values, which will cause a reduction in mobility and high leakage

current (and static power dissipation) due to band-to-band tunneling between the drain and the bulk. Also, the total number of dopants in the channel for very small MOSFETs is increasingly low, resulting in extremely high fluctuataions in the number of dopants, and hence unacceptably large statistical variation of the threshold voltage. These difficulties, especially power dissipation and variability, have introduced the need for new device architectures and the emergence of structures with improved and more flexible electrostatic control of the channel.

Ultra-thin body, fully depleted (UTB FD) SOI MOSFETs represent one solution where channel doping is relatively low; in these devices, the threshold voltage can be set by adjusting the work function of the gate electrode, rather than by doping the channel as in planar bulk MOSFETs. Metal gate electrodes with work functions tunable within a few hundred meV above and below midgap should be used to set the threshold voltage to the desired values. Single gate SOI MOSFETs are projected for 2010 for high-performance logic. Multiple-gate, ultra-thin body, fully depleted MOSFETs, in both planar (DG MOSFET) and vertical dispositions (FinFET), are both more complex and more scalable, and are projected to be implemented in 2011 for high-performance logic.

The Double-Gate (DG) MOSFET on FD SOI technology is known as a promising advanced device which, thanks to the double-gate structure, is expected to overcome drawbacks of the conventional MOSFET in nanometric technologies. Compared to its counterpart single gate FD SOI MOSFET, the DG SOI MOSFET reduces the short channel effects and improves the sub-threshold slope and drive current [2][3][4] while benefiting from the advantages of FD SOI technology. These include reduced latch-up, reduced parasitic source and drain capacitances, smaller sensitivity to temperature variation and reduced leakage current [5]. The double-gate structure allows independent switching of the gates or dynamic adjusting of the threshold voltage. In more conventional (single gate) device structures, a dynamic Vth variation can be achieved by varying the body or back gate voltage for bulk and fully depleted SOI devices respectively. However, since all devices share the same well or substrate (for bulk devices) or the same back-gate (for single gate FD SOI devices), dynamic Vth variation for individual transistors is either highly impractical or impossible to achieve.

Partially depleted SOI devices are better suited to dynamic adjustment of the threshold voltage since the body is isolated and can thus be contacted to a separate bias potential per device. However, double gate SOI MOSFETs offer the same flexibility as PD SOI single gate MOSFETs with regard to this dynamic Vth adjustment. Moreover, it has been demonstrated that an independent control of front and back gates can be exploited to reduce both dynamic power and sensing delay in a sense amplifier design [6]. It can also be used to merge parallel transistors [7] and thus reduce dynamic power through the reduction of parasitic capacitance, as well as static power. Furthermore, designers can choose between different types (symmetric or asymmetric [3]) of DG MOSFET devices, in order to make the threshold voltage tailored to the requirements of circuit operation. This makes it well-suited for some leakage power management circuit techniques commonly used in digital circuit design. Furthermore, it allows consideration of new design approaches. However, all these advantages come at the expense of a higher switching gate capacitance (in the

case of the connected gates scheme) and a die area penalty compared to the single gate device.

Such devices enable designers to achieve improved density, power and speed metrics [3][4][7][8] in logic cells. Further, with four accessible terminals, these devices also offer the opportunity to design novel building blocks exploiting the additional terminal for reconfigurability purposes [9]. In this work, we cover the principles of the design of *m*-input DG MOSFET reconfigurable cells in both dynamic- and static-logic forms. These principles are applied to the design of 2-input cells, and the simulated results are then compared to those of conventional CMOS LUT techniques.

Generic *m*-input reconfigurable cell

The main tenet of our approach lies in the construction of cells containing n- and p-networks for which the data-switching properties can be modified with control voltages applied to the back gates of DGMOS transistors. This dynamically modifies the threshold voltage of individual devices. The behavior of an n-type DGMOS device according to the applied back gate voltage can be roughly described as follows:

- when a sufficiently positive voltage V^+ is applied, the device is always on (regardless of front gate voltage). In other terms, the threshold voltage is lowered to below the lowest voltage applied to the front gate (e.g. logic "0").
- when 0V is applied, normal operation is achieved, i.e. device switching depends on the front gate voltage.
- when a sufficiently negative voltage V^- is applied, the device is always off (regardless of front gate voltage). In other terms, the threshold voltage is raised to above the highest voltage applied to the front gate (e.g. logic "1").

This behavior is shown in simulations for both n-type and p-type devices in Figure 1. These simulations are for individual devices with W/L=0.25µm/0.13µm with 1.2nm front- and back-gate oxide thicknesses, and use a double-gate FD-SOI/CMOS technology model implemented in Verilog-A. This explicit analytical charge-based compact model of independent double gate MOSFET devices is based on Poisson and field continuity equations and demonstrates <2% drain current value error with respect to Atlas simulations over all regions of operation and for both long and short channel devices. It has also been extensively validated against experimental device characteristics. Further details of the model are outside the scope of this work and can be found in [10].

For certain branches it is necessary to use asymmetric devices to achieve a dominant influence of the control voltage on the transistor behavior. Previous work in this field [9] has been inconclusive since only symmetric devices were used, resulting in a circuit structure with limited functionality and unsatisfactory performance. Asymmetric devices provide additional degrees of freedom and can be achieved with different oxide thicknesses or different gate workfunctions (i.e. with different gate metals). Our work is based on the former approach, with front-gate oxide thickness T_{oxf}=2.5nm or 5nm (depending on the degree of asymmetric control required –

increasing the oxide thickness also increases leakage current) and back-gate oxide thickness T_{oxb}=1.2nm. Simulated I_{ds}-V_{gs} characteristics show (for an N-type device of the previously cited dimensions with T_{oxf}=2.5nm, V_{bgn}=0V) a slight (15%) increase in I_{off}, and a more significant (45%) decrease in I_{on}. Again, the model used has been extensively corroborated against technology simulations.

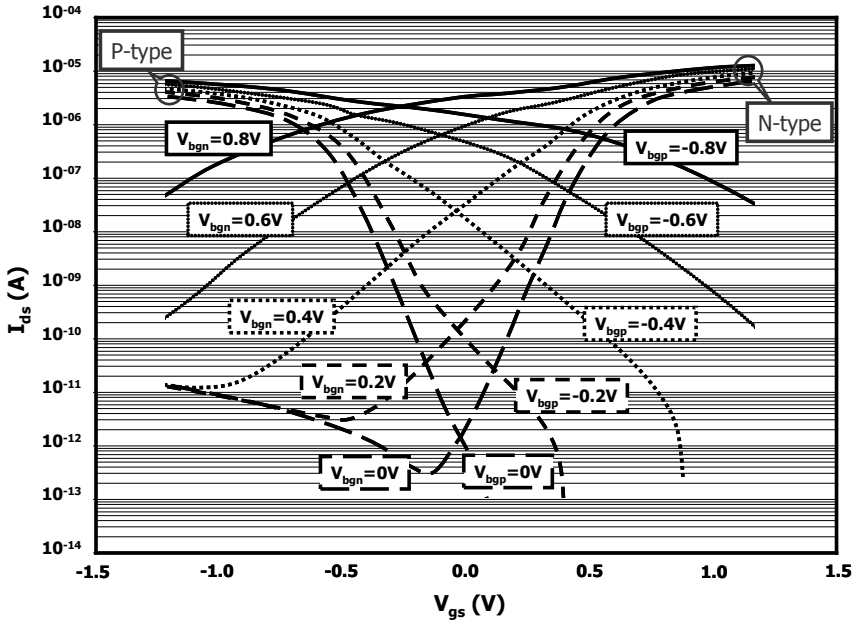


Fig. 1. Log I_{ds}-V_{gs} plot of n-type and p-type DGMOS model with independent gate control

Dynamic-logic reconfigurable cell *DG-DLRC*

The general principle for building an *m*-bit dynamic-logic reconfigurable cell (DG-DLRC) is shown in Figure 2. This novel structure uses n-type dynamic logic, where a switching network composed of n-type devices is sandwiched between clocked precharge and evaluation switches (M_{pc} and M_{ev} respectively), and allows conditional discharge of the output node F during the evaluation phase. The n-type device network that realizes the logic functions is composed of:

- one branch containing a stack of *m* symmetric DG MOSFETs
- *(m-1)* branches each containing a single asymmetric DG MOSFET (with $T_{oxf} > T_{oxb}$).

The front gates of these devices are controlled by the *m* logic inputs. *2(m-1)* control signals are applied to the back gates to configure the logic function dynamically.

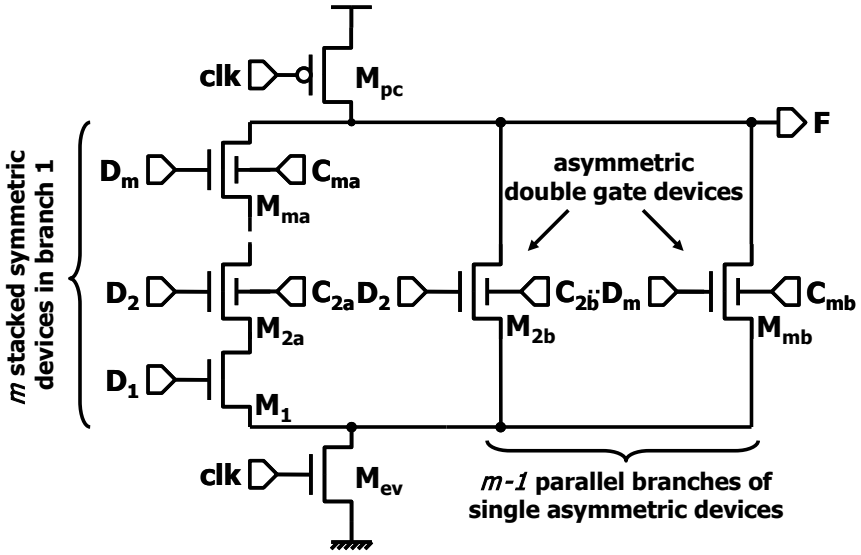


Fig. 2. Generic DGMOS dynamic-logic reconfigurable cell (DG-DLRC)

Dynamic logic is generally more compact (in terms of device count) than static complementary logic when implementing complex logic functions, since it does not require a complementary p-device network and thus demonstrates reduced total parasitic capacitance and silicon area, in particular for cells with a large number of inputs. However, this approach requires clock lines and imposes more stringent constraints on device off currents, since leakage leads to a deterioration of calculated results.

A simple set of configuration codes (i.e. back-gate voltage sets) can be applied to configure an *m*-input reconfigurable cell to a particular logic function from those available (NAND, NOR, INV). After having identified the type of function, the presence of each input D_x ($\forall x \in \{2,m\}$) is evaluated, enabling the corresponding configuration codes $\{C_{xa},C_{xb}\}$ to be extracted from Table 1.

Table 1. General configuration code table for *m*-input DG-DLRC

Function	D_x present in expression		D_x absent from expression	
	C_{xa}	C_{xb}	C_{xa}	C_{xb}
NAND	0	V^-	V^+	V^-
NOR	V^- [1]	0	V^- [1]	V^-
INV	V^-	0	V^- [1]	V^-

For the **NAND**-configuration, 0V is applied to C_{xa} such that transistor M_{xa} operates as a normal n-transistor (i.e. on or off for D_x equal to logic "1" or "0" respectively) when D_x is present in the expression. If D_x is not in the expression, then transistor M_{xa} is turned completely on with $C_{xa}=V^+$. Independently of the presence of D_x in the expression, V^- is applied to C_{xb} to turn transistor M_{xb} off (regardless of the logic value

[1] unless D1 is present in the expression (in this case, $C_{xa}=V^+$)

of D_x). An asymmetric device must be used for M_{xb} to increase the front-gate threshold voltage and thus enable complete turn-off in the NAND-configuration. The value of V^- must be chosen with respect to the gate breakdown voltage limitation. The resulting effective threshold voltage is chosen such that the functionality of the NAND-configuration is met without affecting that of the NOR or INV configurations.

In the **NOR**-configuration and when D_1 is present in the expression, V^+ is applied to C_{xa} in order to significantly decrease the threshold voltage of M_{xa} and turn it completely on, regardless of the logic state of the signal at the front gate. If D_1 is not in the expression, then transistor M_{xa} must be turned off with $C_{xa}=V^-$. If D_x is in the expression, then 0V is applied to C_{xb} for normal operation of transistor M_{xb}, otherwise M_{xb} is turned off with $C_{xb}=V^-$.

In the **INV**-configurations, a single branch is activated to switch with D_1 only (by turning M_{xa} completely on with $C_{xa}=V^+$, and turning M_{xb} completely off with $C_{xb}=V^-$) or with D_x only (by turning M_{xa} completely off with $C_{xa}=V^-$, and selecting normal operation with M_{xb} by applying $C_{xb}=0$). For the latter operation, it is also possible to use $C_{xa}=0V$ to include M_{xa} in switching with D_x (all other control voltages in this branch should then be set to V^+), but this results in non-deterministic timing behavior (since the drive strength depends on the state of D_1).

Static-logic reconfigurable cell DG-SLRC

Static logic styles generally feature better noise immunity than dynamic logic, and thus are well-suited to applications that require resistance to harsh environments. The novel *m*-bit static-logic reconfigurable cell structure (DG-SLRC) is shown in Figure 3. In addition to the n-device branch described in the previous section, DG-SLRC requires a p-device branch composed of:

- one network containing *m* parallel asymmetric DG MOSFETs (with $T_{oxf} > T_{oxb}$)
- a stack of *(m-1)* symmetric DG MOSFETs.

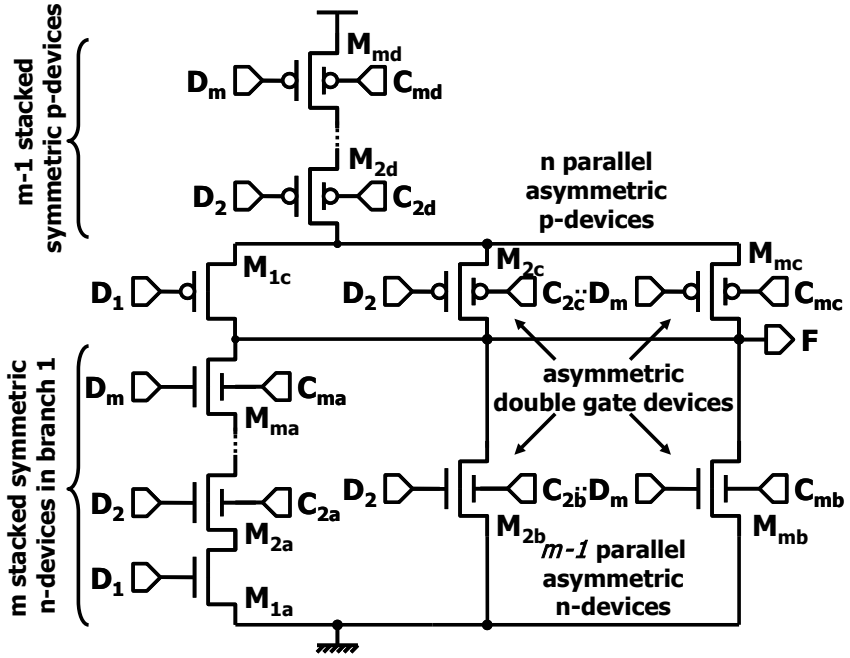


Fig. 3. Generic DGMOS static-logic reconfigurable cell (DG-SLRC)

As before, the front gates of these devices are controlled by the *m* logic inputs. *4(m-1)* control signals are applied to the back gates in order to configure the logic function at the output dynamically. The configuration codes $\{C_{xa},C_{xb}\}$ to be extracted for the various functions are given in Table 2.

Table 2. General configuration code table for *m*-input DG-SLRC

Function	D_x present in expression				D_x absent from expression			
	C_{xa}	C_{xb}	C_{xc}	C_{xd}	C_{xa}	C_{xb}	C_{xc}	C_{xd}
NAND	0	V^-	V^+	0	V^+	V^-	V^+	0
NOR	V^- [2]	0	V^+	V^+	V^- [2]	V^-	0 [2]	0
INV	V^-	0	0	V^+	V^- [2]	V^-	V^+	0

In the **NAND**-configuration and when D_x is present in the expression, 0V is applied to C_{xa} for normal operation of transistor M_{xa}, while V^- is applied to C_{xb}. Since M_{xb} is asymmetric, this device is turned completely off, regardless of the value of D_x. V^+ is applied to C_{xc} for normal operation of M_{xc}, while 0V is applied to C_{xd} in order to turn M_{xd} on regardless of the value of D_x. If D_x is not present in the expression, then M_{xa} is turned completely on ($C_{xa}=V^+$) and M_{xb} completely off ($C_{xa}=V^-$). Here again, 0V is applied to C_{xd} in order to turn M_{xd} on regardless of the value of D_x. V^+ is applied to C_{xc}; this voltage does not ensure that the p-type DG MOSFET M_{xc} is switched completely off, although the off-state is nearly reached due to the

[2] unless D_1 is present in the expression (in this case, $C_{xa}=V^+$)

asymmetric structure of M_{xc} with high T_{oxf}. However, this situation means that power performance is likely to be poor, and the output logic "0" level is degraded (simulation results in the 2-input case show 60mV). To avoid this, the strength (i.e. W/L) of M_{xc} must be reduced.

In the **NOR**-configuration and when D_1 is present in the expression, V^+ is applied to C_{xa} in order to ensure M_{xa} is always on, while 0V is applied to C_{xb} for normal operation of transistor M_{xb} (if D_x is in the expression; otherwise M_{xb} is turned off with $C_{xb}=V^-$). If D_1 is not in the expression, then transistor M_{xa} must be turned off and V^- is applied to C_{xa}. In the p-device network, V^+ is applied to C_{xc} to approach the off-state of M_{xc} if D_1 is in the expression ($C_{xc}=0V$ and M_{xc} is completely on if not) and V^+ is applied to C_{xd} for normal operation of M_{xd} (if D_x is in the expression; otherwise M_{xd} is turned on with $C_{xd}=0V$).

In the **INV**-configurations, a single branch is activated to switch with D_1 only or with D_x only. In the first case, in the n-device network M_{xa} is turned completely on with $C_{xa}=V^+$, and M_{xb} completely off with $C_{xb}=V^-$; while in the p-device network we apply $C_{xd}=0V$ to turn M_{xd} completely on, and $C_{xc}=V^+$ to approach the off-state for M_{xc}. In the second case, we turn M_{xa} completely off with $C_{xa}=V^-$, and select normal operation for M_{xb} by applying $C_{xb}=0V$ in the n-device network; while in the p-device network we set $C_{xd}=V^+$ to achieve D_x-dependent switching, and $C_{xc}=0V$ to turn M_{xc} completely on.

Tests with two-input DG-XLRC

In this section we consider the implementation, in both dynamic- and static-logic forms, of the previously presented reconfigurable cell in its 2-input form. The design of the cells was based on the double-gate FD-SOI/CMOS technology model mentioned earlier, and simulations were performed throughout with a calculation rate of 50Mbit/s (i.e. data period=20ns), using signal rise and fall times of 40ps. The load capacitance considered was 5fF.

Two-input DG-DLRC

Figure 4 illustrates the 2-input reconfigurable cell (with logic inputs D_1=A and D_2=B), implemented with DG devices and based on dynamic logic [11]. Transistors M_1, M_4, and M_5 depict symmetric DG devices (i.e. symmetric oxide thicknesses and workfunctions for the front and back gates) with connected front and back gates. Transistor M_2 depicts a symmetric DG device, while transistor M_3 depicts an asymmetric DG device. Both M_2 and M_3 use independent gate control. For this mixed (symmetric and asymmetric devices) cell denoted DG-DLRC_mixed, asymmetric biasing is used with $\{V^+,V^-\}=\{1.0V,-0.5V\}$.

Another variant of the cell, DG-DLRC_asymm, uses only asymmetric DG MOSFETs. The use of the same device type in the cell can be more convenient since it eases circuit fabrication. In this case, $V_{dd}=0.6V$ to achieve symmetric gate biasing on C_{2a} and C_{2b} where $\{V^+,V^-\}=\{+0.6V,-0.6V\}$ while using a maximum absolute gate-source and gate-drain voltage value of 1.2V .

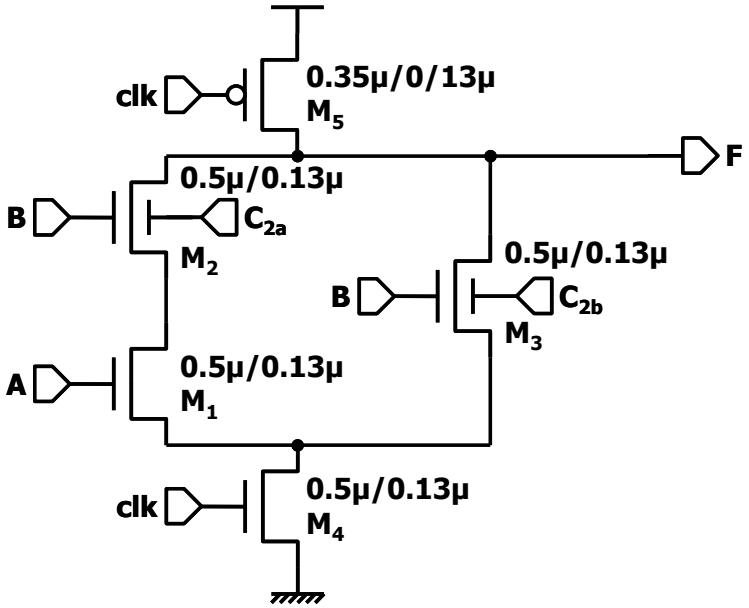


Fig. 4. Two-input DG-DLRC

Table 3 shows the logic state of the cell output (node F) with respect to the applied back gate voltages on the C_{2a} and C_{2b} terminals, as a 2-input implementation of Table 1. As can be observed from Table 3, the cell can implement the NAND, NOR, INV and unconditional '1' and '0' logic functions.

Table 3. Truth table of two-input DG-DLRC

C_{2a}	C_{2b}	Function
0	V^-	NAND(A,B)
V^+	0	NOR(A,B)
V^+	V^-	INV(A)
{0, V^-}	0	INV(B)
V^-	V^-	1
X	V^+	0

This cell has been evaluated using the simulation conditions described previously. The simulation waveforms for DG-DLRC_mixed are shown in Figure 5, where the switching from one configuration to another, as can be observed at the output F, is obtained through the dynamic configuration of signals C_{2a} and C_{2b}. Similar waveforms are obtained with DG-DLRC_asymm.

The power and delay performance characteristics of both variants are summarized in Table 4 for each function configuration. The reconfigurable cell performance (average power and worst case delay) depends not only on the activity factor, the total switched capacitance and device number lying on the critical path, but also on the different back gate biasing used in each configuration. These factors affect, differently

from one configuration to another, the total drive current, sub-threshold and gate leakages, and consequently the total power and the worst case delay.

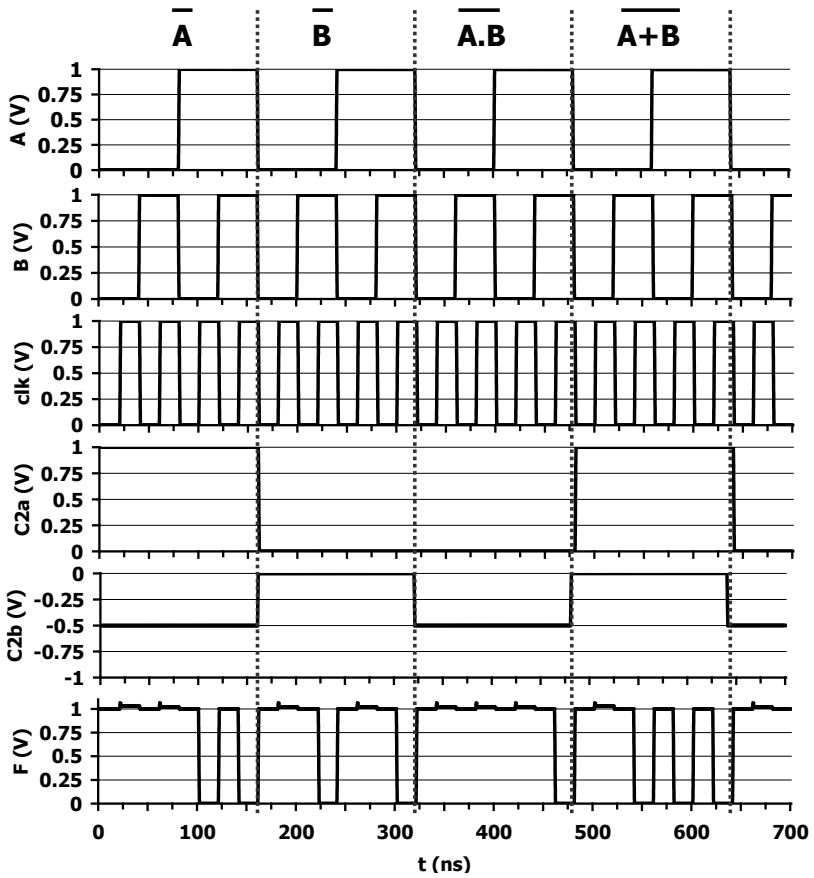


Fig. 5. Simulated configuration of the two-input DG-DLRC to NAND, NOR and INV functions

Table 4. Simulated performance figures for the two-input DG-DLRC

Function	DG-DLRC_mixed			DG-DLRC_asymm		
	Av. power (nW)	Worst-case delay (ps)	PDP (fJ)	Av. power (nW)	Worst-case delay (ps)	PDP (fJ)
NAND(A,B)	256	140.6	0.04	33.2	540	0.02
NOR(A,B)	476.7	740.6	0.35	96.2	2590	0.25
INV(A)	361	140.6	0.05	71.9	2590	0.19
INV(B)	476.3	667	0.32	46.8	2440	0.11

Two-input DG-SLRC

The 2-input static reconfigurable cell (with logic inputs D_1=A and D_2=B) is shown in Figure 6. The truth table of the cell is shown in Table 5, as a 2-input implementation of Table 2. As with DG-DLRC, this cell implements the NAND, NOR and INV functions. Each logic function is obtained by applying the relevant configuration codes in terms of back gate biases $C_{2a\text{-}d}$, as shown in Table 5.

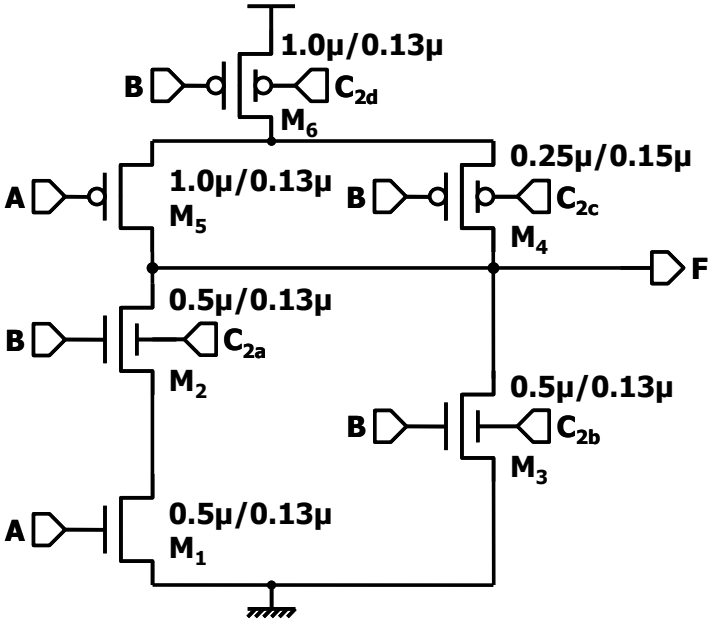


Fig. 6. Two-input DG-SLRC

Table 5. Truth table of two-input DG-SLRC

C_{2a}	C_{2b}	C_{2c}	C_{2d}	F
0	V^-	V^+	0	NAND(A,B)
V^+	0	V^+	V^+	NOR(A,B)
V^+	V^-	V^+	0	INV(A)
{0, V^-}	0	0	V^+	INV(B)
V^-	V^-	0	0	1
X	V^+	V^+	V^+	0

As with DG-DLRC, the static variant can also be implemented using all asymmetric DG devices (as DG-SLRC_asymm). In this case V_{dd}=0.6V and symmetric biasing is used with $\{V^+,V^-\}=\{+0.6V,-0.6V\}$. Correct functionality is observed with this cell due to:

- the reduced V_{dd}/V_{th} ratio (V_{th} ≈0.4V with V_{bg}=0V), thus allowing cut-off of transistor M_3 when V^- is applied to its back gate

- the small W/L ratio for transistor M_4 combined with the small V_{dd}/V_{th} ratio.

The simulation results obtained from both DG-SLRC_mixed and DG-SLRC_asymm are shown in Figure 7. The power and delay performance characteristics of both variants are summarized in Table 6 for each function configuration.

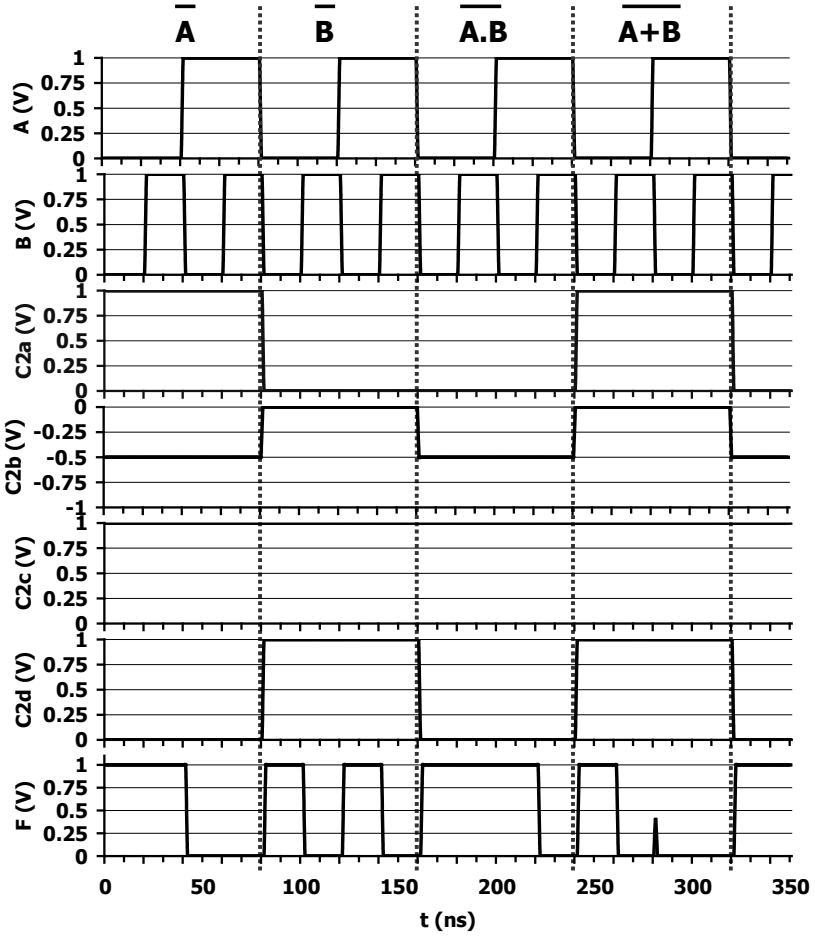


Fig. 7. Simulated configuration of the two-input DG-SLRC to NAND, NOR and INV functions

Table 6. Simulated performance figures for the two-input DG-SLRC

Function	DG-SLRC_mixed			DG-SLRC_asymm		
	Av. power (nW)	Worst-case delay (ps)	PDP (fJ)	Av. power (nW)	Worst-case delay (ps)	PDP (fJ)
NAND(A,B)	1189	590.5	0.70	126	1620	0.20
NOR(A,B)	182	309.4	0.06	197	660	0.13

INV(A)	2800	111.5	0.31	331	660	0.22
INV(B)	397	295.3	0.12	102	1740	0.18

Comparison to conventional LUT and discussion

We have carried out experiments to evaluate the performance gain of DG-xLRC with respect to conventional solutions. While this technique can be considered to open up many possibilities for new system-level programming paradigms, it is also possible to consider the cell family to be a set of incomplete look-up tables (LUTs) [12] and make a direct comparison to conventional *m*-bit MUX-based LUTs (the reference structure of which is shown in Figure 8). It should be noted that the aim of this section is to provide an objective comparison at the circuit level using individual characteristics, rather than a system-level comparison where the impact of cell characteristics is not so clear.

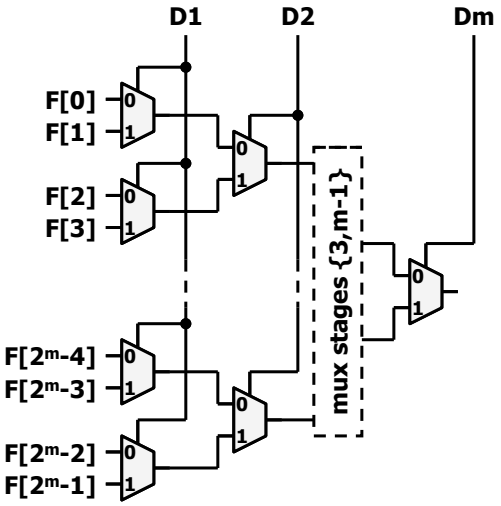


Fig. 8. Reference *m*-bit MUX-based look-up table

Gate area and memory requirements

For 2-, 3- and 4-input LUTs and DGMOS-based reconfigurable cells, we evaluated the gate area (i.e. channel dimensions only), and the required number of memory cells to retain the configuration codes (Figure 9).

The gate area results reflect the exponential and linear growth of transistor count in LUTs and DG-xLRCs respectively. For LUTs, the transistor count grows with $N_{mux}*(2m-1)$ (where m represents the number of inputs and N_{mux} represents the 2-1 MUX transistor count, usually equal to 12), while transistor count grows with $3+2(m-1)$ and $2+4(m-1)$ for DG-DLRC and DG-SLRC respectively. Total area comparisons

incorporate extra interconnect requirements (an extra -V power line, precharge and evaluation lines for the dynamic cell, double inputs) with some reduction in configuration lines for certain variants. The complete layouts (including all routing but excluding configuration memory cells and precharge/evaluate logic buffers) for the 2-input dynamic and static cells show area reduction factors of 6.5 and 4.7 respectively as compared to the CMOS-LUT, instead of 7.8 and 4.9 considering gate area only. The precharge/evaluate logic and signal distribution tree was not included in the analysis.

The number of memory cells required has an impact not only on auxiliary hardware requirements, but also on configuration time. For LUTs, this increases with *2m*, while for DG-DLRC and DG-SLRC it is equal to *2(m-1)* and *4(m-1)* respectively.

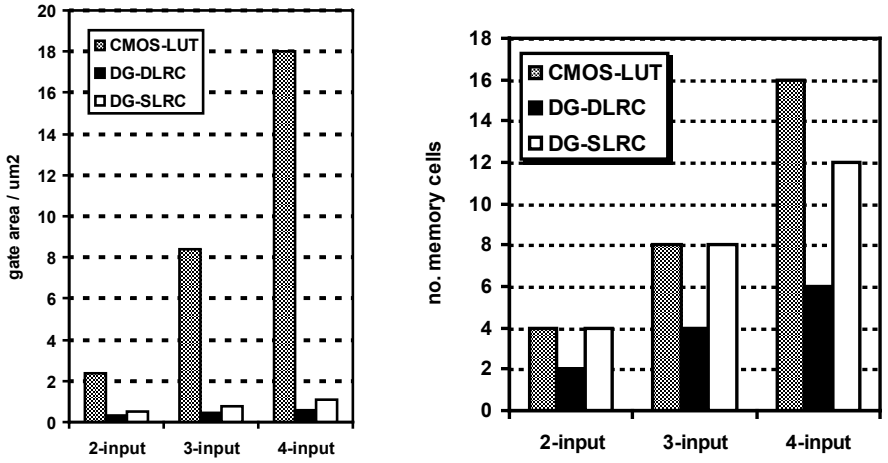


Fig. 9. Comparison of m-input DG-xLRC and CMOS-LUT characteristics (a) gate area (b) no. memory cells

It should of course however be borne in mind that while a LUT potentially offers configurations, DG-xLRC offers rather less. The number of available functions corresponding to *m*-input cells is plotted in Figure 10 and compared to the figures for CMOS-LUTs for values of *m* ranging from 2 to 6. In practice, the number of inputs that the reconfigurable cells can reasonably handle is 4. Beyond this figure, the number of series devices in a stack becomes too high.

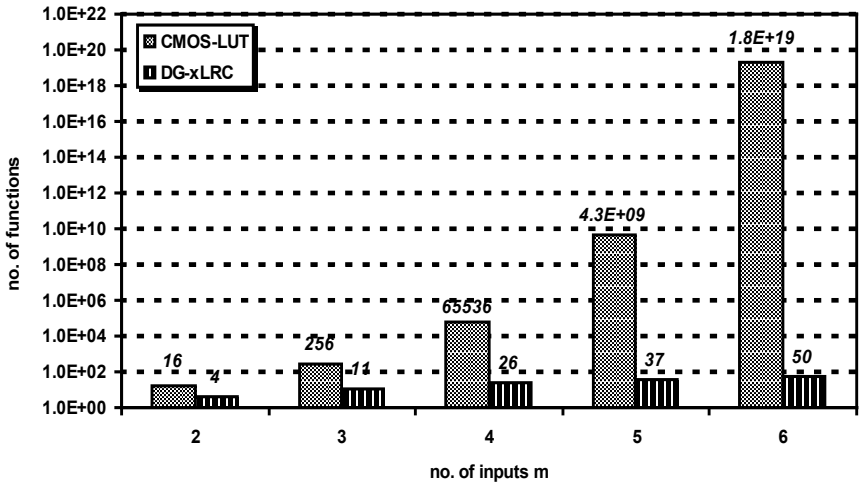


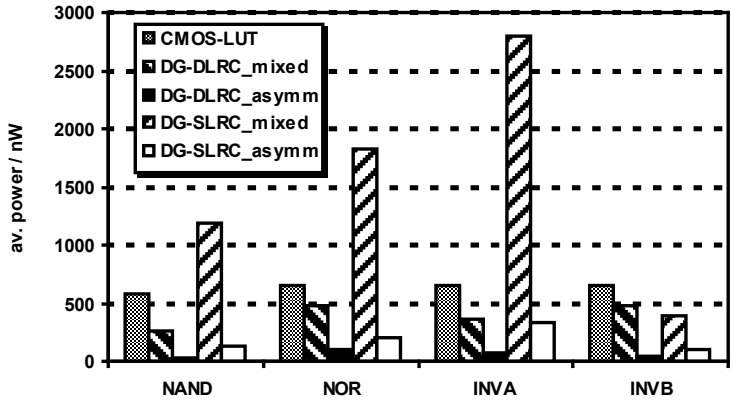
Fig. 10. Number of available functions for m-input reconfigurable cells

It is clear from this figure that a direct transposition of this cell as a LUT in conventional configurable logic blocks will result in limited flexibility. For this reason we believe that further work must be carried out to explore new programming paradigms to benefit from the cell performance (and in particular its reduced configuration memory requirements for easier dynamic reconfiguration) at system level.

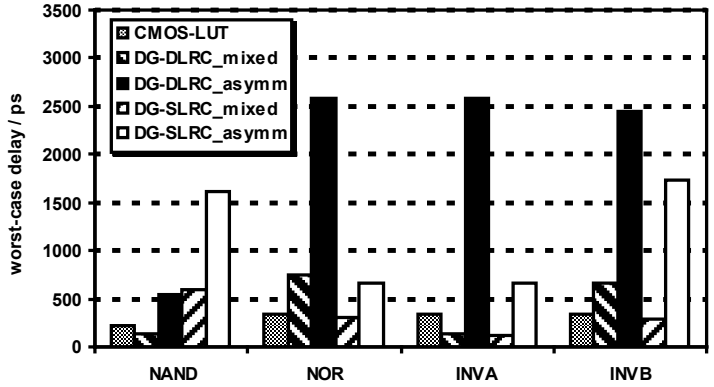
Average power and worst-case delay

We have also carried out detailed simulations of the 2-input solutions to compare average power and worst-case delay performance metrics. To this end we have simulated the LUTs in a 65nm CMOS technology. The choice of this reference technology was based on a comparison of oxide thicknesses, doping levels, mobility parameters and gate metal types. However, since the reconfigurable cells use 130nm gate lengths (for reasons of model validity and lack of technological maturity) the 65nm CMOS standard cell transistor dimensions were scaled to match the gate lengths and achieve comparable parasitic capacitance values and a fair basis for comparison.

Identical simulation conditions were used, i.e. 50Mbit/s calculation rate, load capacitance C_L=5fF, 40ps rise and fall times on inputs. Comparisons of the CMOS-based LUT figures were carried out for the four operational functions with respect to both DG-DLRC and DG-SLRC, in mixed and all-asymmetric variants (Figure 11).



(a)



(b)

Fig. 11. Comparison of two-input DG-xLRC and CMOS-LUT characteristics (a) average power (b) worst-case delay

These figures clearly show that, apart from the mixed implementation of DG-SLRC, total power performance is systematically better with DG-xLRC solutions, in one case achieving an average of over 90% reduction in power over the four function configurations. For static power, it should be noted that all configurations of both static and dynamic logic cells (except the unconditional '0' configuration) bias N-type and P-type DGMOS back gates to 0V / V^- and V^+ respectively (leading to either the same or lower I_{off} as with connected gates), except when an unconditional short is required – in which case the off current of the branch is defined by another transistor in the equivalent configuration to that of a connected gates transistor. This means that the low I_{off} values of DGMOS transistors are exploited in the proposed cells (our simulations show I_{off} = 0.7pA for an N-type DGMOS of 0.5µm/0.13µm with t_{oxf}=2.5nm and t_{oxb}=1.2nm) – however the I_{on} values are lower than a connected-gates

equivalent transistor since the back gate is set to 0V or V^+ for N- and P-type conducting transistors respectively. The peak current value for a transistor with the previously cited characteristics (i.e. for $V_{fg}=V^+$ and $V_{bg}=0V$) is around 50µA. This has an impact on the cell drive current, and the consequences are visible in Figure 11 in terms of the mediocre worst-case delay comparison. The best achievement is an overall 20-30% delay penalty for the mixed solutions. Additional technology and circuit optimization should enable some tradeoff between power and speed through the improvement of cell drive current (by increasing device width) – but clearly the power, gate area and I_{off} will all deteriorate by such a strategy.

Overall recommendations are that (i) the all-asymmetric device reconfigurable logic cells using $\{V^+,V^-\}=\{0.6V,-0.6V\}$ are best-suited to low power reconfigurable circuits operating with moderate speed, while (ii) the mixed-device reconfigurable cells using $\{V^+,V^-\}=\{1.0V,-0.5V\}$ can operate at comparable speeds to CMOS-LUTs but only the dynamic-logic variant shows benefits in terms of power.

Conclusion

In this paper, we have presented a new style of reconfigurable cell dedicated to programmable logic applications and based on the DG MOSFET device, particularly exploiting those with asymmetric oxide thicknesses for the front and back gates and independently controlled gates. Significant gate area reductions are possible compared to conventional CMOS LUT techniques (between 80-95%) while configuration memory requirements are also reduced (up to 60%). The 2-input reconfigurable cell used as a benchmark was implemented in both static and dynamic logic styles. Simulation results in DG FD SOI/CMOS technology of the proposed cell have shown that it can be used either as an all-asymmetric device variant with low V_{dd} (0.6V) in low power reconfigurable applications (up to 90% power reduction is possible) or as a mixed-device variant with a higher V_{dd} (1V) to achieve comparable speeds to CMOS-LUTs (20-30% penalty).

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