Analysis and Design of Charge Pumps for Telecommunication Applications

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Abstract. This chapter addresses modern telecommunication integrated circuits from the synthesizer focal point; in particular it concentrates at the analysis and the design of integrated charge pump circuit blocks. It presents an overview of charge pump topologies in addition to a coherent analysis of the associated benefits and shortcomings of all circuit alternatives. Moreover a novel favorable charge pump combining current steering techniques with well utilized unity gain buffers in a novel, noiseless feedback scheme, is introduced to improve on switching speed, inherent charge pump ac noise, dead-zone interval, therefore overall steady state aliased loop noise; while on the other hand this charge pump exhibits superb DC matching characteristics in a wide output voltage range. Furthermore a well documented estimation of the active devices that contributes mostly to the overall charge pump noise performance is presented. Also an associated mathematical analysis concerning the frequency content of the charge pump noise current is given. This proposed topology manifests its applicability to charge pump alternatives, as it is demonstrated by the associated simulation results from a 0.18μm design. Because of the low-noise and accurate properties of this improved charge pump, it is ideally suited to modern telecommunication standards synthesizer realizations.

1 INTRODUCTION

Fully monolithic Phased-Locked Loops (PLLs) are essential building blocks, widely used in modern communication or complex digital systems [1-8]. A PLL based on a charge pump is often preferred over other synthesizer alternatives, because it exhibits a wide capture range with no systematic phase offset and arguably provides one of the simplest and most effective design platforms [9-14]. The Charge Pump based PLL also provides flexible design tradeoffs by decoupling various design parameters such as the loop bandwidth, damping factor and lock range [22]. Figure 1 shows a typical implementation of a charge pump based PLL. It consists of a Phase/Frequency Detector (PFD), a Charge Pump (CP), a Loop Filter (LF), a Voltage Controlled Oscillator (VCO) and a divider. The most widely used PFD generates a pair of digital pulses corresponding to the phase/frequency error between the reference clock f_{ref} and the VCO output, by comparing the positive (or negative) edges of the two inputs. The CP circuit converts the digital pulses into an analogue current which is consequently integrated producing a voltage on the passive (or active) loop filter. This voltage drives the VCO circuit block

which in turn produces the synthesized frequency of operation as it is demanded by the system specification.

However, some non-idealities of the CP such as DC mismatch of the charging/discharging currents and glitches degrade the performance of the overall loop. Moreover the noise of the charge pump is the dominant close-in phase noise contributor in a PLL [15]. Several charge pump implementations have been proposed in the associated literature [16-18]. In [16, 17] an opamp has been used in order to keep the dc mismatch current, and hence the resultant phase offset at a minimum level and improve the overall performance. This in effect adds significant noise contribution at the output of the proposed charge pump due to the increased gain introduced by the opamp. Others [18] assume that the Up and Dn signals from the PFD that drive the charge pump switches could not be simultaneously high, to avoid the dc mismatch between the pump-up and pump-down currents. This is a fallacy because at lock both the Up and Dn signals are high for a given short time to ensure the elimination of the PLL dead-zone, which if present will degrade significantly the in-band noise suppression characteristic function of the PLL.

The objective of this chapter is the design of an improved single-ended low noise charge pump with low dc mismatch current, high voltage output range and programmable gain. The second section depicts some typical charge pump architectures either for single-ended or differential design, along with the advantages and disadvantages of each category. In the third section a detailed analysis of the improved charge pump is presented and compared to other alternative designs. Also the noise contribution of the improved charge pump active devices to the total output noise is given with the appropriate mathematical noise analysis. In the fourth section the simulation results from three alternative methods (DC, PSS and Pnoise) are presented, over temperature and process corners for the charge-pump key specifications to signify the applicability of the overall approach. Finally the key concluding remarks of this chapter are given in the last section.

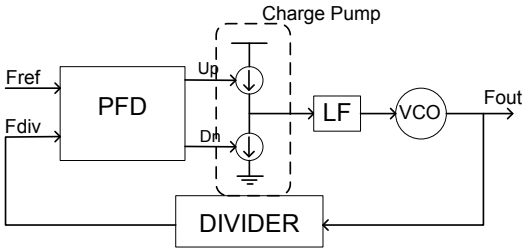

Figure 1. Block level diagram of a charge pump based PLL

2 CMOS CHARGE PUMP ARCHITECTURES

2.1 Single-ended charge pump architectures

Single-ended charge pump circuits are an elegant approach to system flexibility, low-power consumption, minimization of pads and external components, or area. The output current of the charge pump can be as high as 4.5mA [23] at lock to provide better spur performance thus less leakage current and to have high SNR for low noise contribution to the PLL, while this current can be significantly more while the PLL is in the tracking period, to improve on settling time. By using tri-state operation, the current consumption of the charge pump is limited to a few hundred μA depending on the reference clock frequency and the delay of the PFD. Figure 2 shows some typical single-ended charge pump topologies.

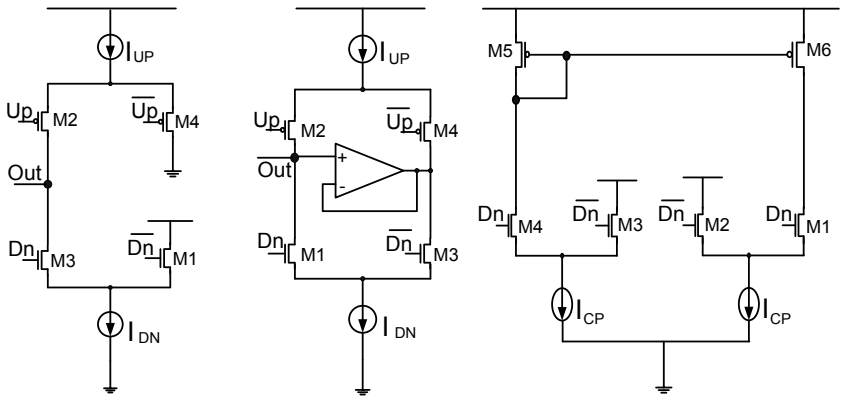

Figure 2. Single-ended charge pump architectures: a) with current steering switch, b) with unity gain active amplifier and c) with NMOS switch only

Figure 2a shows a charge pump utilizing a current steering switch. This structure provides high speed switching for a single-ended charge pump, since the switching time is improved by the current steering properties of the associated switching pair (M1-M3 and M2-M4). Another charge pump approach utilizing current steering with an active amplifier [24-25] is shown in figure 2b. This unity gain amplifier, buffers the voltage at the output node forcing the drain voltage of the current sources I_{DN} and I_{UP} to be the same when M1 and M2 are on or when they are off. This reduces the charge sharing effect, when the switch is turned on. This architecture ensures fast transient response through current steering, reduces the effect of any parasitic capacitance, at the expense of extra current. Finally, in figure 2c the inherent mismatch of pmos and nmos transistor is avoided by using only nmos switches [26]. Since the current does not flow in the current mirror, (M5 and M6), when the UP switch is turned off, the current mirrors still limit the performance unless large current is used [3].

2.2 Differential charge pumps

A fully differential charge pump has several advantages over the conventional single-ended charge pump [27-28]. Firstly, the switch mismatches between nmos and pmos transistors do not substantially affect the overall performance. This relaxes the matching requirement between the two type of transistors. Secondly, the differential charge pump has only nmos switching transistors thus the inverter delays for the Up and Dn signals are fully symmetric and therefore do not generate any offset. Thirdly, this configuration doubles the range of the output voltage compliance compared to the single-ended charge pump. This is a significant advantage for low voltage operation, since the limited output voltage range of the charge pump makes it difficult for the VCO to meet the specified tuning range. Fourthly, the differential output stage is less sensitive to the leakage current, since the leakage current behaves as a common-mode offset at the dual output stages. Lastly, the use of two on-chip loop filters provides better immunity to the supply, ground and substrate noise, while the lack of bond wire inductors facilitates faster switching speeds and reduces transient oscillations. However, these advantages can only be achieved at the cost of extra area due to the use of two loop filters, common-mode feedback circuitry [3], higher noise levels and power consumption imposed by the potential introduction of an active filter and most importantly the flexibility of altering the overall PLL loop characteristics by changing the loop filter should this prove desirable.

3 IMPROVED CHARGE PUMP DESIGN

The improved accurate low noise charge pump is shown in figure 2. It is a single-ended tri-state charge pump with programmable gain. This topology exhibits improved switching speed, since all nodes are precharged to the resultant operating points and the current is either steered to the output or to the unity-gain buffer. The two opamps O_{P1} and O_{P2} are used in order to minimize the DC mismatch current that will be introduced by the output voltage variation. The O_{P1} and O_{P2} inputs are connected at the drains of the corresponding transistors as it is shown in figure 3, while the opamp outputs drive the gates of transistors M3 and P1 respectively.

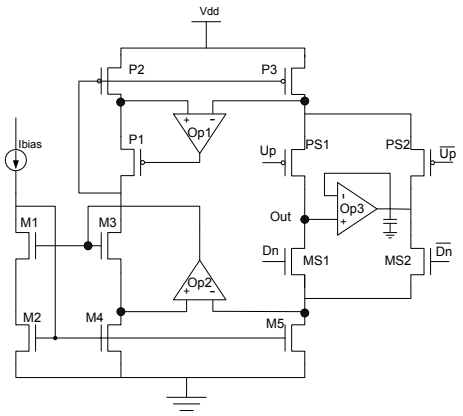

Figure 3. Improved Charge Pump Circuit

3.1 Characteristics of the Improved Charge Pump Approach

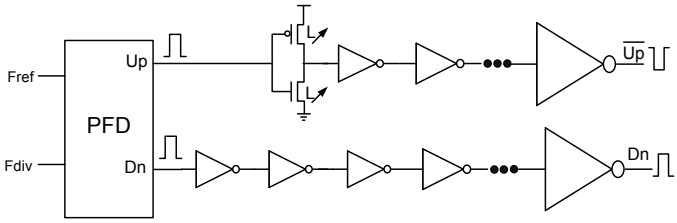

Figure.4. Buffer chain between PFD and CP

In the improved circuit transistors M1, M2, M3 and M4 compose a cascode current mirror with increased output resistance and minimized channel length modulation. This cascode connection offers the advantage of low voltage operation for the charge pump. The bias current (Ibias) from the input branch is mirrored to the output branch where P3 and M5 act as current sources. The current source mirroring ratio is 4, which means that the output current is four times larger than Ibias. MS1 and PS1 are the transistor switches which are driven by the Dn and Up signals from the PFD. When the Up signal is low, the PS1 switch is turned on and the current Iup from P3 charges the loop filter capacitor, increasing the output voltage. On the other hand when the Dn signal is high, the MS1 switch is turned on and the output voltage is decreased by the discharging current Idn that flows through M5. Transistors MS2 and PS2 are the switches which are driven by the complementary Up and Dn signals, providing a constant current flow path when the switches MS1 and PS1 are off. This implies a fast switching operation at the expense of increased power consumption.

When the loop is locked, both switches are on for a small fraction of the time. At lock both MS1 and PS1 have to switch on and off simultaneously to

reduce the noise introduced in the loop and the magnitude of the $2 \cdot f_{ref}$ and consequent spurs. For this reason a buffer with a timing synchronization scheme which constitutes from two chains is used; the first chain is used to generate the Up signal and the second to generate the Dn signal. This buffer placed between PFD and CP, as shown in figure 4. The scaling ratio for the inverters is chosen to be close to 4 [19], in order to achieve the best power, speed and area trade-off. Also the channel length L, of the nmos and pmos transistor in the first inverter of the Up signal is increased to equalize the delay between the two timing control signals introduced by the asymmetry of the two chains [7]. Synchronization can also be achieved by using the two paths of the chain, where the first one includes an extra inverter compared to the second one and introduce an active resistor (a transmission gate adequately dimensioned) in the second path. In addition to that the dimensions of the switches must be properly sized, in order to turn on and off simultaneously.

An important advantage of the improved CP circuit is the low DC mismatch between the pump up and pump down currents. The two opamps O_{P1} and O_{P2} are used in order to minimize this DC offset current. As it is shown in figure 3, the two inputs of O_{P1} and O_{P2} are connected to the drains of P2-P3 and M4-M5 transistors respectively, forming a closed loop. If the output voltage increases to lock at a higher frequency, then the voltage at the drain of M5 increases as well. Because of the O_{P2} the same voltage is forced on the drain of M4. Likewise O_{P1} forces the voltage to the drains of P2 and P3 to be almost the same. As a result, the same amount of current flows between the two branches, for a wide output voltage dynamic range.

The dimensions W/L of the current source transistors that is M5 and P3 are chosen in such a way to minimize the current mirroring mismatch from the input to the output branch. Also the systematic current variation due to any residual in the V_{DS} despite the presence of the opamps has been remedied by choosing large gate lengths for the current source transistors. In addition the PS1 and MS1 transistor switches, which operate in the linear region, have been designed with minimum gate length, in order to achieve maximum output voltage range.

Moreover the unity gain amplifier O_{P3} plays an important role, since it sets the voltage at the drain of the switches PS1 and MS1 at the output node. Thus the charge sharing effect becomes minimal when the switches turned on. It also increases the switching-speed of the charge pump due to current constant flow from P3 to M5, even when the PLL is locked. Hence the charge and discharge of the parasitic capacitances at the drain node of P3 and M5 is avoided. This increases switching speed, therefore the dead zone and the resultant noise contribution is reduced during the lock condition at the expense of a small current consumption introduced by O_{P3}, since it only needs to source or sink a small P and N mismatch current. Finally a compensation capacitance has been added at the output of the amplifier, to increase the phase margin, as denoted

by an associated stability analysis. Moreover it acts as a charge reservoir during switching transitions.

3.2 Comparison to Alternative Approaches

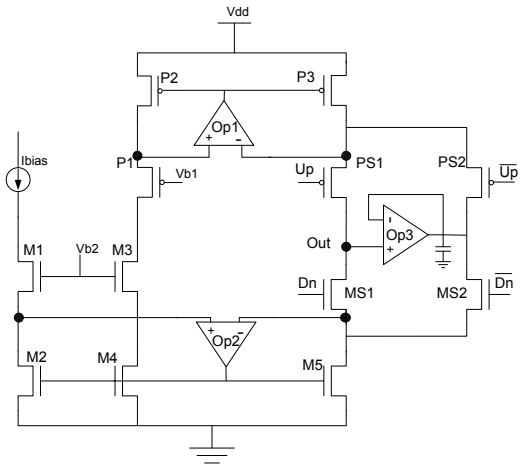

Figure. 5. Opamp drives directly the gates of P2 and P3

The significant improvement compared to similar, alternative charge pump implementations [16, 17] is in essence due to the fact that the output of the opamps drives the gates of the cascode transistors and not the gates of the current source transistors directly. In the improved approach P1 is connected as a source follower, resulting to a significant reduction of the O_{P1} noise contribution at the charge pump output.

For example in the case where the O_{P1} drives directly the gates of P3 and P2 transistors, as shown in figure 5, the noise current i^*_{out1} generated at the output of P3 is given by the following equation:

$$i^*_{out1}{}^2 = gm^2_{P3} \cdot V_n^{*2} \tag{1}$$

where Vn^{*2} represents the output referred voltage noise of the opamp O_{P1} (both flicker and thermal) and gm is the transconductance of the current sinking transistor. From the above equation it can be seen that the noise current is the product of the noise voltage and the transconductance of P3. In our case, as shown in figure 3, the output of O_{p1} is connected to the gate of P1 instead of P3. Taking into account that P2 acts as a current source with a finite large output resistance r_o, the noise current of P2 is equal to:

$$i^{*}{}_{n2}{}^{2} = \frac{V_n^{*2}}{r_o^{2}} \tag{2}$$

This current produces a noise voltage at the gate of P2 equal to

$$v_{n2}{}^{*2} = \frac{i^{*}{}_{n2}{}^{2}}{gm^{2}{}_{P2}} \tag{3}$$

Thus the noise current that appears to the output of P3 is given by the equation:

$$i^{*}{}_{out2}{}^{2} = gm^{2}{}_{P3} \cdot v_{n2}{}^{*2} = \frac{gm^{2}{}_{P3} \cdot V_n^{*2}}{gm^{2}{}_{P2} \cdot r_o^{2}} \tag{4}$$

Therefore the ratio of the improved charge-pump over the one in [16] is given by the equation:

$$\frac{i^{*}{}_{out2}{}^{2}}{i^{*}{}_{out1}{}^{2}} = \frac{1}{gm^{2}{}_{P2} \cdot r_o^{2}} \tag{5}$$

For example if common modern transistor values r_o=72kΩ and g_m=2.84mS are subsidized in the above equation, a significant reduction by 45dB, of the Op1 induced noise at the output is obtained.

3.3 Analysis and Estimation of Noise Contributors of the Improved Charge Pump

The analytical estimation of the noise contribution, from the charge pump transistors is presented in this section. As it is well known the flicker (1/f) and thermal (white) noise from the active devices are the dominant noise sources that affect the overall noise performance of the charge pump. The noise plot of an active device (MOS or Bipolar transistor) is shown in figure 6, which has only two distinctive regions; thermal noise and 1/f region. The 1/f noise corner is in the vicinity of 500kHz to 1MHz for a sub-micron CMOS technology and it is in the vicinity of 1kHz to 10kHz for bipolar transistor [21].

There are three different combinations for the charge pump switching conditions which are given in the following table:

Table 1.

Signals	MS1	PS1
Up(low), Dn(high)	On	On
Up(low), Dn(low)	Off	On
Up(high), Dn(high)	On	Off

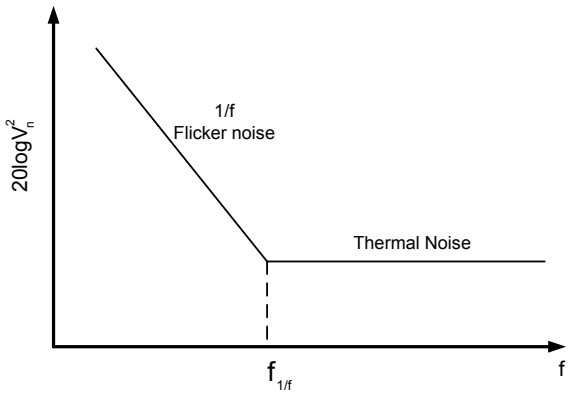

Figure. 6 Noise characteristics of a MOS transistor at a fixed bias voltage

1. PS1 on and MS1 on

The first condition is when the two transistor switches are both on for a small fraction of time corresponding to the locked condition of the loop.
For the flicker noise estimation a noise voltage source is placed at the appropriate gate device and the resultant noise current is calculated at the output of the transistor. So in this condition the transistors that affect the total noise of the charge pump are: M2, M4, M5, P2, P3. g_{mni} and g_{mpi} are the transconductances for nmos and pmos transistors respectively, where index *i* indicates the number of the corresponding transistor. For the noise calculation the flicker noise is easily modeled as an equivalent voltage source $V^*_n{}^2$ in series with the gate of a MOS transistor and roughly given by the following equation

$$V^*_n{}^2 = \frac{K_f}{C_{ox} \cdot W \cdot L} \cdot \frac{1}{f} \tag{7}$$

where K_f is a process-dependent constant on the order of 10^{-25} V^2F, C_{ox} is the oxide capacitance, W and L are the width and length of the transistor respectively. The inverse dependence of (7) on W, L suggests that to decrease 1/f noise, the device area must be increased.
Taking into account that $W_{M2}=W_{M4}$, $W_{P2}=4\cdot W_{M4}$ and $W_{P3}=4\cdot W_{P2}=16\cdot W_{M2}$ the total output noise current is given by the following expression:

$$
\begin{aligned}
i^*_{n,out}{}^2 &= g_{mp3}{}^2 \cdot V^*_{n4}{}^2 + g_{mp3}{}^2 \cdot V^*_{np3}{}^2 + g_{mp3}{}^2 \cdot V^*_{np2}{}^2 + g_{mn5}{}^2 \cdot V^*_{n5}{}^2 = \\
&= g_{mp3}{}^2 \cdot V^*_{n4}{}^2 + g_{mp3}{}^2 \cdot V^*_{np3}{}^2 + g_{mp3}{}^2 \cdot V^*_{np2}{}^2 + g_{mn5}{}^2 \cdot V^*_{n5}{}^2 = \\
&= i^*_{n2}{}^2 + \frac{1}{4} i^*_{n2}{}^2 + \frac{1}{4} i^*_{n2}{}^2 + \frac{1}{16} i^*_{n2}{}^2 \Rightarrow i^*_{n,out}{}^2 = \frac{25}{16} i^*_{n2}{}^2
\end{aligned}
\tag{8}
$$

where $i^*_{n2}{}^2$ is the output reffered noise current of transistor M2. It should be noted that the first two terms which are the summation of the noise current from M2 transistor are cancelled by the third term; the negative sign of this third term comes from the fact that the two noise currents $g_{mn5}{}^2 \cdot V^*_{n2}{}^2$ and $g_{mp3}{}^2 \cdot V^*_{n2}{}^2$ are fully correlated with a phase difference of 180 degrees to each other (for the actual CP switching frequencies). This is because the P3 transistor sources current while M5 transistor sinks the same noise current. Moreover these transistors have equal transconductances, since the ratio of their mobilites is equal to the ratio of the dimensions W/L for the same current.

2. PS1 off and MS1 on

In the second condition only M2 and M5 transistors are taken into account since they affect the charge pump noise and the total output noise current is given by the following expression:

$$
i^*_{n,out}{}^2 = g_{mn2}{}^2 \cdot V^*_{n2} + g_{mn5} \cdot V^*_{n5}{}^2 = i^*_{n2}{}^2 + \frac{1}{4} i^*_{n2}{}^2 = \frac{5}{4} i^*_{n2}{}^2 \tag{9}
$$

The diode connected M2 produces a noise current $i^*_{n2}{}^2$ which is mirrored at the output of the charge pump. M5 acts as a current sink producing also a noise current which is four times smaller than the noise current of M2, because its width is four times larger than the width of M2, as depicted in (7).

3. PS1 on and MS1 off

In the last operating condition the output noise current consists of the noise currents of the M2, M4, P2 and P3 transistors. M5 does not contribute any noise at the output because the MS1 switch is in the off state. Taking into account that $W_{M2}=W_{M4}$, $W_{P2}=4 \cdot W_{M4}$ and $W_{P3}=4 \cdot W_{P2}=16 \cdot W_{M2}$ the total output noise current is given by the following expression:

$$
i^*_{n,out}{}^2 = g_{mn2}{}^2 \cdot V^*_{n2} + g_{mn4} \cdot V^*_{n4}{}^2 + g_{mp2}{}^* \cdot V^*_{np2}{}^2 + g_{mp3}{}^2 \cdot V^*_{np3}{}^2 = \tag{10}
$$

$$= i^*_{n2}{}^2 + i^*_{n2}{}^2 + \frac{1}{4} i^*_{n2}{}^2 + \frac{1}{16} i^*_{n2}{}^2 = \frac{37}{16} i^*_{n2}{}^2$$

Comparing the results from the three different operating conditions, a significant conclusion is obtained. In the first case, though both the switches MS1 and PS1 are on, the circuit does not exhibit higher noise. This is because the noise current generated by the M2 transistor is fully correlated in both the pmos and nmos branch and therefore cancelled at the output of the charge pump. The most noisy operation state is the last one where the PS1 switch is on and the MS1 switch is off. In the third section of the chapter these noise calculations will be confirmed by the associated simulation results.

3.4 Spectral Components of the Charge Pump Output Signal

In this section an attempt to calculate the spectral components of the output signal Iout, as a function of the phase error $\Delta\theta$, between f_{ref} and f_{div}, is presented. In the following analysis it is assumed that the output of the charge pump consists of current pulses of amplitude I_{cp}. It is also assumed that there is no mismatch between the current sources (M5, P3) of figure 3. The duty cycle of the output pulse is equal to τ/T_{ref}, where τ is the active time of the charge pump output current and T_{ref} is the period of the reference signal. From the signal processing theory [20] it is known that the Fourier series expansion for a periodic train of pulses of amplitude I_{cp} and duration τ is:

$$I_{out}(t) = \frac{I_{cp}\tau}{T_{ref}} + 2\frac{I_{cp}\tau}{T_{ref}} \sum_{n=1}^{\infty} \frac{\sin(n\pi\tau / T_{ref})}{n\pi\tau / T_{ref}} \cos(\frac{2\pi nt}{T_{ref}}) \quad (11)$$

The equation (11) can be expressed as a function of the phase error $\Delta\theta$, taking into account that the ratio τ/T_{ref} is proportional to $\Delta\theta/2\pi$:

$$I_{out}(t) = \frac{I_{cp}\Delta\theta}{2\pi} + 2\frac{I_{cp}\Delta\theta}{2\pi} \sum_{n=1}^{\infty} \frac{\sin(n\pi\frac{\Delta\theta}{2\pi})}{n\pi\frac{\Delta\theta}{2\pi}} \cos(\frac{2\pi nt}{T_{ref}}) \quad (12)$$

If the duty cycle δ_{cp} equals to τ/T_{ref} and for small values of the δ_{cp}, the sinc function $\sin(n\pi\tau/T_{ref})/(n\pi\tau/T_{ref})$ can be approximated as unity. This results in the following expression for I_{out}:

$$I_{out}(t) = I_{cp}\delta_{cp} + 2I_{cp}\delta_{cp} \sum_{n=1}^{\infty} \cos(2\pi n f_{ref} t) \quad (13)$$

which shows that the amplitude of the spectral components of I_{out} are twice as large as its dc value $I_{cp}\delta_{cp}$. Therefore, if $\delta_{cp}=\Delta\theta/2\pi$ equals to zero the charge pump output ideally contains no dc or ac signal components.

The next step is to study the effect of mismatch in current sources. Mismatch originates in the different type of devices used to implement the n-type current sink, which sinks current from the output node to ground and the p-type current source which sources current from the supply to the output node. Moreover the nominal current supplied by the n-type and p-type current sources is likely to be a function of the voltage at the output node of the charge pump. This is filtered by the loop filter producing the tuning voltage V_{tune} to the oscillator, and therefore it is a function of the output frequency of the entire loop. If $V_{mismatch}(n\cdot f_{ref})$ is the magnitude of the ripple voltage at the fundamental and harmonics of the reference frequency, then the equation which relates the above voltage with the current-source mismatch is given below:

$$V_{mismatch}(n\cdot f_{ref}) = I_{out}(n\cdot f_{ref})\cdot\left|Z(j2\pi n f_{ref})\right| \tag{14}$$

where $\left|Z(j2\pi n f_{ref})\right|$ is the magnitude of the transimpedance function of the loop filter and n ranging from 1 to ∞.

It is common to express the magnitude of the undesired signal components with respect to the magnitude of the carrier frequency f_{LO}. From the standard modulation theory [20] the relationship of the peak phase deviation $\theta_p(f_m)$ to the peak frequency deviation $\Delta f(f_m)$ and the modulation frequency f_m is given by

$$\theta_p(f_m) = \frac{\Delta f(f_m)}{f_m} \tag{15}$$

The peak frequency deviation is the product of the magnitude of the spectral components of the mismatch voltage $V_{mismatch}(n\cdot f_{ref})$ with the gain K_{VCO}(V/Hz) of the VCO:

$$\Delta f(f_m) = V_{mismatch}(n\cdot f_{ref})\cdot K_{VCO} \tag{16}$$

Combining (14) and (16) and substituting into (15) we get the peak phase deviation due to each of the spurious frequency components $n\cdot f_{ref}$

$$\theta_p(n\cdot f_{ref}) = \frac{I_{out}(n\cdot f_{ref})\left|Z(j2\pi n f_{ref})\right|\cdot K_{VCO}}{n\cdot f_{ref}} \tag{17}$$

Each of the baseband modulation frequencies $n \cdot f_{ref}$ generates two RF spurious signals, which are located at offset frequencies $\pm n \cdot f_{ref}$ from the carrier frequency f_{LO}. The amplitude of each spurious signal A_{sp} is related to the magnitude of the carrier A_{LO} and to the peak phase deviation θ_p by

$$A_{sp}(f_{LO} \pm n \cdot f_{ref}) = A_{LO} \frac{\vartheta_p(n \cdot f_{ref})}{2} \tag{18}$$

Substituting (17) into the numerator of (18) the following expression in dB is obtained

$$\left[\frac{A_{sp}(f_{LO} \pm n \cdot f_{ref})}{A_{LO}} \right]_{dBc} = 20 \cdot \log \frac{I_{out}(n \cdot f_{ref}) \left| Z(j2\pi n f_{ref}) \right| \cdot K_{VCO}}{2 \cdot n \cdot f_{ref}} [dBc] \tag{19}$$

An important conclusion that can be drawn from (19) is that the relative amplitude of the spurious signals is independent on the absolute value of loop bandwidth or on the nominal charge-pump current I_{cp}. Instead, they are determined by the transimpedance of the loop filter, by the magnitude of the reference spurious components, by the VCO gain and by the value of the reference frequency.

3.5 Noise Performance of Charge Pump

An ideal CP-PLL with zero phase error neither sources current to, nor sinks current from, the loop filter. However, PLLs with zero phase error are insensitive to small loop-phase deviations due to finite rise times in the PFD and charge pump which is also called the “dead zone”. A commonly employed solution to “dead-zone” is to use an artificial phase offset so that CP pumps/sink current when PLL is locked. When the PLL is locked the average output current flowing into the filter is zero. Both the currents from the P3 and M2 transistors in figure 3, are on for the duration of the “dead zone” pulse. Even though the average current is zero, noise is injected from both transistors currents for the duration of the “dead zone” pulse. The charge pump noise current injected to the loop filter under lock condition can be calculated as,

$$i^*_{n,out}{}^2 = 2 \cdot \left(\frac{\delta_{cp}}{T_{ref}} \right) \cdot I^2_{n,CP} \tag{20}$$

where constant factor 2 is used to account for the source and sink current pulses. $I^2_{n,CP}$ is the noise current of the CP in A^2/Hz. δ_{CP} is the dead zone

pulse width and T_{ref} is the reference period signal. The above equation suggests that if the reference frequency is increased then more noise will be injected into the loop filter and in consequence to the VCO circuit block. Moreover the PLL close-in phase noise will increase with the reference frequency by a factor proportional to $10 \cdot \log (f_{ref})$. Also a "dead zone" pulse with large duration leads to an increased noise as depicted by equation (20).

4 Simulation Results

The improved charge pump was designed using 0.18um CMOS technology. The supply voltage was 2.5Volt for the charge pump and inverters in the buffer chain. Simulations were obtained by using Cadence design framework with spectre device models from UMC 0.18um and 0.35um devices. The pump up and pump down currents are 1mA from a 2.4V power supply. The CP design includes a programmable gain by a step of 250uA. Corner and temperature analysis has also been performed, in order to further the demonstrability, applicability and robustness of the improved circuit. The percentage of DC mismatch current over output voltage of the improved CP, for three different process and temperature worst cases (typical─$0 \cdot \sigma$ @ 27^{o}C, slow─ $-3 \cdot \sigma$ @ 85^{o} C, fast─$+3 \cdot \sigma$ @ -45^{o}C) as shown in figure 7.

The circuit is able to operate with a mismatch current less than 2.25% at the typical case and 2.5% at the extreme process/temperature conditions. The output voltage ranges from 300mV to 2.2V. Beyond these limits, transistors close to the supply rails (P3, M5), leave the saturation and enter to the linear region of operation, which results to an increased mismatch current. The power consumption of the improved charge pump including the three opamp consumption is roughly 6.65mW for a 2.4 power supply voltage.

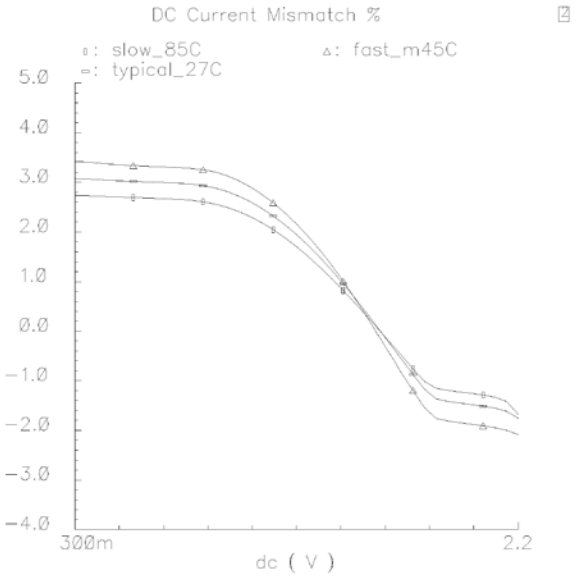

Figure. 7. The dc mismatch of the output current vs output voltage

A periodic noise analysis (Pnoise) has also been performed in order to obtain the noise contribution of the devices at the output of the charge pump. Figure 8 illustrates the noise power spectral density of the output current, when the loop is locked, which means that the transistors are on for a small fraction of time that is equal to the reset delay of the PFD. This time delay is 500ps, which results in a duty cycle of 0.5%. Because of the fast switching characteristics of the improved charge-pump even smaller duty cycles can be used, further reducing the close in noise contribution of the charge pump by as much as 6dB!

Due to the delay added in the reset path of the PFD, the current sources (P3, M5) are on for small or zero phase errors. The dumped charge on the capacitor of the loop filter as a function of the phase error is illustrated in figure 9. The X axis represents the phase error in time. A maximum 180 degrees phase deviation corresponds to 50ns.

In addition to that a second periodic noise analysis has been performed to confirm the validity of equation (20). The three plots in figure 10 represent the power spectral density of the charge pump noise current for three different duty cycles. As it can be observed, increased duty cycle leads to an increased noise to the charge pump output.

To verify the theoretical noise analysis and highlight the active noise contributors of the charge pump, an ac noise simulation has been done for the circuit. Three different cases have been simulated for typical model transistor and room temperature (27C) and the results are given in the following tables.

At the first column is given the corresponding noise contributor transistor and at the second column is the simulated current noise at a specific spot frequency (f=1Hz for this case).

Table 2.

PS1 on MS1 on	
Noise Contributors	Noise Current (A^2/Hz)
M4	2.3e-16
M5	5.8e-17
P2	3.15e-17
P3	7.95e-18

Table 3.

PS1 off MS1 on	
Noise Contributors	Noise Current (A^2/Hz)
M2	1.875e-16
M5	5.61e-17

Table 4.

PS1 on MS1 off	
Noise Contributors	Noise Current (A^2/Hz)
M4	8.4e-16
M5	2.3e-16
P2	5.25e-17
P3	13.15e-18

The most significant noise contributors have been obtained for each case in consistency with the theoretical analysis, which is given in the previous section. It is worthy to note that M2 in table 2 does not produce any noise contribution, due to the correlation of the current noise components which cancel each other at the output. Moreover nmos transistors contribute higher amount of noise current than pmos transistor due to their higher mobility.

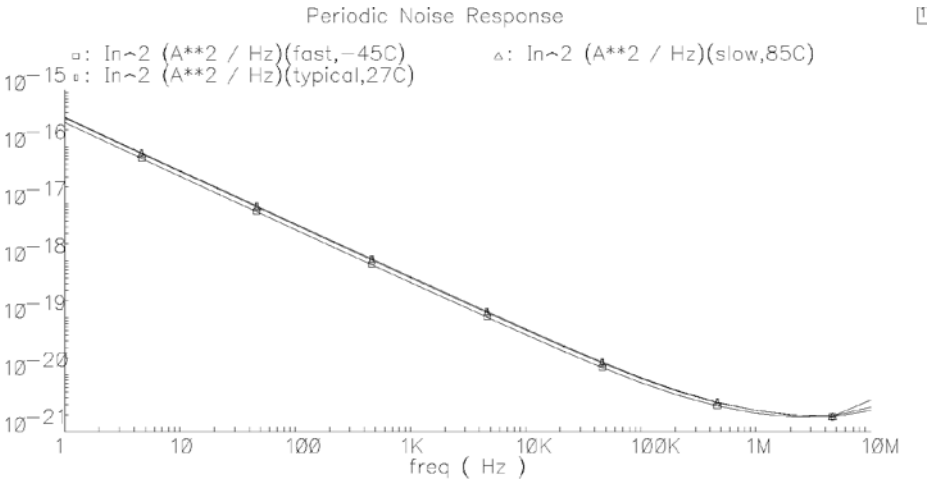

Figure. 8. Noise power spectral density from Pnoise analysis

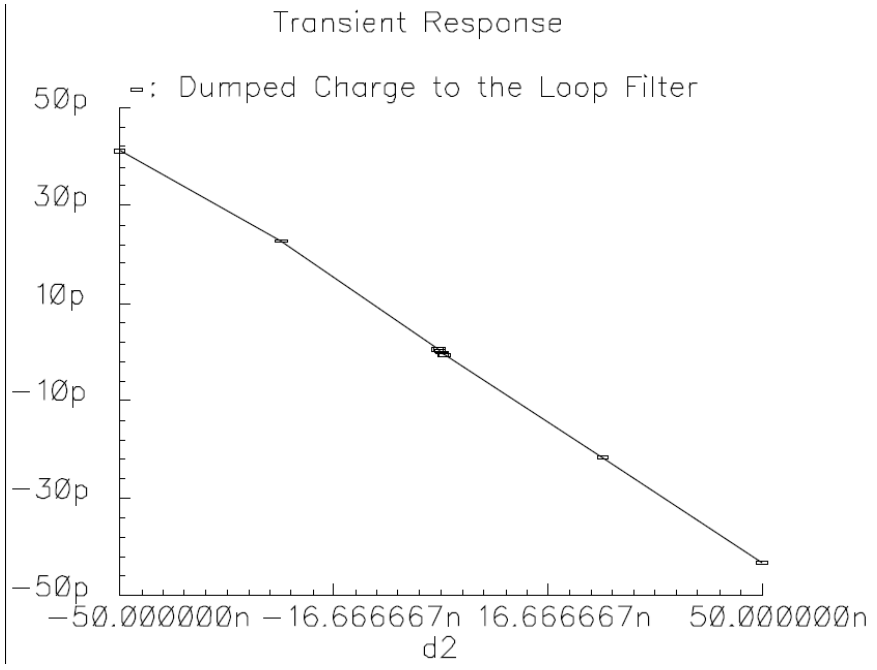

Figure. 9. Dumped charge as a function of phase error

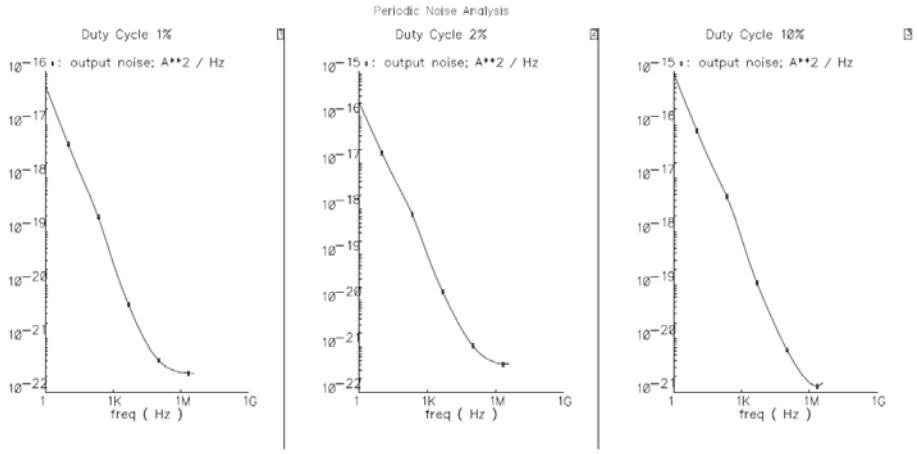

Figure 10. PSD of CP Current Noise for three different Duty Cycle

5 Conclusions

The design and analysis of a low noise charge pump has been presented in this chapter. Low noise charge pumps are essential to modern telecommunication systems, because they dominate the close-in noise of the associated synthesizer. In modern GSM, CDMA or OFDM standards the noise of the PLL is defined by the in-band noise, since the VCO noise can be reduced by simply opening the loop bandwidth to hit the VCO phase noise characteristic in a more attenuated level at a higher frequency which is especially true nowadays with the evolution of the fractional-N synthesizers. Therefore the low-noise properties of the charge pump are becoming increasingly more essential.

The improved charge-pump (figure 3) performs better than older alternatives, because it uses the current steering technique to switch on and off, therefore minimizes delays. Furthermore the introduction of O_{P3} at figure 3 ensures that all nodes are pre-charged to their final levels, and therefore less time is needed for the circuit to settle, furthering the initial speed improvement. Fast switching speed in essence demands a smaller dead-zone time and thus minimizes the noise contribution of the charge pump at lock (and non-lock) condition.

Inherent noise of the charge-pump is reduced by adding the stabilizing opamp circuits in an improved fashion compared to other alternatives [16, 17, 18]. By adding this novel feedback approach it is possible though to improve on output matching, without increasing noise. The improved charge-pump accuracy over the full output range, expressed by an excellent P/N mismatch, ensures that there is a limited systematic DC offset and therefore the spurious content is smaller, thus making it easier to meet the modern $2 \cdot f_{ref}$ spurious content specifications, which are steadily decreasing in size.

In table 5 alternative advanced CP families are compared, to provide a good perception of the improvement introduced by the circuits presented in the current chapter.

Table 5.

CP version	Switching Speed	Noise Performance	DC mismatch
Cheng et al.	Very Good	Good	Good
Rapinoja et al.	Medium	Good	Good
Chang et al.	Good	Medium	Good
This approach	Very Good	Very Good	Very Good

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