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Abstract. Network-on-Chip (NoC) is viewed as a viable substitution for traditional interconnection networks to achieve high performance, communication efficiency and reliability in complex VLSI architectures at deep sub micron. Achieving high performance, power efficiency with optimum area is a target for any routing algorithm in NoC. In this paper, we propose a novel routing scheme named 'ERA', which offers higher throughput with controlled delays while remaining power aware. ERA is an adaptive routing algorithm, which avoids congestion and tends to minimize the hot spots in the network. Unlike other existing algorithms, the proposed algorithm does not require any virtual channels to avoid deadlocks. We compare our algorithm with XY and OE on the basis of a performance metric called 'power performance factor' for different traffic patterns and injection models. Our results show that ERA performs better than these two algorithms.

Key words: Network-on-Chip, Energy Model, Deterministic Routing, Adaptive Routing, Deadlock, Turn Model, Latency, Throughput

1 Introduction

Regular tile-based NoC architecture has recently been proposed as a solution to interconnect design for complex on-chip designs [1]. This architecture consists of a number of IP cores (DSP, storage or a processing element) and switches/routers. Various IP cores communicate with each other by means of routers.

Routing is essentially how data flows from a source to the destination. It can be deterministic or adaptive. Deterministic routing algorithms allow lower delays due to their simplistic logic when network is not congested [2]. Adaptive algorithms have the ability to sense the network congestion and redirect the packets along the other routes. Adaptivity may lead to uniform traffic and power distribution (minimizing hot spots) in the network and higher throughput.

In this paper, we propose a novel adaptive routing scheme which senses power dissipation on the neighbouring nodes. In this way, it optimizes power and also avoids the congestion occurring in the network. Latency and path length (Manhattan distance of the destination from a node) is taken into account when equal

power dissipation is anticipated in two or more directions. OE turn model [3] is used for routing as it avoids deadlock without the need of any virtual channel (VC). Deadlock can also be avoided by increasing the number of VCs but employing more VCs require adding buffer space and additional control logic to routers; communication performance of the network and reliability of the routers may be affected [3, 4]. OE (Odd Even) turn model approach [3] is preferred for deadlock avoidance instead of the turn model [4] because of its uniformly distributed nature.

This paper is organised as follows. Section 2 presents an overview of the NoC simulators – NIRGAM integrated with ORION used for evaluating the performance statistics and power calculation respectively. Section 3 briefly summarizes the work done in the development of various routing strategies for NoC. Detailed description of the proposed scheme is discussed in Section 4. Section 5 introduces a figure of merit termed power performance factor for multiobjective optimization of power, latency and throughput. Comparative study of the other algorithms with our proposed function is given in Section 6 with detailed results. We finally summarize our work in Section 7.

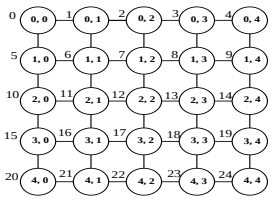


Fig. 1. 2D mesh topology.

2 NoC Simulation Framework

NIRGAM (NoC Interconnect Routing and Application Modelling) [5] is a modular, discrete event and cycle accurate simulator developed in SystemC. In NIRGAM, a 2D interconnect of tiles (Fig. 1) can be simulated with various options of virtual channels, clock frequency, buffer parameters, routing mechanisms and applications, etc. Each NIRGAM tile consists of various components like input channel, controller, virtual channel allocator, output channel controller and an IPcore. Each IPcore is attached to a router/switch by means of a bidirectional core channel. Energy dissipated at these components are calculated using ORION model [6, 7].

ORION [6, 7] is a power simulator used to evaluate power performance tradeoffs in respect of NIRGAM design parameters. ORION can compute static as well as dynamic energy of a component. Power computation is done by passing requisite parameters such as number of buffer reads and writes, crossbar

traversals and arbitrations at each clock intervals through ORIONs functions. Total energy (E_{T}) dissipated across a router in terms of power consumed by its components is expressed as:

$$E_{\mathrm{T}} = E_{\mathrm{buffer}} + E_{\mathrm{arbiter}} + E_{\mathrm{crossbar}} + E_{\mathrm{clk}} + E_{\mathrm{link}} \quad (1)$$

In this manner power dissipated at each router is calculated at each clock cycle using the ORION power models. At each clock cycle, these updated power values are transmitted to the neighbouring routers. Each router has a process sensitive to the power updation event and maintains an array Power[ ] which holds the value of power dissipated at the neighbouring routers. Values stored in Power[ ] is used in the proposed algorithm for uniform power dissipation and minimizing hotspots.

3 Related Work

A number of deterministic and adaptive routing algorithms have been proposed for NoC [8, 9, 2, 10, 11]. Problems like deadlock, livelock and starvation are major issues for a routing function. Routing algorithms can easily avoid livelock by being minimal. Deadlock can be avoided by removing any cyclic dependency between channels. Turn Model [4] prohibits smallest number of turns for preventing cycles to ensure no deadlocks [12]. The degree of adaptiveness offered by turn model is highly uneven. An improvement is OE turn model [3] which provides more even routing adaptiveness. Algorithms like XY, OE, etc are deadlock free without requiring multiple VCs whereas algorithms like PROM [8], MAXY [9], etc. use different VC allocation schemes for achieving deadlock free scenario.

So far, most of the published works either focus on improving performance parameters (throughput, latency) or on minimizing energy needs. To the best of our knowledge, there does not exist any NoC routing algorithm which takes into account both power and performance factors simultaneously to develop an overall efficient routing scheme. ERA is such an efficient routing algorithm which not only guarantees high performance but also helps in the design of low power NoCs by minimizing the power consumption and appearance of hot spots.

4 ERA: An Efficient Routing Algorithm

We propose an adaptive routing algorithm which takes into account power dissipation, congestion as well as the delays encountered in the network. At every node, the set of available directions for the next hop are determined as per OE turn model. For optimizing power dissipation, only those directions are chosen for which the power dissipation is less than the average power computed over all available directions. If the set contains multiple directions, algorithm tends to minimize number of hops by selecting those directions for which product of power and path length (manhattan distance of the next hop node from the destination node) has lower value. Finally for minimizing congestion, we check the availability of buffers in the final two directions and choose the one with more number of available buffers. Proposed method is illustrated in Algorithm 1.

Algorithm 1 ERA: An Efficient Routing Algorithm

Require: S_x, S_y: x and y coordinate of source node
D_x, D_y: x and y coordinate of destination node
C_x, C_y: x and y coordinate of the current node
Power[4]: set containing power at neighbours
Ensure: Routing path from current node.

```
set-avail-final = ∅
p-factor = ∅
set-avail = available directions given by OE turn model
path-len[N] = |D_x − (C_x − 1)| + |D_y − C_y|
path-len[S] = |D_x − (C_x + 1)| + |D_y − C_y|
path-len[E] = |D_x − C_x| + |D_y − (C_y + 1)|
path-len[W] = |D_x − C_x| + |D_y − (C_y − 1)|
if (C_x = D_x) AND (C_y = D_y) then
  return ip-core
end if
for i ∈ { N, S, E, W } do
  if set-avail[i] then
    total-power += Power[i]
    p-factor[i] = path-len[i] * Power[i]
    count-avail-dir++
  end if
end for
average-power = total-power/count-avail-dir
for i ∈ { N, S, E, W } do
  if set-avail[i] then
    if Power[i] < average-power then
      set-avail-final = set-avail-final ∪{i}
    end if
  end if
end for
if set-avail-final has one direction then
  return direction
else
  direction1 = set-avail-final with min p-factor
  direction2 = set-avail-final with 2nd min p-factor
  if buffer[direction1] > buffer[direction2] then
    return direction1
  else
    return direction2
  end if
end if
```

5 Power-Performance Factor (ϕ_f)

For a power aware yet most efficient routing scheme, low power consumption, smaller delays and high values of throughput are desirable. To take all these factors into account, we define a figure of merit, 'power-performance factor' derived from average value of performance metrics – power, latency, throughput.

$$\phi_f = \frac{(\text{average power consumed} * \text{average latency})}{\text{average throughput}} \tag{2}$$

A low value of ϕ_f indicates low average power consumption and latency and/or high average throughput. Lower the value of ϕ_f, better is performance of algorithm in terms of performance metrics.

6 Experimental Setup and Results

NIRGAM [5] integrated with ORION [6, 7] is used for performing simulations to evaluate effectiveness of our algorithm. All the experiments are performed on a 5x5 mesh topology. Flit size is 5 bytes, 1 for the head and 4 for the data payload. Only single VC is used with 32 buffers. Simulations are run for 5000 clock cycles– first 3000 cycles for traffic generation. For power calculations 110nm technology and Clock Frequency of 1 GHz is assumed.

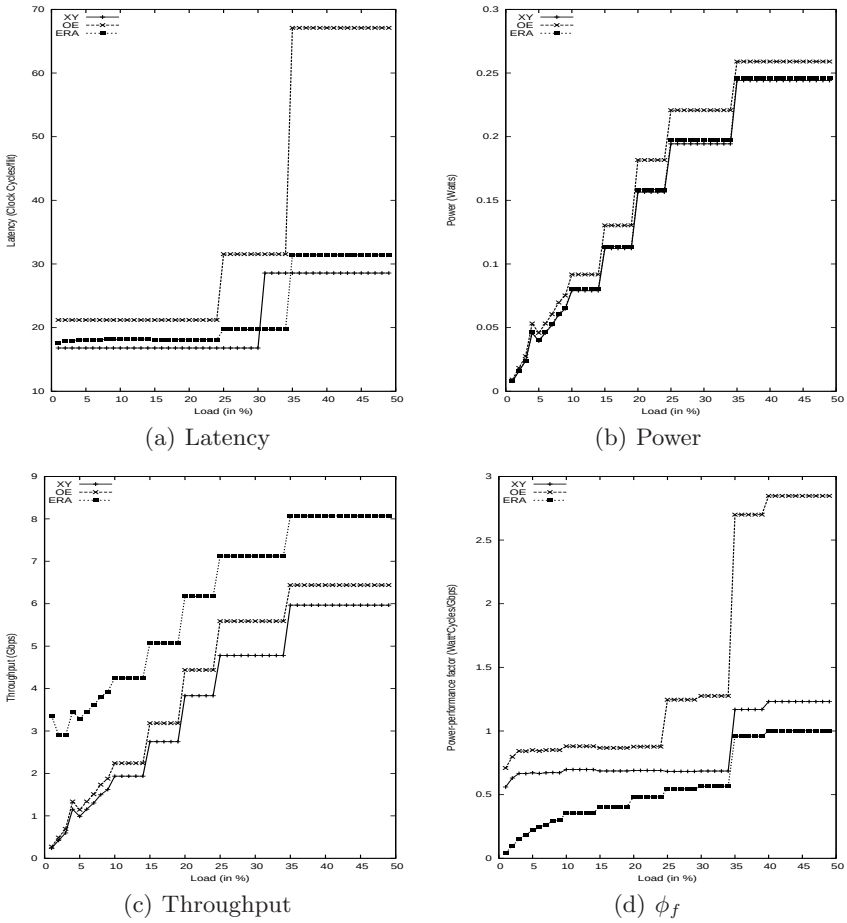
6.1 Transpose and Bit Shuffle Traffic Scenarios

Transpose and Bit Shuffle are synthetic traffic patterns commonly employed for real world applications [13]. Under 'Transpose' traffic scenario, source and destination addresses are represented as a 2-tuple $\langle r, c\rangle$, r is the row and c is the column index. For source at $\langle i, j\rangle$, the destination will be $\langle j, i\rangle$.

In 'bit shuffle', address of a node is represented by $n * r + c$ for a mesh of size nxn. Also for a given source, the destination node is obtained by a circular left shift of the source address. Fig. 1 show both 1-tuple and 2-tuple addresses for nodes in a 5x5 mesh.

Fig. 2(d) and Fig. 3(d) indicate that the ϕ_f is lesser for ERA as compared to both XY and OE. ERA exhibits higher throughput and controlled latency because of its adaptive nature and in-built capability of avoiding congestion through checking the availability of buffers and choosing path of lower power consumption. Under transpose traffic pattern, ERA performs better than OE in all respects i.e. higher throughput, lower latency and lower power consumption. In case of Bit Shuffle, though OE offers higher throughput at higher values of load but ERA performs better in case of power and latency factors resulting in a better power-performance factor in all cases. XY is a simple, minimal and deterministic algorithm with low latency. It does not respond to the congestion taking place in the network and a large part of network bandwidth is left unexploited. This results in lower throughput values for XY than ERA in both transpose and bit shuffle scenarios. Slightly higher value of latency and power in case ERA than XY

is compensated by achieving higher throughput and ERA ultimately succeeds in maintaining lower value for the power-performance factor. As a result, it can be observed that its performance level is better than the other schemes like XY and OE.



(a) Latency (b) Power

(c) Throughput (d) ϕ_f

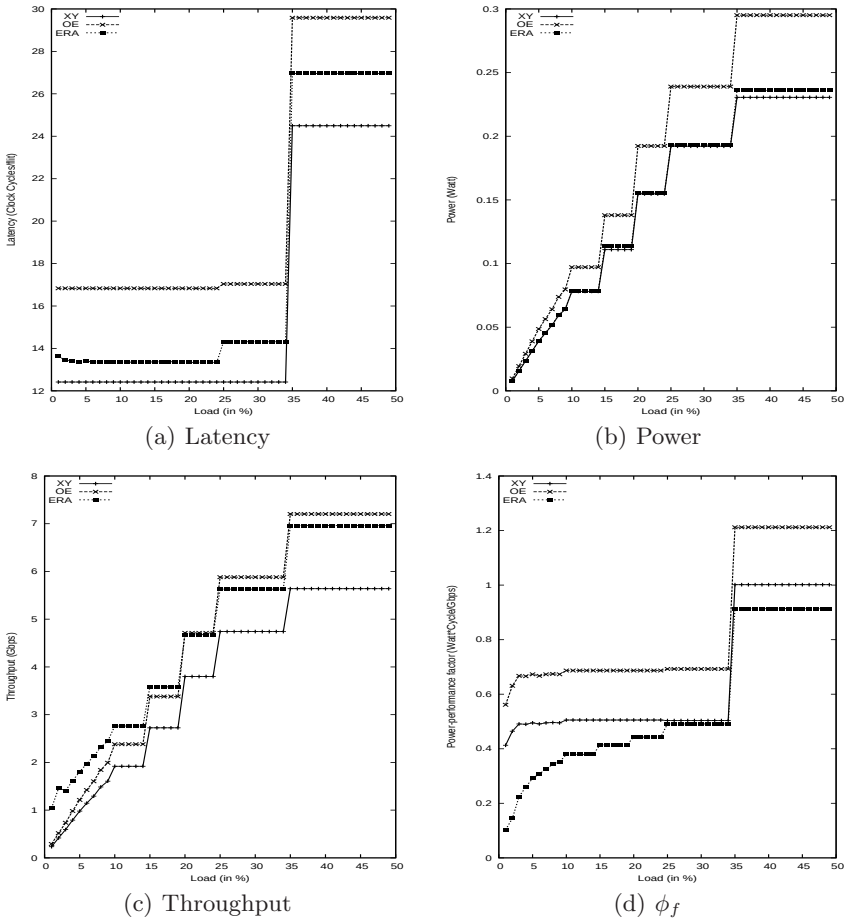
Fig. 2. (a) Latency, (b) Power, (c) Throughput and (d) ϕ_f for XY, OE and ERA under Transpose traffic pattern.

6.2 Multimedia Traffic with Negative Exponential Distribution

Multimedia traffic exhibits the property of self similarity and resembles closely to traffic of the real time applications [14]. It has been reported that NoC traffic shows the property of self similarity [15, 16]. The main configurable parameters

are Hurst Parameter (degree of self-similarity), minimum and maximum size of each frame. The inter frame interval is generated using an exponential distribution.

Negative Exponential Distribution (NED) function as discussed in [17] is used with multimedia traces to get a more realistic scenario. Spatial inter-core communication pattern can be approximated by NED. This characteristic is exploited by using exponential distribution function based on Manhattan distance between source and destination. Keeping Hurst parameter constant (0.81), we



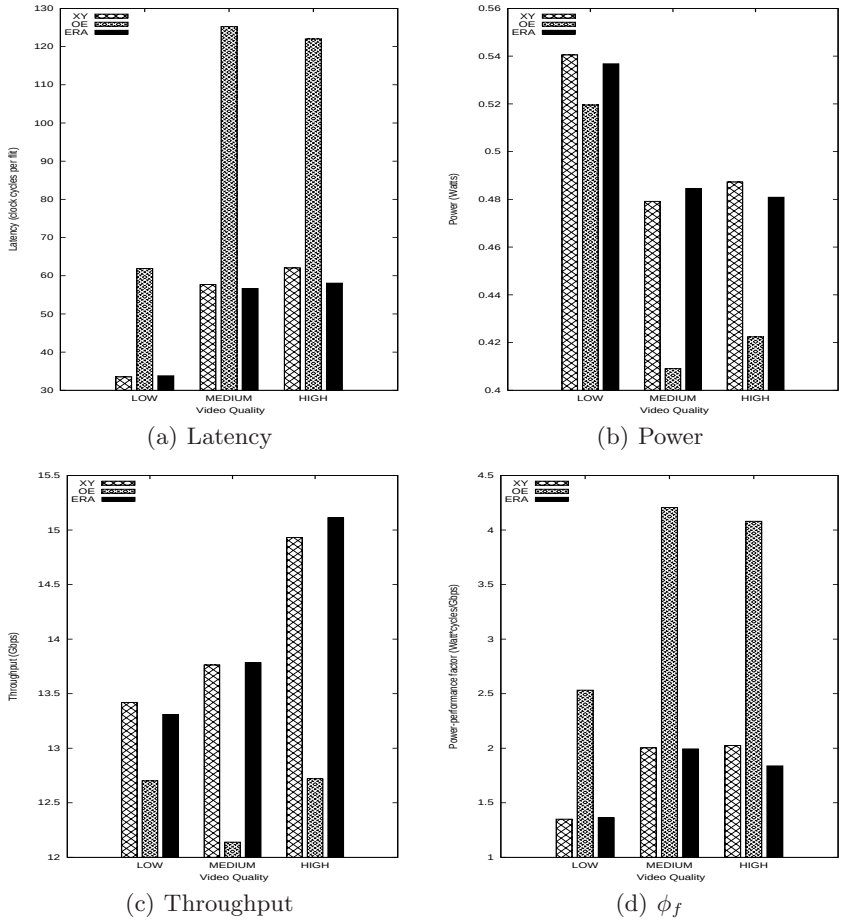
(a) Latency (b) Power

(c) Throughput (d) ϕ_f

Fig. 3. (a) Latency, (b) Power, (c) Throughput and (d) ϕ_f for XY, OE and ERA under bit shuffle traffic pattern.

vary the range of minimum and maximum size of a frame and the average off time between them so as to simulate results for different quality of videos [18].

Flit interval is maintained at 2 clock cycles. Comparison is done for three cases namely low, medium and high quality videos. Multimedia injection model is used with NED traffic pattern. Fig. 4 shows that in all the three scenarios our algorithm performs nearly similar to XY and better than OE. For high quality videos, ERA is better than XY.



(a) Latency (b) Power

(c) Throughput (d) ϕ_f

Fig. 4. (a) Latency, (b) Power, (c) Throughput and (d) ϕ_f for XY, OE and ERA under NED traffic pattern.

6.3 Hot Spot Traffic Scenario

Under hot spot traffic, hot spots are created at nodes where heavy traffic is felt. The percentage defined with respect to a particular hot-spot node determines

the amount of traffic passing through it. In our simulation framework, node 18 is chosen as a hot spot with 30%.

The routing algorithm chooses those paths in which less average power is dissipated from the set of all available directions. In this effort, it significantly helps in the removal of hot spots through uniform power distribution across network. Table 1 depicts the results obtained. We can observe that the percentage of total power dissipated at the hot spot node is more in case of other routing algorithms as compared to ERA. Moreover there is no sensing of power dissipation at the neighbouring nodes by the other algorithms. It can be argued that ERA not only adapts to the congestion in the network but also remains power aware.

Table 1. Power dissipation at the hot-spot and the power performance factor

	XY	OE	ERA
% of total power dissipated at hot spot node	7.156	7.342	5.78
Power performance factor	0.5803	0.5622	0.3670

7 Conclusion

We have presented a novel routing scheme which can consider the performance and power simultaneously. The proposed scheme is adaptive which controls the delay by taking into account the path length and offers high throughput as well by avoiding the congested paths. The proposed method remains power aware as it prioritises the path with low power dissipation and significantly helps in the minimisation of hot spot occurrences. The proposed method outperforms the deterministic algorithms like XY even when the traffic load is high in mesh topology. However, at very heavy loads, XY performs slightly better because of its simplicity and minimality. As can be seen from the results, ERA outperforms OE routing algorithm in terms of latency, throughput and power under all traffic scenarios. ERA requires all the routers to have the information about the power consumption on all its neighbouring routers. The hardware implementation of the algorithm and power calculation for the route logic circuitary can be looked upon as a part of future work. Also detailed studies for comparison of ERA with respect to other existing algorithms will be performed in future.

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