Structural DfT Strategy for High-Speed ADCs

Yolanda Lechuga, Roman Mozuelos, Mar Martínez, Salvador Bracho

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Yolanda Lechuga, Roman Mozuelos, Mar Martínez, and Salvador Bracho

[1]Microelectronics Engineering Group
University of Cantabria Av. de los Castros s/n
39005 Santander, Spain

{yolanda.lechuga, roman.mozuelos, mar.martinez, salvador.bracho}@unican.es

Abstract. This paper presents a Design-for-Test (DfT) approach for folded ADCs. A sensor DfT circuit is designed to sample several internal ADC test points at the same time, so that, by computing the relative deviation among them the presence of defects can be detected. A fault evaluation is done considering a behavioral model to compare the coverage of the proposed test approach with a functional test. Afterwards, a fault simulation is used on a transistor level implementation of the ADC to establish the optimum threshold limits for the DfT circuit that maximize the fault coverage figure.

Keywords: Folding and interpolated A/D converters, Design-for-Test, Circuit simulation, Behavioral modeling, Simulink environment.

1 Introduction

Nowadays, the analogue-to-digital converter is a common block in mixed-mode circuits. Embedded ADCs are used in a wide range of applications such as satellite receivers, new generation DVD players, interfaces with storage elements such as computer hard-disks, or the emerging ultra-wide band radio technology. These converters demand high performance to be suitable for the digital telecommunication market, which requires low linearity errors, high speed and low power consumption (battery-powered devices). Low-power performance leads to explore other suitable architectures featuring low-to-moderate resolution in addition to the flash ADC topology. Folding and interpolating techniques are proposed [1-3] as this type of ADC has the advantage of small number of comparators and chip area while the operating speed is the same that of the flash type.

To better explore the design options, and to preliminary evaluate any test approach, it is advisable to perform an analysis at the system behavioural level before starting at transistor level [4]. Behavioural simulators work much faster and it is possible to use the electrical design parameters (gain, bandwidth, offset, parasitic elements) for building the behavioural model; in order to estimate the effects of the injected faults on the specifications of the data converter. In that sense, a system implementation on the MATLAB/SIMULINK environment provides a significant number of advantages.

Traditionally, ADCs are characterized through a specification test, based on a parameter characterization that requires expensive instruments to accurately measure analog signals [5]. To overcome problems related to functional testing, different BIST (Built-in Self Test) techniques have been proposed. They use internally generated or analyzed signals to translate on-chip the methods used in the functional tests [6-9].

The use of structural fault-model testing has been recognized as a promising alternative or addition to specification testing [10]. Some Design-for-Test (DfT) techniques do not attempt to extract the ADC performances to identify the defective circuits, but use a fault model to describe the electrical faulty behavior of a real defect. Therefore the effectiveness of the test technique can be estimated by analyzing the fault coverage figure.

This paper is organized as follows: Section II summarizes the original contributions of this work. Section III briefly describes the architecture of the folded and interpolated ADC used as benchmark circuit, as well as the electrical parameters chosen to build its behavioural model. Section IV presents the proposed structural design-for-test method. Section V describes the fault evaluation performed to check the test goodness on the behavioural model, and also on a transistor level implementation of the ADC. The paper finishes in Section VI with the conclusions.

2 Contribution to Technological Innovation

This work proposes a structural DfT method that monitors some internal test points to extract information about the ADC behaviour. The voltage deviation among these test points is the parameter chosen to infer the presence of a defect in the CUT.

We take advantage of a behavioral description of both the folded and interpolated converter and the design-for-test approach to allow a fast evaluation of the influence of the circuit parameter deviations on the DfT fault coverage and to establish a relationship with the converter performances.

A CAT platform has been used for fault injection and simulation [11], in order to set the optimum threshold voltage that results in maximum fault coverage. The paper is going to be focused in the fault evaluation process of the DfT approach, including a detailed description of the circuit modules necessaries to implement it.

3 Folded and Interpolated A/D Converter and Behavioral Model

The folded and interpolated (FI) A/D converter architecture divides the codification process in two steps performed in parallel: a coarse encoder for the most significant bits and a fine subsystem for the least significant bits [1-3]. It uses an analog pre-processing in the form of a “folding amplifier” (FB) to significantly reduce the number of comparators required to the fine subsystem with regard to a flash ADC.

The block diagram of a 6-bit folded A/D converter implementation is shown in Fig. 1. This circuit uses a resistive reference ladder to obtain 20 voltage references to feed the preamplifier array. A preamplifier block, senses the difference between the

differential input signal *(Vip, Vin)* and a differential threshold *(Vrp, Vrn)* to produce a differential signal that later drives the folder blocks.

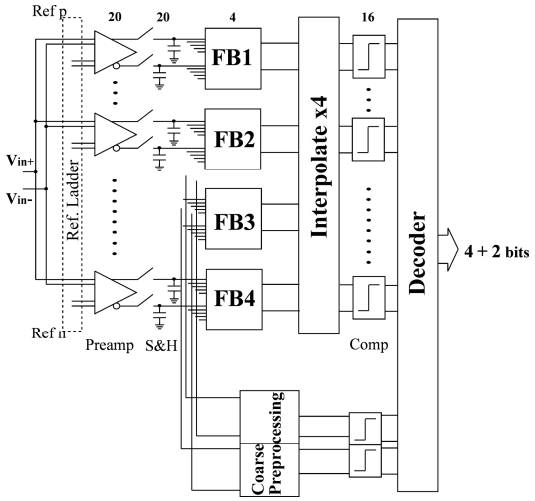

Fig. 1. Block diagram of the folded A/D converter.

The folded A/D converter uses a distributed implementation of the track-and-hold (S&H) function to ease the synchronization between the coarse and fine bits.

The most popular method of producing folding signals involves the use of coupled differential pairs in the folder circuit. A folding degree of 4 was chosen for our application. An interpolation network, usually made of a string of equal resistors, produces additional folding signals without requiring additional folder blocks allowing the reduction of the ADC complexity and power consumption. It also performs an averaging that reduces the offset requirements of the comparators [3].

The analog coarse preprocessing circuit generates analog versions of the two MSBs. Both are generated by means of combination of the output signals of the S&H stages, so folding is not only used in the fine converter but also in the coarse one.

The differential outputs of the interpolation network and the coarse preprocessing block are digitalized by a set of 18 comparators. Then, the decoder uses the cyclic thermometric code provided by the 16 comparators of the fine converter and the 2 bits of the comparators of the coarse block to encode the 6-bit output and to obtain the overflow and underflow signals.

The converter behavior has been modeled by using the MATLAB/SIMULINK environment. The model allows the inclusion of the main sources of distortion in the converter blocks as a set of parameters to take into account the current-voltage relationship between the circuit inputs and outputs.

Table 1 summarizes the MATLAB/SIMULINK models of the converter blocks with their main high level parameters.

Table 1. High-level parameters for the FI ADC blocks.

ADC Block	Parameter
Reference Ladder	Nominal resistance value, Sigma variance
Preamplifier	Transistor transconductance, Bias current
	Load resistor, Bandwidth
Sample and Hold	Gain, Offset, Sampling capacitor
	Switch transistor areas, Jitter
	KT/C Noise, Switch transistor conductances
Folder Block	Transistor transconductance, Bias current
	Load resistor, Bandwidth
Interpolate Network	Nominal resistance value, Sigma variance
Coarse ADC	Transistor transconductance, Bias current
	Load resistor, Bandwidth
Comparator	Offset voltage, Hysteresis
Digital encoder	Redundancy

4 DfT Approach

The proposed method is based on a structural test that provides a digital go/nogo output to be used as interface with a low cost ATE. To diminish the process parameter spread, instead of analyzing the voltage values of the converter internal nodes, we are going to focus on the relative variations that appear among them.

The voltage difference between $\Delta V_1 = [V_{SH}(i) - V_{SH}(i+1)]$ and $\Delta V_2 = [V_{SH}(i+1) - V_{SH}(i+2)]$ is computed by means of a differential difference amplifier (DDA) whose transference function implements (1).

$$\Delta V_{out} = A_{VDDA} \cdot [(V_{SH}(i) - V_{SH}(i+1)) - (V_{SH}(i+1) - V_{SH}(i+2))] \quad (\mathbf{1})$$

Where ΔV_{out} is the output of the DDA, A_{VDDA} is the DDA voltage gain, and $V_{SH}(i)$ are the output voltages, either positive or negative, of the S&H block number "i".

In order to simplify the DfT, the circuit is designed to give zero volts at the DDA output for the fault-free ADC. Thus, any deviation at the DDA output above a voltage limit would indicate the presence of a fault in the ADC. This threshold voltage has to be chosen to accommodate the measurement resolution, noise, temperature and process variations. The comparison of the DDA output with the threshold voltage is done by two differential pair comparators (DPC), to detect both positive and negative increments on ΔV_{out}.

The DDA output only will be zero volts if the transfer function of the three preamplifiers connected to the S&H modules is linear. As it happens for a limited range of the ADC input voltage, the DfT uses two additional comparators to discriminate the opportunity window where the DDA has to be evaluated.

The proposed method uses a five signal test bus to connect to the DfT the three signals sampled by the DDA plus the two additional signals needed by the comparators to establish the sampling window (Fig. 2).

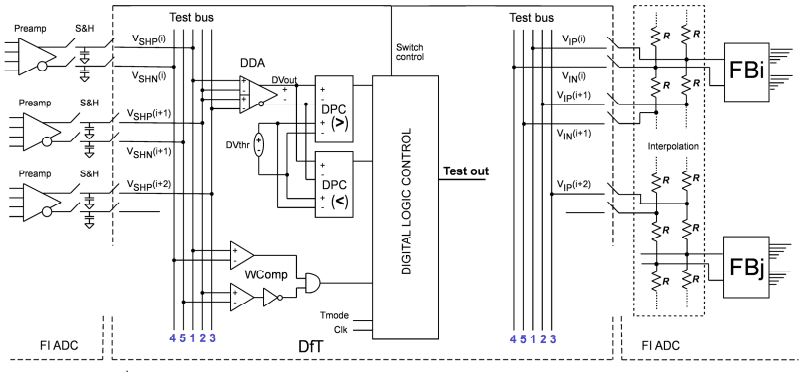

Fig. 2. Simplified scheme of the proposed Design-for-Test structure.

The digital logic control propagates a start pulse using an own test clock. First, it connects the positive outputs of the S&H number 1, 2 and 3 (V_{SHP1}-V_{SHP2}-V_{SHP3}) and wait for the window comparators, connected to the positive and negative outputs of the S&H numbers 1 and 2 (V_{SHP1}-V_{SHN1} and V_{SHP2}-V_{SHN2}), to detect an ADC input voltage that corresponds with the linear range of preamplifiers 1-3. Then, the control circuit allows the DDA output processing by the DPC to detect the presence of a defect in the ADC. If the differential pair comparators are both zero the control circuit provides another test clock pulse to start the second measurement, and the process is repeated until all the S&H modules are evaluated.

After the S&H outputs, the DfT analyses the 16 differential outputs of the interpolated network. Finally, the DfT is connected to the outputs of the coarse preprocessing blocks. In this module, the positive and negative outputs of each amplifier are connected to two DDA inputs; meanwhile, the third input is tied to a reference voltage.

5 Test Evaluation Results

The fault evaluation method consists on injecting faults in one of the modules analyzed by the DfT, meanwhile the remaining ones are considered fault-free. First, the positive outputs of the modules and then the negative ones are processed to obtain the digital outputs of the differential pair comparators *DPC(>)* & *DPC(<)* (Fig. 2).

Fault simulation analysis has been done with a fast ramp and a sinewave input stimulus comprising, both of them, the limits of the ADC full scale. The sinewave input is used for computing the main specifications of the ADC by traditional functional test routines. For the DfT evaluation (fast ramp as input stimulus) only a few codes have been computed during each input transition. One important advantage

of this input vector is that it has no linearity requirements, so it could be easily generated on-chip, to convert the DfT implementation into a full BIST structure.

5.1 Behavioral Model

The fault coverage results from the proposed structural DfT are compared to a functional test based in the estimation of the SINAD degradation. Table 2 summarises this fault coverage comparison. The table shows the deviation in each parameter that induces a degradation of three dBs at the converter SINAD and the deviation of the parameter that provokes a voltage at the differential difference amplifier of 100 mV. Some parameters that do not induce a high enough change in the ADC SINAD or in the DfT voltage are labelled by "----" in Table 2.

Table 2. Fault detection on the ADC building blocks of the behavioral model.

ADC Block	Model Parameter	SINAD	DfT
Reference Ladder	ΔR_{REF}	> 35 %	> 20 %
Preamplifier	ΔR_L	> 20 %	> 5 %
	$\Delta \beta_n$	----	----
	ΔI_{BIAS}	----	> 20 %
	BW	$< 5 \cdot f_{in}$	$< 7 \cdot f_{in}$
Sample & Hold	Aperture Time	> 5 % of TCLK	> 10 % of TCLK
	Jitter	> 2 % of TCLK	> 1 % of TCLK
Folder Block	ΔR_L	> 5 %	> 5 %
	$\Delta \beta_n$	----	----
	ΔI_{BIAS}	> 15 %	> 55 %
	BW	$< 7 \cdot f_{in}$	$< 3 \cdot f_{in}$
Interpolated Network	ΔR_{INTERP}	----	> 300 %
Coarse Preprocessing	ΔR_L	> 75 %	> 10 %
	$\Delta \beta_n$	----	> 200 %
	ΔI_{BIAS}	> 250 %	> 10 %

The SINAD measurement and the DfT circuit detect some faults easily. For instance, deviations of the nominal value of one resistor of the reference ladder and the interpolating network, deviations in the load resistor of the preamplifiers and folder blocks, the reduction of the bandwidth of one of the folder blocks, or jitter in the sample and hold modules. The other two parameters used in the preamplifier behavioural description, transistor β_n and differential pair bias current, I_{Bias}, have a relatively small influence on the converter SINAD because they induce a very small change in the zero crossings of the preamplifier outputs. The DfT can detect deviations on the differential bias current, but not in the transistor β_n because the DfT evaluation is restricted to the CUT linear region.

Table 2 also shows that the DfT tolerance to the aperture time is worse than the SINAD limit, due to all S&H switches being affected by aperture time in the same way, effect that the DfT circuit can not detect easily.

5.2 Transistor Level Implementation

A transistor level implementation of the FI ADC has been developed using the UMC 0.13μm technology. We have injected catastrophic faults into two critical blocks of this circuit (preamplifiers and folder blocks) to evaluate the optimum threshold limit for the DfT that permits to obtain a fault coverage higher than 99%.

The following catastrophic fault model has been used: Three short faults have been included for each transistor. They interconnect the drain, source and gate terminals with different resistance values. The open source and drain faults are placed in series with the two transistor terminals. As far as the open gate faults is concerned, the fault model used forces the transistor to be open, although floating gate voltage would depend on coupling capacitances with adjacent lines, that influence the electrical behaviour of the defective line [12]. Since data from the layout are needed to evaluate coupling capacitances, the simulations of open gate faults are planned to be repeated as future work, once circuit layout is finished.

For fault injection and simulation, we have used the Computer-Aided-Test (CAT) platform [11], integrated in the Cadence Design Framework Environment. It has been developed for the evaluation of test techniques for mixed-signal and RF circuits, and it includes tools for fault simulation, test generation and test optimization.

For the preamplifiers, a total amount of 1,160 catastrophic faults have been simulated (20 times 58 faults per preamplifier), and all of them can be detected by the DfT using a threshold voltage of 100 mV. As far as the open faults is concerned, open drain faults in the differential pair transistors with DC input are more difficult to be detected for the corner preamplifiers (Preamp1 and Preamp20, Fig. 1). In these cases the DfT can detect open faults with an equivalent resistance higher than 40kΩ, whereas, for the rest of open drain and source faults, a threshold voltage of 100 mV is enough to detect faults with an equivalent resistance higher than 10kΩ.

For the folder blocks, 496 catastrophic faults have been simulated (4 times 124 faults per folder block). In this case, all the short and open faults injected in the middle folder blocks (FB2 and FB3, Fig. 1) can be detected using a threshold voltage of 100 mV. For the corner folder blocks (FB1 and FB4, Fig. 1), four DS shorts, four open drain faults, four open source faults and two open gate faults cannot be detected. For these undetectable faults DDA outputs are very close to the 100 mV threshold voltage, thus, probably they could be detected by increasing DDA gain.

In summary, we have obtained an overall fault coverage of 99.15% using a threshold voltage of 100mV. And this fault coverage could even be enhanced, if needed, for the analysis of other ADC blocks, by simply modifying the DDA gain.

5 Conclusions and Further Work

This paper presents a DfT approach for folding and interpolated ADCs. It analyses internal ADC nodes to compare relative deviations among them and, thus, the defects on the CUT can be detected.

A behavioral modeling of the ADC and the DfT has been done in MATLAB/SIMULINK to facilitate the analysis of the proposed test approach.

The detection threshold level to be used by the DfT to considerer a circuit defective is established by means a fault simulation using a CAT platform.

The proposed approach is intended for embedded modules, it also lowers the test time as only a few ADC samples are necessary for the DfT. However as a structural test, it does not provide information about the ADC performances.

As future work, we plan to check the ability of the DfT to detect simulated GOS (Gate Oxide Shorts) and parametric faults in all the ADC blocks, as well as experimentally on a prototype, where it will be necessary to establish the DfT circuit impact on the ADC performance. Finally, it is interesting to study how to complement this test strategy with other methods based on digital or supply current measurements, in order to increase fault coverage by including faults inside the comparators.

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