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Abstract. A CMOS self-biased fully differential amplifier is presented. Due to the self-biasing structure of the amplifier and its associated negative feedback, the amplifier is compensated to achieve low sensitivity to process, supply voltage and temperature (PVT) variations. The output common-mode voltage of the amplifier is adjusted through the same biasing voltages provided by the common-mode feedback (CMFB) circuit. The amplifier core is based on a simple structure that uses two CMOS inverters to amplify the input differential signal. Despite its simple structure, the proposed amplifier is attractive to a wide range of applications, specially those requiring low power and small silicon area. As two examples, a sample-and-hold circuit and a second order multi-bit sigma-delta modulator either employing the proposed amplifier are presented. Besides these application examples, a set of amplifier performance parameters is given.

Keywords: Fully-differential amplifier, inverter-based amplification, low power, self-biasing.

1 Introduction

The complementary fully differential amplifier has a wide range of applications in both the analog and digital domain. This type of amplifier may be used in applications where a wide input signal range is necessary, such as filters, voltage comparators, low voltage differential-signalling (LVDS) systems, and TTL-to-CMOS buffers. Examples of single-ended versions of this type of amplifier have been proposed in [1]. Besides a fully complementary structure, the amplifiers in [1] use a self-biasing method which avoids using separate biasing circuits to bias the amplifier. The advantages of self-biasing techniques are well-known: they simplify the implementation of amplifiers by removing amplifier biasing circuitry, thus saving power and die area; they enable circuits to be insensitive to process, supply voltage, temperature (PVT) and parameter variations; circuits employing these techniques are capable of supplying switching currents greater than the quiescent bias currents [1].

Similar to the amplifiers in [1], a single-ended self-biased amplifier was proposed in [2]. As in all single-ended amplifiers, they suffer from the lack of common-mode (CM) rejection and are highly sensitive to surrounding noisy circuitry. Although die

area is practically doubled, the benefits of fully differential circuits outrun their disadvantages, thus it is always a better option than their single-ended counterpart.

Fully differential self-biased amplifiers have already been proposed, such as, a folded cascode CMOS opamp (with and without gain boosting) [3], a class AB amplifier [4], and an LVDS signal receiver [5]. The amplifier reported in [4] is a pseudo-differential amplifier that relies on a complex active common-mode feedback (CMFB) network which has a separate biasing circuit, thus, is not completely self-biased. The LVDS signal receiver from [5] uses a continuous time CMFB circuit with resistors, thus lowering the achievable gain.

The objective of this brief is to propose a simple CMOS inverter-based self-biased fully differential amplifier with constant DC gain over PVT variations for a wide range of applications. Basically this circuit is a differential version of the amplifier proposed in [1], where self-biasing and output common-mode adjustment is realized through a switched-capacitor (SC) CMFB network.

This paper is organized as follows. Section 2 debates on the contribution of technologic innovation introduced by the proposed circuit. The theory of operation and design analysis of the amplifier is described in Section 3. This section also proposes a design methodology. Application examples in a sample-and-hold amplifier and a sigma-delta ($\Sigma\Delta$) modulator with simulation results are shown in Section 4. The paper is completed with a section dedicated to the conclusions.

2 Contribution to Technological Innovation

It is well-known that circuits employing self-biasing are less sensitive to PVT variations [1]. In fact, these circuits have the advantage of being able to reestablish their nominal operating point after a perturbation in the operation. As a result, the yield of the designed circuits is improved substantially. Also, self-biased circuits do not necessitate dedicated biasing circuitry, and thus power and area are lowered.

Another desired characteristic of a circuit is the capability of being implemented differentially. Fully differential circuits suppress even-order harmonic distortion and are more robust to extrinsic (surrounding) noise. This is a major concern in mixed-signal circuits, where the noise from digital circuitry is coupled into the sensitive analog blocks via the substrate and supply lines. Implementation simplicity (in terms of structure, number of devices, and layout effort) is another issue, since, generally, it leads to circuits consuming less power and area, presenting low noise, and easy to be laid out.

In this work we present a CMOS inverter-based self-biased fully-differential amplifier with the innovation of using a simple SC CMFB circuit to both control the output CM voltage and bias the amplifier. The proposed amplifier accomplishes the above mentioned characteristics and is well suited for a broad range of applications as will be demonstrated.

3 Inverter-Based Self-Biased Fully Differential Amplifier

3.1 Theory of Operation

The proposed amplifier, illustrated in Fig. 1, comprises two input CMOS inverters (M_2, M_3) and two voltage controlled resistors (VCR) M_1 and M_4, biased in the boundary of the saturation and triode regions (it is very difficult to bias both these transistors simultaneously in the saturation region). A simple SC CMFB circuit comprising only two capacitors (C_{CM}) and five switches is used to properly adjust the output common-mode voltage to about $V_{DD}/2$ and, on the other hand, to provide closed-loop control (self-biasing) of the amplifier. The VCRs, M_1 and M_4, have their gate voltages controlled by the output of the SC CMFB circuit, V_{CM}. M_1 and M_4 together with V_{CM} are connected to the input inverters in a negative feedback loop reducing the effect of PVT variations on the amplifier's DC gain. As an example of compensation, if V_{DD} increases, the source-gate voltage in PMOS device M_1, V_{SGP1}, also increases producing an increase in the bias current I_D. This increase will change proportionally the current in the two input inverters, increasing the output CM voltage. As a consequence, the CMFB circuit will produce a higher V_{CM} output control voltage (assuming that V_{CMI} is constant and provided by a bandgap circuit) forcing V_{GSP1} to remain constant, thus compensating the V_{DD} variation. Process and temperature variations have similar compensations through the negative-feedback loop. As will be seen in the following sub-section, the DC gain, A_{V0}, is approximately the ratio of a transconductance by an output conductance, gm/gds. The DC gain is maintained constant because variations in gm (± 30%) are accompanied by similar variations in gds, thus their ratio has variations less than 7 % over PVT variations.

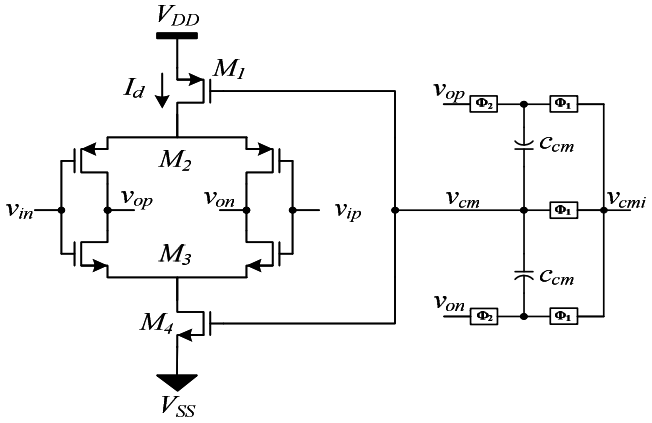

Fig. 1. Schematic of the fully-differential single-stage self-biased amplifier with the SC CMFB circuit.

3.2 Design Analysis

Performing a small signal analysis followed by a Y-parameter simplification of the amplifier it is possible to obtain the amplifier's transfer function, given by,

$$A_V \cong \frac{s\cdot(cgd_2+cgd_3)-gm_3-gm_2}{s\cdot(cgd_2+cgd_3+C_L+C_{CM})+gds_2+gds_3} \quad (\mathbf{1})$$

Equation (2) presents the amplifier's DC gain. Some assumptions have been made, namely, $gm_3 \cong k{\cdot}gm_2 = k{\cdot}gm$ ($k = \mu_N/\mu_P$), $b_{ef2} \cong b_{ef3} = b_{ef}$ ($b_{ef} \cong 0.85$) and $gds_2 \cong gds_3 = gds$. μ_N and μ_P represent the mobilities of the NMOS and PMOS transistors, respectively. b_{ef} represents the gm degradation in devices M_2 and M_3 due to body-effect. Special care should be taken when considering a value for b_{ef}, as it may vary with the operating region of each transistor.

$$A_{V0} \cong \frac{b_{ef}\cdot gm\cdot(1+k)}{2\cdot gds} \quad (\mathbf{2})$$

It should be noticed that (1) represents the gain of a standard inverter input amplifier, in other words, no parameters of devices M_1 and M_4 appear in the transfer function.

From (1) it is also possible to obtain expressions for the dominant pole frequency (BW), gain-bandwidth product (GBW), and the unity gain frequency (UGF), which are important performance parameters in opamp circuits. The following equations respectively represent the mentioned performance parameters. Parasitic capacitor $cgd = cgd_2 = cgd_3$ and C_L represents the output load capacitance.

$$f_{pole} = BW = \frac{2\cdot gds}{C_L+C_{CM}+2\cdot cgd} \quad (\mathbf{3})$$

$$GBW = A_{V0}\times BW = \frac{b_{ef}\cdot gm\cdot(1+k)}{C_L+C_{CM}+2\cdot cgd} \quad (\mathbf{4})$$

$$UGF = \frac{b_{ef}\cdot gm\cdot(1+k)-2\cdot gds}{C_L+C_{CM}} \quad (\mathbf{5})$$

By considering the DC gain and GBW as initial specifications for the opamp, a possible design procedure would be to use (4) to obtain the gm that satisfies the GBW for a given effective load ($C_{eff} = C_L + C_{CM} + 2cgd$), and then to employ (2) to find the gds that satisfies the A_{V0} requirement. The drain currents for M_2 and M_3 can be calculated using gm and a given drain-source saturation voltage, $V_{DSsat} = V_{GS} - V_T \geq$ 100 mV. Finally, M_2 and M_3 should be sized to be in saturation and to have an adequate gds (adjusted by the channel lengths). Multiplying the drain current of M_2 (or M_3) by two (to account for both current paths, differential circuit) it is possible to size M_1 and M_4 in the triode/saturation boundary region for a $V_{DSsat} \geq 100$ mV ($V_{DSsat1,4}$ should not be large to avoid degrading output swing). Some care should be taken in the sizing of the transistors to guarantee the desired output common-mode voltage, power budget, output swing and PVT and mismatch insensitivity.

4 Simulation Results

This section presents simulation results of the proposed amplifier for two target applications. Firstly, the amplifier is applied in a sample-and-hold amplifier (SHA) intended for the front-end stage of a low resolution, high speed pipelined analog-to-digital converter (ADC). Secondly, the proposed amplifier is used in a multi-bit ΣΔ modulator targeted at hearing aid devices. Both amplifiers were designed in a 130 nm high speed 1.2 V CMOS technology (L_{min} = 120 nm). The mobility and threshold parameters (Level 2), K_N, K_P, V_{TN} and V_{TP} of the devices are, respectively, 525 μAV^{-2}, 145 μAV^{-2}, 0.38 V and -0.33 V. For V_{cmi}, 550 mV was used.

4.1 Application in a Sample-and-Hold Amplifier

An interesting application for the proposed amplifier is in a SHA as depicted in Fig. 2. This SHA was successfully applied in the front-end stage of a low resolution (7 bit) and high speed (500 MS/s) pipelined ADC. As a result, the basic specifications of the amplifier, such as DC gain (A_{V0}) and GBW, should be large enough to accommodate these requirements. Furthermore, the power consumption must be kept as low as possible to avoid degradation in the ADC performance.

With these prerequisites in mind and by using the proposed design procedure as an initial step followed by electrical simulations for sizing refinements (this includes typical and, at least, process corners), the transistors are sized as reported in Table 1.

Table 1. Feature size of the transistors for the sample-and-hold amplifier.

Transistor	W (μm) / L (μm)
M_1	47 / 0.18
M_2	32 / 0.16
M_3	32 / 0.16
M_4	32 / 0.50

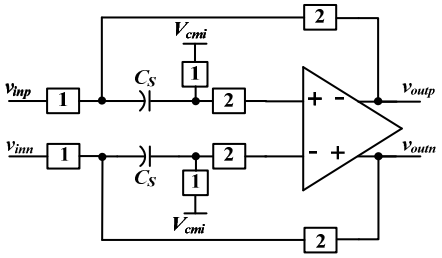

Fig. 2. Complete electrical schematic of the sample-and-hold amplifier.

To evaluate the overall performance and robustness of the designed amplifier, its key parameters are simulated for different PVT corners according to Table 2. At typical conditions (Ct), the amplifier dissipates 0.9 mW and achieves a DC gain of 25.8 dB with a GBW larger than 2.88 GHz (for an effective load capacitance of 0.5 fF). The results for the other PVT corners are shown in Fig. 3. It should be noted that, although the GBW and the static power vary considerably, the DC gain varies less than ±0.75 dB considering all corners. These results were expected and clearly

indicate the contribution of self-biasing in reducing amplifier sensitivity to PVT variations, concerning the DC gain.

Table 2. List of PVT corners used in the electrical simulations.

Corner	Process	Supply Voltage	Temperature
Ct	TT	1.2	27
C1	TT	1.14	27
C2	TT	1.26	27
C3	SS	1.14	-40
C4	SS	1.14	85
C5	SS	1.26	-40
C6	SS	1.26	85
C7	FF	1.14	-40
C8	FF	1.14	85
C9	FF	1.26	-40
C10	FF	1.26	85

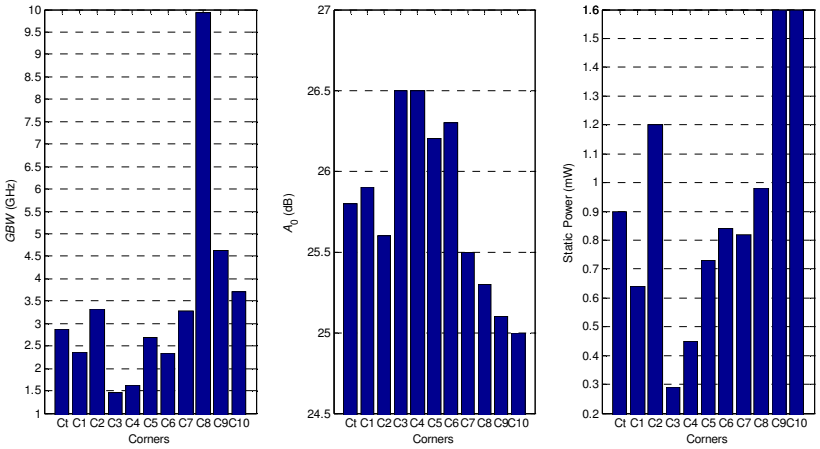

Fig. 3. GBW, A_0, and static power of the amplifier for PVT corners listed in Table 2.

4.2 Application in a Multi-Bit Sigma-Delta Modulator

The proposed amplifier was also applied to a second-order four-bit ΣΔ modulator as shown in Fig. 4. In this context, the amplifier is employed to realize a low power SC integrator, which is one of the key elements that determine the global performance of the ΣΔ modulator. This modulator is intended for hearing aids, and, therefore, it requires a dynamic range of about 96 dB with a peak signal-to-(noise plus distortion) ratio (SNDR) above 60 dB. Additionally, the signal bandwidth is 20 kHz. These specifications are met using a second-order four-bit ΣΔ modulator with nonlinear digital-to-analog converters with an oversampling ratio of 32.

The most stringent requirements are needed in the first integrator, which results in a higher complex amplifier design than necessary for the second integrator. It was verified by high level simulations that a minimum DC gain of 40 dB in the amplifier of the first integrator is enough to achieve the target dynamic range of 96 dB. In

addition, the amplifier needs to settle its output with an error lower than 10 bit of resolution required for 60 dB of SNDR when operated at 1.28 MHz sampling frequency. This is achieved with a GBW higher than 8.4 MHz. To meet all these specifications the amplifier is sized following the same procedure described earlier and the results are shown in Table 3.

Table 3. Feature size of the transistors for the amplifier of the first integrator.

Transistor	W (μm) / L (μm)
M_1	8.5 / 1.2
M_2	15 / 0.8
M_3	16 / 1.3
M_4	7.75 / 4.5

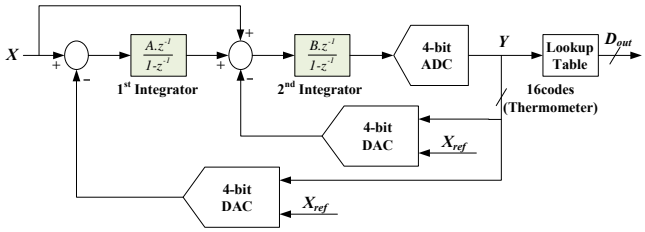

Fig. 4. Complete block diagram of the second-order four-bit ΣΔ modulator.

The performance of the amplifier was verified through different PVT corners simulations as indicated in Table 2. The amplifier achieves a DC gain of 42.9 dB with a GBW larger than 8.4 MHz (for an effective load capacitance of 10 pF) dissipating only 41 μW at typical operation. The results for the remaining corners are depicted in Fig. 5. As in the previous example, we can note that the DC gain varies less than ±1.5 dB considering all corners.

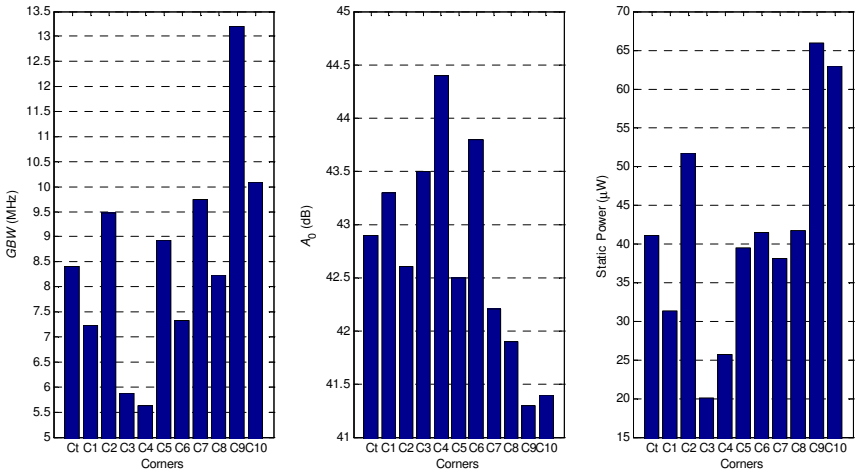

Fig. 5. GBW, A_0, and static power of the amplifier for PVT corners listed in Table 2.

5 Conclusions

A CMOS self-biased fully differential amplifier was presented. In order to generate the biasing voltages of the amplifier, a CMFB is employed. The CMFB circuit, based on an SC network, uses the amplifier's outputs to derive the mentioned voltages, hence the designation, self-biased amplifier. Due to the self-biasing structure of the amplifier and its associated negative feedback, the amplifier is compensated to achieve low sensitivity to PVT variations. The output common-mode voltage of the amplifier is adjusted through the same biasing voltages provided by the CMFB circuit. The amplifier core is based on a simple structure that uses two CMOS inverters to amplify the input differential signal. Despite its simple structure, the proposed amplifier is attractive to a wide range of applications, specially those requiring low power and small area. As two examples, a second order ΣΔ modulator and a SHA circuit either employing the proposed amplifier were presented. Besides these application examples, a set of amplifier performance parameters was given.

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