Sliding Mode Control of Unified Power Quality Conditioner for 3 Phase 4 Wire Systems

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Abstract. This paper presents the sliding mode control (SMC) of unified power quality conditioners (UPQC) intended to compensate power quality issues in three-phase four-wires systems. The SMC UPQC can be applied in electrical grids or isolated grids to mitigate power quality problems at the consumer facilities and also to minimize issues for the grid supplier. The UPQC is configured as a shunt-series filter. The shunt Active Power Filter (APF) uses a three-phase rectifier with SMC to enforce sinusoidal mains currents. The series APF uses three single-phase H-bridge inverters and SMC to improve the voltage quality at the point of common coupling. SMC design, analysis and simulation results are presented and discussed.

Keywords: Unified Power Quality Conditioner; Active Power Filter; Sliding Mode Control.

1 Introduction

In recent years, economic and environmental reasons entail the best possible use of energy resources. Recent technological developments enabled better usage of energy resources, mainly alternative energies [1]. However, due to the usually relatively low duty-cycle and randomness of these energies, their interconnection to the electrical grid might require the use of power electronics systems, and power quality mitigating devices, such APF, to increasing power quality [2], according to the standards recommended maximum power quality disturbances (IEEE 519, IEC 50160).

Most common power quality issues arise in the distribution grids, including voltage variations, harmonics, voltage sags and swells, voltage unbalances, harmonic currents, high reactive power burden and excessive neutral wire current. APFs can solve voltage and current waveform issues, reducing harmonics in a wide frequency band without resonance problems [3].

2 Contribution to Collective Awareness Systems

This paper proposes a UPQC system with the ability to increase the quality of distribution of electrical power to achieve better efficiency. It proposes a contribution towards the sustainability of global systems considering the economic aspect and the environmental, reaching an important advance in the sustainable growth systems while benefiting from future collective awareness system to take informed decisions, making effective the involvement of the customer and sustainable energy systems.

3 UPQC Topology

Conventional UPQC have two basic configurations [3]. The most common is the series-shunt which injects the voltage compensation at the source side and the current compensation at the load side. This configuration has the advantage of the current flowing through the series transformer containing only the fundamental frequency. The shunt-series UPQC injects currents at the source side and compensates voltage at the load side. This configuration has the advantage of avoiding the interference between the shunt inverter and the passive filters, caused by the high frequency switching of the UPQC [3].

This paper presents the study of a shunt-series configuration provided with a passive LC filter on the series side as depicted in Fig. 1.

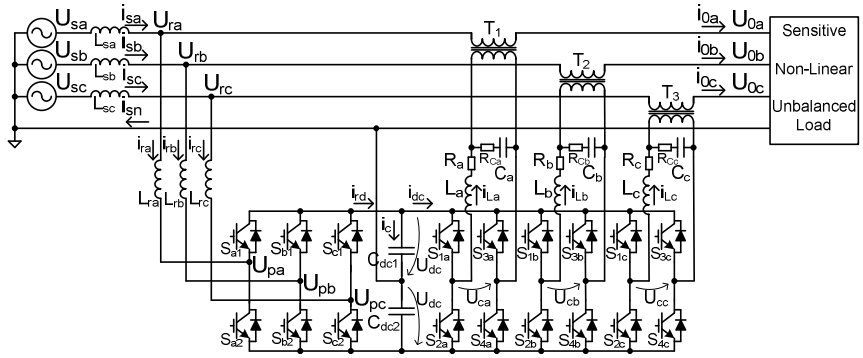

Fig. 1. Shunt-Series UPQC.

To compensate the neutral current a split capacitor topology (C_{dc1}, C_{dc2}), with the midpoint connected to the neutral wire, enables return currents through the capacitors, being $i_{sa} + i_{sb} + i_{sc} = i_{sn}$. The return of the neutral current through the DC bus capacitors unbalances the voltage of the two capacitors and decreases the dynamic response of the shunt APF. To minimize this problem, an extra control system to equalize the voltage on the two capacitors is usually included [3], even for small neutral currents, with zero average values, flowing into the source due the high switching harmonics.

3 Control

3.1 Shunt APF

The shunt APF must enforce sinusoidal i_{sa}, i_{sb} and i_{sc} currents in the mains source, [4]. Additionally, the shunt APF must stabilize the DC bus voltage [3].

Sliding Mode Internal Current Control. The shunt APF injects the necessary currents to cancel unwanted harmonics produced by non-linear and unbalanced loads. A SMC technique is used to control the mains current. Considered one generic single phase k of the corresponding source, as represented in Fig. 1. Assuming ideal switches and ideal components, the dynamics of the i_{sk} current $k \in \{a, b, c\}$ can be described considering that the voltage U_{pk}, relative to the neutral voltage, is dependent on the switches states of the shunt inverter semiconductors, as in (1).

$$U_{pk} = \delta(t)U_{dc} = \begin{cases} U_{pk} = U_{dc} \ \text{ for } \delta(t) = +1 \ (S_{k1} \ ON \ and \ S_{k2} \ \ OFF) \\ U_{pk} = -U_{dc} \ \text{for } \delta(t) = -1 \ (S_{k1} \ OFF \ and \ S_{k2} \ \ ON) \end{cases} \quad (\mathbf{1})$$

The first time derivative of the i_{rk} current is given as $\frac{di_{rk}}{dt} = \frac{U_{rk} - \delta(t)U_{dc}}{L_{rk}}$ considering that $i_{sk} = i_{rk} + i_{0k}$, and $\frac{di_{sk}}{dt} = \frac{di_{rk}}{dt} + \frac{di_{0k}}{dt}$, then, the phase canonical model of current i_{sk} is written as (2).

$$\frac{di_{sk}}{dt} = \frac{U_{rk}}{L_{rk}} - \frac{\delta(t)U_{dc}}{L_{rk}} + \frac{di_{0k}}{dt} \quad (\mathbf{2})$$

The first time derivative of i_{sk} contains the control action $\delta(t)U_{dc}$, thus the strong relative degree [5] of i_{sk} is 1, and a suitable sliding surface can be obtained as a linear combination of the control error $e_{i_{sk}} = i_{sk}^{ref} - i_{sk}$r, where i_{sk}^{ref} is the reference value to be tracked by the i_{sk} current. Considering a positive gain K_p, used to limit the semiconductors switching frequency, a suitable sliding surface $S(ei_{sk}, t)$ [5] is:

$$S\left(e_{i_{sk}}, t\right) = K_p \, e_{i_{sk}} = K_p\left(i_{sk}^{ref} - i_{sk}\right) = 0 \quad (\mathbf{3})$$

The switching strategy is obtained applying the sliding mode stability condition $S\left(e_{i_{sk}}, t\right) \dot{S}\left(e_{i_{sk}}, t\right) < 0$ [6], with $\dot{S}\left(e_{i_{sk}}, t\right) = K_p\left(\frac{di_{sk}^{ref}}{dt} - \frac{U_{rk}}{L_{rk}} + \frac{\delta(t)U_{dc}}{L_{rk}} - \frac{di_{0k}}{dt}\right)$. As $S\left(e_{i_{sk}}, t\right)$ is proportional to $e_{i_{sk}}$, the stability condition is written as:

$$\begin{cases} \text{if } e_{i_{sk}} > 0, \quad \text{then } \frac{de_{i_{sk}}}{dt} < 0 \Rightarrow \frac{di_{sk}^{ref}}{dt} - \frac{U_{rk}}{L_{rk}} + \frac{\delta(t)U_{dc}}{L_{rk}} - \frac{di_{0k}}{dt} < 0 \\ \text{if } e_{i_{sk}} < 0, \quad \text{then } \frac{de_{i_{sk}}}{dt} > 0 \Rightarrow \frac{di_{sk}^{ref}}{dt} - \frac{U_{rk}}{L_{rk}} + \frac{\delta(t)U_{dc}}{L_{rk}} - \frac{di_{0k}}{dt} > 0 \end{cases} \quad (\mathbf{4})$$

From (4), the sliding mode reaching condition can be obtained as $\frac{\delta(t)U_{dc}}{L_{rk}} > \text{MAX}\left(-\frac{di_{sk}^{ref}}{dt} + \frac{U_{rk}}{L_{rk}} + \frac{di_{0k}}{dt}\right)$. Supposing that U_{dc} is high enough to satisfy this reaching condition and if $e_{i_{sk}} > 0$ then $\frac{de_{i_{sk}}}{dt} < 0$ the control action is $\delta(t) = -1$ or if $e_{i_{sk}} < 0$

then $\frac{de_{i_{sk}}}{dt} > 0$ the control action is $\delta(t) = 1$. To define a finite switching frequency, the i_{sk} current must have a non-zero ripple content Δi_{sk}. The switching law is then:

$$\delta(t) = \begin{cases} -1 \text{ for } S(e_{i_{sk}}, t) > +\Delta i_{sk}/2 \\ 1 \text{ for } S(e_{i_{sk}}, t) < -\Delta i_{sk}/2 \end{cases} \quad (5)$$

The sliding surface (3) and the non-linear switching law (5) do not depend on any load parameter, but only on the measured i_{sk} current error $e_{i_{sk}}$. To generate the sinusoidal and balanced i_{sk}^{ref} current references in the *abc* frame the inverse Park Transform (*dq0* to *abc*), is used where i_d, i_q and i_0 are the direct, quadrature and zero sequence component of the current reference. The i_{sk}^{ref} current references in *dq0* (i_d, i_q and i_0) will be obtained using a slow enough linear controller to minimize current total harmonic distortion (THD). The response time should be tailored to avoid DC bus voltage dropouts in the case where fast increments of load currents are required, which can affect the global dynamic of series APF.

Linear External DC Bus Voltage Control. The external loop to regulate the voltage in the DC bus capacitors uses a PI controller, $C_{v(s)} = \frac{1+sT_z}{sT_p}$, designed to present small load sensitivity. The PI output is the reference for the current i_d component of Park Transform [7], while the i_q and i_0 components of Park Transform are set to zero to have near unity power factor ($v_q = 0$) and to balance the three phases. The previously designed sliding mode internal current control closed loop behavior is modelled by a first order system represented as $\frac{i_{rk}}{i_{sk}^{ref}} = \frac{k_e}{T_d s+1}$ where $k_e = \frac{U_{sd}}{2U_{dc}}$ and T_d is estimated knowing that line currents should be sinusoidal to avoid line current distortion. The PI parameters T_z and T_p of the voltage controller $C_v(s)$ are calculated using the Symmetrical Optimum technique, [8]. Assuming $U_d = 2U_{dc}$ and $C = C_{dc1}/2 = C_{dc2}/2$, the differential equation of the DC bus voltage is $\frac{dU_d}{dt} = \frac{i_{rd}-i_{dc}}{C}$. Applying superposition with zero disturbances and supposing $\alpha_v = 1$ (sensor voltage gain), the closed-loop transfer function of the DC bus voltage control has a third order polynomial denominator, $\frac{U_d}{U_d^{ref}} = \frac{1+sT_z}{s^3\frac{T_p T_d C}{k_e}+s^2\frac{T_p C}{k_e}+sT_z+1}$, represented in (Fig. 2).

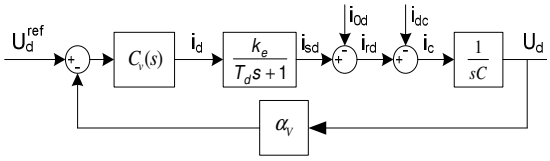

Fig. 2. DC bus voltage control.

Applying Symmetrical Optimum criteria $b_k^2 = 2b_{k-1}b_{k+1}$, to ensure a low enough sensitivity to the UPQC disturbances. The value T_d=4ms was used to obtain the T_z and T_p, so that line currents are almost sinusoidal and DC bus voltage response is fast

enough to avoid affecting the series APF performance [5]. The PI parameters are $T_z = 4T_d$ and $T_p = \frac{8T_d^2 k_e}{C}$.

3.2 Series APF

To compensate the voltage distortion, the three series transformer primaries are driven using three single-phase H-bridge inverters (Fig. 1) controlled using SMC. Considering the per-phase equivalent of the series APF, with $k \in \{a, b, c\}$, where the C_k is the filter capacitor and the load is reduced to the transformer primary.

The U_{ck} output voltage depends on the switches states S_{1k}, S_{2k}, S_{3k} and S_{4k}.

$$U_{ck} = \gamma_c(t)U_d = \begin{cases} U_{ck} = U_d & \text{for } \gamma_c(t) = +1 \quad (S_{1k},\ S_{4k}\ ON) \\ U_{ck} = 0 & \text{for } \gamma_c(t) = 0\ (S_{1k},\ S_{3k}\ ON\ or\ S_{2k},\ S_{4k}\ ON) \\ U_{ck} = -U_d & \text{for } \gamma_c(t) = -\ \ (S_{2k},\ S_{3k}\ ON) \end{cases} \quad (6)$$

Assuming ideal components, the dynamic model with state variables u_{0k} and i_{Lk} is written as (7), were i_{0k} is the load current:

$$\frac{d}{dt}\begin{bmatrix} u_{0k} \\ i_{Lk} \end{bmatrix} = \begin{bmatrix} 0 & 1/C_k \\ -1/L_k & -R_k/L_k \end{bmatrix}\begin{bmatrix} u_{0k} \\ i_{Lk} \end{bmatrix} + \begin{bmatrix} -1/C_k & 0 \\ 0 & 1/L_k \end{bmatrix}\begin{bmatrix} i_{0k} \\ \delta_c(t)U_d \end{bmatrix} \quad (7)$$

The proposed of the series APF is compensate the voltage at the load side. According to [5], [6] and [9], to control the load voltage u_{0k} is necessary to obtain a equation which includes the dynamic of switching. The first order derivative of u_{0k} doesn't include the switch condition $\delta_c(t)$, for this reason we need to calculate the second order derivative for the u_{0k} . Thus, the strong relative degree of u_{0k} is 2 written as $\frac{d^2u_{0k}}{dt^2} = -\frac{1}{C_k}\frac{di_{0k}}{dt} - \frac{u_{0k}}{L_kC_k} - \frac{R_k i_{Lk}}{L_kC_k} + \frac{\delta_c(t)U_d}{L_kC_k}$.

The robust sliding surface (8) is a linear combination of the control error $e_{u_{0k}}$ and its derivative, $e_{u_{0k}} = u_{0k}^{ref} - u_{0k}$, where u_{0k}^{ref} is the voltage reference to be tracked and u_{0k} the voltage feedback.

$$S(e_{u_{0k}}, t) = k_1 e_{u_{0k}} + k_2 \frac{de_{u_{0k}}}{dt} = 0 \quad (8)$$

The system response depends on the coefficients k_1 and k_2 which must be selected to ensure stability and fast response for operating conditions. Considering $\beta = k_2/k_1$ the sliding surface is written as:

$$S(e_{u_{0k}}, t) = \frac{C_k}{\beta}(u_{0k}^{ref} - u_{0k}) + C_k \frac{du_{0k}^{ref}}{dt} + i_{0k} - i_{Lk} = 0 \quad (9)$$

The switching strategy is obtained applying the sliding mode stability condition $S(e_{u_{0k}}, t)\,\dot{S}(e_{u_{0k}}, t) < 0$, with $\dot{S}(e_{u_{0k}}, t) = \frac{i_{Lk}}{C_k} - \frac{i_{0k}}{C_k} + \beta\left(\frac{1}{C_k}\frac{di_{0k}}{dt} + \frac{u_{0k}}{L_kC_k} + \frac{R_k i_{Lk}}{L_kC_k} - \frac{\delta_c(t)U_d}{L_kC_k}\right)$. As $S(e_{u_{0k}}, t)$ is proportional to $e_{u_{0k}}$, the stability condition is written as:

$$\begin{cases} \text{if } e_{u_{0k}} > 0, & \text{then } \dfrac{de_{u_{0k}}}{dt} < 0 \Rightarrow \dfrac{i_{Lk}}{C_k} - \dfrac{i_{0k}}{C_k} + \beta\left(\dfrac{1}{C_k}\dfrac{di_{0k}}{dt} + \dfrac{u_{0k}}{L_kC_k} + \dfrac{R_k i_{Lk}}{L_kC_k} - \dfrac{\delta_c(t)U_d}{L_kC_k}\right) < 0 \\ \text{if } e_{u_{0k}} < 0, & \text{then } \dfrac{de_{u_{0k}}}{dt} > 0 \Rightarrow \dfrac{i_{Lk}}{C_k} - \dfrac{i_{0k}}{C_k} + \beta\left(\dfrac{1}{C_k}\dfrac{di_{0k}}{dt} + \dfrac{u_{0k}}{L_kC_k} + \dfrac{R_k i_{Lk}}{L_kC_k} - \dfrac{\delta_c(t)U_d}{L_kC_k}\right) > 0 \end{cases} \quad (\mathbf{10})$$

From (10), the sliding mode reaching condition is $\beta\frac{\delta_c(t)U_d}{L_kC_k} > \text{MAX}\left(\frac{i_{Lk}}{C_k} - \frac{i_{0k}}{C_k} + \right.$ $\left. +\beta\left(\frac{1}{C_k}\frac{di_{0k}}{dt} + \frac{u_{0k}}{L_kC_k} + \frac{R_k i_{Lk}}{L_kC_k}\right)\right)$. Supposing that U_d is high enough to satisfy this reaching condition and using a hysteresis comparator, with Δu_{0k} as hysteresis, to avoid infinite switching frequency, the switching law is (11), being $\delta_c(t) \in \{-1;\ 0;\ 1\}$ to obtain three possible U_{ck} levels.

$$\begin{cases} \text{if } \ e_{u_{0k}} > \dfrac{\Delta u_{0k}}{2}, & \text{then } \dfrac{de_{u_{0k}}}{dt} < 0 \Rightarrow \delta_c(t) = 1 \\ \text{if } \dfrac{-\Delta u_{0k}}{2} < eu_{0k} < \dfrac{\Delta u_{0k}}{2}, & \text{then } \delta_c(t) = 0 \\ \text{if } \ e_{u_{0k}} < \dfrac{-\Delta u_{0k}}{2}, & \text{then } \dfrac{de_{u_{0k}}}{dt} > 0 \Rightarrow \delta_c(t) = -1 \end{cases} \quad (\mathbf{11})$$

This technique samples u_0, i_0 and i_L, but the closed loop dynamics does not depend on load parameters. Fast response with zero steady-state errors are also attained [10].

4 Simulation

The UPQC was simulated using Matlab/Simulink considering non-ideal mains voltage with 5% THD. Several loads, described in the Appendix, were tested.

To evaluate the UPQC response with wide operating conditions, different loads and conditions were tested successively. The test begins with a balanced R load. Then, an unbalanced RL load is switched on to add to the existing balanced R load. In a third step it is added a non linear load, made by three single-phase bridge rectifiers, with upstream inductance L and parallel RC type circuit downstream of the bridge. In the fourth step a voltage sag in the main source appears, being cleared in the fifth step.

The first simulation (Fig. 5) is performed without any compensation. High neutral current exists due to the switching on of unbalanced and non-linear loads. The load voltage has a THD of 5.4%. The THD of currents reach a maximum of 25,1% in the worse case.

Using the compensating UPQC, the delivered voltage (Fig. 6) has a maximum THD of 0.6%, and currents drops to a maximum THD of 2.37%. The UPQC clearly improves the quality power to the main source (current) and to the load side (voltage). The neutral current is mostly zero throughout the simulation (except for switching harmonics and switch on transients).

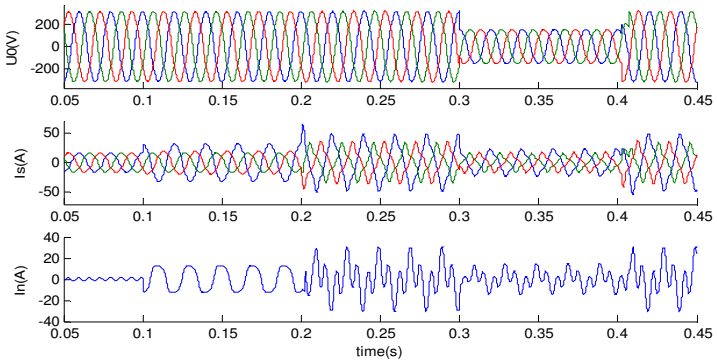

Fig. 5. Results under unbalanced and distorted voltage source with non-linear loads without compensation.

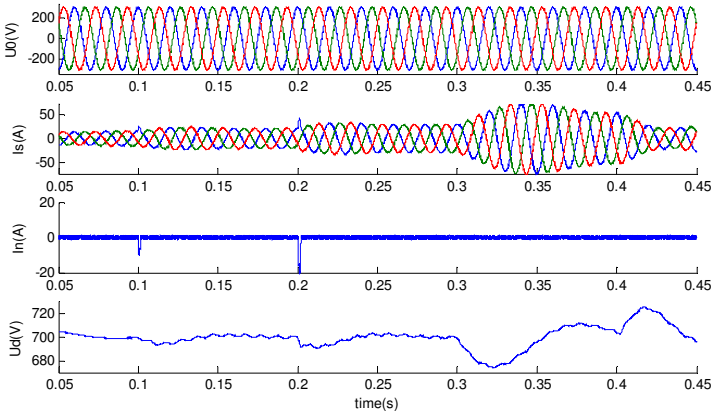

Fig. 6. Results under unbalanced and distorted voltage source with non-linear loads with compensation.

5 Conclusion

This study demonstrates the sliding mode control of UPQC to improve power quality on three-phase four-wire systems. The UPQC can mitigate the harmonic content of voltage at the load side (88% reduction), and the harmonic current at the source side (90% reduction), while virtually eliminating the neutral current and improving the power factor. The measured values of the harmonic distortion of current source and the voltage delivered to the load were well within the recommended values according to standards IEEE-519 or IEC61000.

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Appendix

The UPQC parameters are presented in Tab. 1.

Table 1. System Parameters

Parameter	Value	Parameter	Value	Parameter	Value	Parameter	Value
U_{sk}	$230V_{ef}$	L_r	1mH	1ºst - R_{abc}	20Ω	3ºst - L_{NL}	8.4mH
R_s	10mΩ	C_k	112μF	2ºst - L_{abc}	5mH	3ºst - C_{NL}	1000μF
L_s	0.1mH	L_k	0,9mH	2ºst – R_{0a}	R_{abc}	3ºst - R_{NL}	50Ω
U_d	700V	R_{Ck}	15Ω	2ºst – R_{0b}	$50R_{abc}$	4ºst - R_{sag}	R_s
C_{dc}	5mF	U_{ref}	$230V_{ef}$	2ºst - R_{0c}	$5R_{abc}$	4ºst - L_{sag}	L_s

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