# A Top-Down Optimization Methodology for SC Filter Circuit Design Using Varying Goal Specifications

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Centre for Technologies and Systems (CTS) – UNINOVA
Dept. of Electrical Engineering (DEE), Universidade Nova de Lisboa (UNL)
2829-516 Caparica, Portugal
has14926@campus.fct.unl.pt, {rmt, nunop}@uninova.pt

**Abstract.** The design of Switched-Capacitor (SC) filters can be an arduous process, which becomes even more complex when the high gain amplifier is replaced by a low gain amplifier or a voltage follower. This eliminates the virtual ground node, requiring the compensation of the parasitic capacitances during the design phase. This paper proposes an automatic procedure for the design of SC filters using low gain amplifiers, based on a Genetic Algorithm (GA) using hybrid cost functions with varying goal specifications. The cost function first uses equations to estimate the filter transfer function, the gain and settling-time of the amplifier and the RC time constants of the switches. This reduces the computation time, thus allowing the use of large populations to cover the entire design space. Once all specifications are met, the GA uses transient electrical simulations of the circuit in the cost functions, resulting in the accurate determination of the filter's transfer function and allowing the accurate compensation of the parasitic capacitances, obtaining the final design solution within a reasonable computation time.

**Keywords:** Computer-aided design, genetic algorithm, filter design, switched-capacitor.

## 1 Introduction

Analog filters are very important blocks in several electronic systems such as RF transceivers or sigma delta modulators. They allow selecting signals with different frequencies and eliminating unwanted signals.

The scaling-down of transistors in advanced deep-submicron CMOS technologies results in the reduction of the intrinsic gain ($g_m/g_{ds}$) [1] and increases the variability, making the design of high gain high bandwidth opamps increasingly difficult. This limitation has large impact in the performance of filter circuits.

To avoid the difficulty of designing high gain amplifiers, SC filters can be implemented using low gain amplifiers [2]. However, this approach removes the circuit's virtual ground node. Without this node, parasitic insensitive SC branches cannot be used and the filter's transfer function becomes sensitive to the effects of parasitic s, which have to be compensated during the design phase of the filter.

This paper presents an automatic procedure for the compensation of the parasitic capacitances introduced by parasitic sensitive branches and a general design methodology for the design of SC filters, using low gain amplifiers, based on a GA

using hybrid cost functions with varying goal specifications. The exact transfer function of a SC filter can be obtained by simulating the circuit's impulse response. This, however, results in a large computation time that limits the maximum size of the population of the GA. An alternative is to estimate the filter's transfer function using equations, resulting in a low computation effort and allowing the evaluation of a larger population in a reasonable time. This approach allows the design space of the filter to be completely explored. Once a solution is found, it is then possible to reduce the population size in the GA, obtaining the final design solution using the more computation intensive and more accurate simulation based cost functions. During this step, the optimization will also calculate the final values of the capacitances taking into consideration the parasitic capacitance values. This hybrid cost function (equation based/simulation based) allows a larger design space to be explored and obtaining a design solution with a good accuracy, while still having a low computation time.

## 2 Relationship to Collective Awareness Systems

Collective awareness systems are information and communication technology systems that allow the interaction of people, knowledge, and objects through a network. The development of these systems, which require faster, smaller, and less power consuming circuits, while performing more complex operations, is only possible using advanced nanometer CMOS technologies. Filter circuits are essential blocks in front-end transceivers that allow the data collection and also support the communication between the agents involved in a network. This paper describes a top-down optimization methodology for the design of SC filter's using low gain amplifiers. Using this optimization methodology, it is possible to quickly study new SC filters in order to find new topologies capable of addressing the more demanding specifications required for collective awareness systems.

## 3 Proposed Design Methodology

A software add-on was developed to implement the proposed methodology. This add-on was integrated into an existing optimization software platform [3], [4], [5], based on the open-source circuit simulator, Ngspice [6]. Initially, a population consisting of N randomly created chromosomes is generated based on the maximum and minimum allowed values of each component, which defines the design space. The fitness of each chromosome is then calculated, based on the desired specifications, and sorted. A new population is created based on the genetic material of the best chromosomes and complemented with selection, cross-over and mutation operations among the remaining chromosomes. This process is repeated during a number of generations or until the desired specifications are met. The fitness is calculated using the exponential-based equations presented in [7].

The methodology uses a multi-step approach to obtain the optimized filter design. In the first step, the SC filter is optimized from an ideal standpoint using the equation

that describes its transfer function. Once the desired specifications for the filter are met, the second step starts, where the tool focuses on optimizing the amplifier circuit at transistor level, in order to have enough gain and closed-loop bandwidth to replace the ideal gain obtained from the top-level optimization. After this step, it is necessary to compensate the effects of the amplifier's input and input to output parasitic capacitances in the SC filter. In the third step, the switches are optimized in order to have a RC time constant that is small enough to charge the capacitors in half the clock period. When these specifications are met the parasitic capacitances of the switches are compensated through a transient simulation, in Ngspice, to determine the fitness of each SC circuit at transistor level. During this step, the design space (the component's values allowed variations) is restricted to be around the best values obtained in the previous steps. After this final optimization step, the resulting component's values take into consideration all the parasitic effects in the circuit. In order to facilitate the convergence of the GA during the first step, the cost function uses variable goal specifications. By starting the optimization with an "easier" goal and then converging the goal to the desired specifications, it is possible speed up the convergence process and obtaining a solution in fewer generations.

## 4 A 2nd Order Low-pass SC Filter

A 2nd order low-pass biquad filter (Fig. 1) is presented as a proof-of-concept for the proposed design method. This architecture is based on the continuous low-pass Sallen-Key topology replacing the resistors with parallel SC branches. Capacitors $C_2$, $C_B$ and $C_{B2}$ were added to the architecture to facilitate the compensation of the parasitic capacitances in each node.

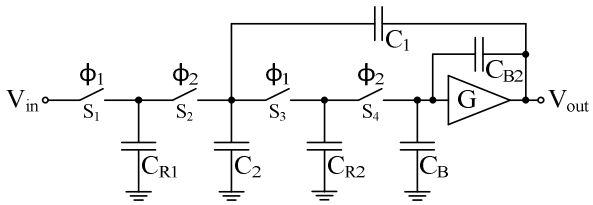


**Fig. 1.** Low-pass SC biquad filter in single-ended configuration.

### 4.1 First Step – Top-level Optimization

In the top level optimization, all the filter components are considered ideal (capacitors, switches and amplifier). The chromosome used in this step, which is shown in Table 1, contains the values of the capacitors and the desired gain for the amplifier. Once the values of the capacitors are generated, they are scaled down based on the smallest capacitor and the desired minimum value. The optimization will then try to find a solution that best fits the design specifications, while minimizing the gain value, because this will make the optimization of the amplifier circuit, in the second step, easier, as this value will be used as a design specification. The optimization will also try to minimize the total value of the capacitors.

**Table 1.** Chromosomes used in each optimization step by the GA.

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Top level | $C_{R1}$ | $C_{R2}$ | $C_1$ | $C_2$ | $C_B$ | $C_{B2}$ | G | | | | | |
| Amplifier | $W_1$ | $L_1$ | $W_2$ | $L_2$ | $W_3$ | $L_3$ | $W_4$ | $L_4$ | $W_5$ | $L_5$ | $I_D$ | $V_{cm}$ |
| Switches | $W_{s1}$ | $W_{s2}$ | $W_{s3}$ | $W_{s4}$ | $L_s$ | | | | | | | |

The design specifications in this step are given in the frequency domain (Fig. 2), and are evaluated based on the ideal transfer function of the filter, which was obtained from a charge conservation perspective, considering that the filter's output is sampled at the end of phase $\Phi_1$. The passband specification is controlled by the indicators $F_{passlow}$ and $F_{cutoff}$, in which the signals attenuation must be delimited between $A_{max1}$ and $A_{max2}$, i.e., these four indicators are used to obtain the desired low frequency gain of the filter and move the poles to frequencies around or above $F_{cutoff}$. To place the poles as close as possible to the cutoff frequency, two additional indicators are used ($F_{specific}$ and $A_{min1}$). By indicating the desired attenuation at a specific frequency we are forcing the poles to move to the cutoff frequency. The indicators $F_s/2$ and $A_{min2}$ are used to reinforce the pole placement at the cutoff frequency.

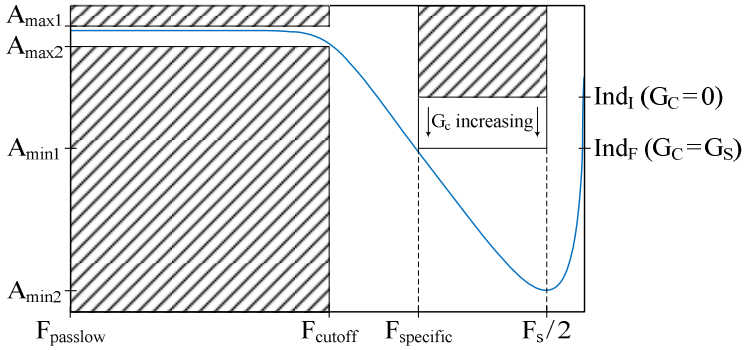


**Fig. 2.** Filter's variable goal specifications.

In this optimization step, the evaluation of the chromosomes is based on a variable goal equation (1), i.e., the specifications (goals) of the indicators ($A_{min1}$ and $A_{min2}$) will start with an initial value ($Ind_I$) and converge as the generations progress, following an exponential evolution, to the final value ($Ind_F$). The speed at which the indicator converges to the final value is controlled by the variable w. The variables $G_C$ and $G_S$ represent the current generation and the generation at which the indicator reaches its final value at the latest, respectively. Fig. 2 shows how the indicator $A_{min1}$ behaves when using the variable goal equation. While converging from $Ind_I$ to $Ind_F$, the optimizer will find the chromosome that satisfies the passband specification and that has an attenuation at $F_{specific}$ closest to the variable goal equation, at the current generation. Once the variable goal equation reaches the final value ($G_C = G_S$), the optimizer will find the chromosome that satisfies the passband specification and that has the smallest $A_{min1}$ at $F_{specific}$. By temporarily softening the specifications we are increasing the probability of converging to the best solution.

$$\text{Variable Goal Specification} = \text{Ind}_F + (\text{Ind}_I - \text{Ind}_F)e^{-5\,w(G_c/G_s)} \quad (1)$$

### 4.2 Second Step – Amplifier Optimization

In this step, the amplifier circuit is designed to have the gain value obtained in the previous step and optimized following the time-domain methodology that was presented in [5], which ensures that if a given settling error is reached within the desired settling time, then the amplifier has enough open-loop gain, closed-loop bandwidth, and slew-rate. This methodology simplifies the circuit's evaluation and helps the optimization process to converge faster. To calculate the settling time it is necessary to obtain the closed-loop circuit transfer functions during phase $\Phi_2$ and $\Phi_1$ (Fig. 3a and Fig. 3b), and apply the inverse Laplace transform multiplied by a unity input step (1/s). The closed-loop transfer function can be obtained by replacing the amplifier block G(s) with its equivalent medium frequency small signal model. Both transfer functions need to be calculated because charge flows to the filter's output in both clock phases.

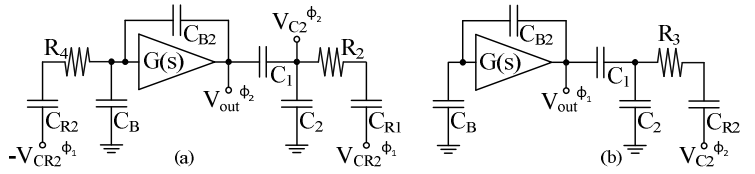


**Fig. 3.** Equivalent closed-loop circuit during clock phase (a) $\Phi_2$ and (b) $\Phi_1$.

$V_{CR2}^{\Phi_1}$ and $V_{C2}^{\Phi_2}$ represent the charge stored in capacitor $C_{R2}$ during phase $\Phi_1$ and in capacitor $C_2$ during phase $\Phi_2$, respectively, and can be calculated from (2), where $V_{amp}$ represents the amplitude of the input signal.

$$V_{C2}^{\Phi_2} = C_{R1}V_{amp}/(C_1 + C_2 + C_{R1})$$
$$V_{CR2}^{\Phi_1} = (C_1 + C_2)V_{C2}^{\Phi_2}/(C_1 + C_2 + C_{R2}) \quad (2)$$

The amplifier circuit used is shown in Fig. 4. Due to its differential configuration, this amplifier is capable of achieving gains larger than one.

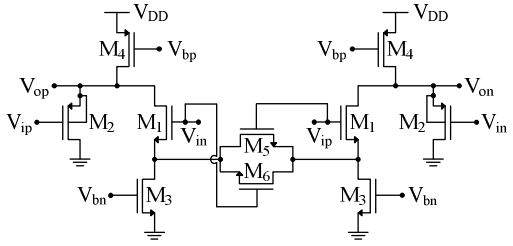


**Fig. 4.** Voltage-combiner amplifier with source degeneration.

The chromosome for this step (Table 1) contains the width and length of the amplifier's transistors, the biasing currents and the input common-mode voltage. The design specifications which are evaluated during this step are the average between the amplifier's input and output common mode voltages, which is evaluated based on DC Operating Point (OP) simulation; the closed-loop gain, which is calculated from the step response with s = 0; the settling time during phase $\Phi_2$ and $\Phi_1$, also calculated from the step response; and the amplifier's current and area.

During this optimization step, the amplifier's input and the input to output parasitic capacitances are calculated based on a DC OP simulation. Once the specifications are met the corresponding parasitic capacitances are stored, to be later compensated into capacitor $C_B$ and $C_{B2}$. Considering the amplifier circuit from Fig. 4, the compensated capacitor values can be obtained from (3), where $G_1$ and $G_2$ represent the voltage gain between the gate and drain and the voltage gain between the gate and the source of transistor $M_1$, respectively.

$$\begin{aligned} C_{B2}{}' &= C_{B2} - C_{gb2} - C_{gs2} \\ C_B{}' &= C_B - C_{gb1} - (1+G_1)C_{gd1} - (1+G_2)C_{gs1} - C_{gd2} - C_{gg5} \end{aligned} \tag{3}$$

### 4.3 Third Step – Switch Sizing Optimization

In the third step, the switches dimensions are optimized. The chromosome for this step (Table 1) contains the widths and lengths of the transistors operating as switches. Even though it is possible to use the same methodology as in the previous step and obtain the exact expressions for the time constants, it is computationally heavy and should only be used when first order RC approximations do not give sufficiently accurate results. In this filter the only switch that requires the computationally heavy method is switch $S_2$, because it is the switch most susceptible to the charge effect from the amplifier at transistor level. The settling time of this switch can be obtained from the closed-loop circuit shown in Fig. 3a considering node $V_{c2}{}^{\Phi_2}$ as the output instead of $V_{out}{}^{\Phi_2}$. The remaining RC time constants are calculated using first order approximations. The fitness equation of this step is based on the RC time constants/settling time and the overall switch area.

Clock-boosted phases were used to reduce the switches conductance non-linearity and overall value. During this step the value of the switches parasitic capacitances are calculated based on a DC OP simulation and stored, so that they can be used in the next step to compensate their effect on the filter.

### 4.4 Fourth Step – Top-Level Adjustment

The last optimization step is used to validate the equation-based design through electrical simulation and to fine-tune the capacitor values. The filter transfer function is now evaluated by running an electrical transient time simulation of the impulse response of the complete filter circuit. Since this procedure is very computational intensive and takes some time, it is difficult to use large populations or a large number of generations in this step. Due to this limitation, the design space is restricted to be around the values of the best chromosome obtained previously. Moreover, the capacitor values are adjusted to take into consideration the parasitic capacitances previously calculated. Unlike the calculation of the amplifier's parasitic capacitances which is relatively straightforward, due to their value being constant for a fixed voltage, the value of the switch's parasitic capacitances can have a variation of over 5 times depending if the switch is ON or OFF, making the compensation process more complex. Equation (4) was implemented to overcome this problem. The first generation chromosomes are all identical apart from a random compensation factor (CF) which varies between 0 and 5. From this initial population, it is possible to converge to an optimized solution very rapidly, i.e., within a few generations.

$$C_{comp} = C_{nom} - CF\, C_{par}, \qquad 0 < CF < 5 \tag{4}$$

## 5 Simulation Results

The biquadratic low-pass filter shown in Section 4 was designed in a standard 1.2 V 130 nm CMOS technology. The filter specifications used in this section are shown in Table 3. All simulations obtained from the optimizer were validated in Spectre using BSIM3V3.2.4 models of the transistors and MIMCAPS capacitor models (including parasitics).

In the first step, several optimizations were performed with and without the use of the varying goal specifications, on average, without using the varying goal specifications; it took the optimizer 96 generations to find a chromosome with fitness above 90%, and only 58 generations when using the varying goal specifications during the first 30 generations. In both cases, each generation was composed of 2500 chromosomes. The values obtained in this step were $C_{R1}$ = 54.44 fF, $C_{R2}$ = 50.00 fF, $C_1$ = 4530.80 fF, $C_2$ = 99.24 fF, $C_B$ = 473.95 fF, $C_{B2}$ = 131.64 fF, and G = 1.

Table 2 shows the amplifier specifications, the simulation results and the best chromosome optimized in the second step, obtained after only 10 generations of 2500 chromosomes each. The results show that the continuous time equation-based methodology gives similar results to the ones obtained through Cadence. Based on the DC OP simulation of the amplifier using the best chromosome, the values of the parasitic capacitances were calculated and compensated into capacitors $C_B$ and $C_{B2}$.

**Table 2.** Amplifier specifications, simulation results, and best chromosome.

| | Norm. closed-loop gain | Settling-Time $\Phi_2$ (%) | Settling-Time $\Phi_1$ (%) |
|---|---|---|---|
| Specifications | 3.8808 | < 75.0 | < 75.0 |
| Optimizer | 3.8808 | 65.13 | 59.92 |
| Cadence | 3.8808 | 65.20 | 55.20 |

| $W_1$ (µm) | $W_2$ (µm) | $W_3$ (µm) | $W_4$ (µm) | $W_5$ (µm) | Power (µW) | $C_{Bcomp}$ (fF) |
|---|---|---|---|---|---|---|
| 0.37 | 62.29 | 39.19 | 90.5 | 0.38 | 261.38 | 468.67 |
| $L_1$ (nm) | $L_2$ (nm) | $L_3$ (nm) | $L_4$ (nm) | $L_5$ (nm) | $V_{cmi}$ (mV) | $C_{B2comp}$ (fF) |
| 520 | 240 | 350 | 450 | 220 | 450 | 26.99 |

The filter's switches were also optimized in order to have time constants small enough to charge the capacitors in less than half a clock period. The length chosen for the switches was fixed at L = 120 nm and the optimized widths obtained were W1 = W3 = W4 = 240 nm and W2 = 300 nm. The optimizer took 15 generations of 2500 chromosomes to find the smallest widths for the switches while maintaining times constants small enough to charge the capacitors in less than half a clock period.

Table 3 shows the results obtained during each step of the optimization process. From rows (B) and (C), it can be concluded that the equation method for the automatic compensation of the amplifier's parasitic capacitances is very accurate. From (E) and (F), it can be seen that the open source simulator Ngspice gives very similar results to Cadence.

**Table 3.** Specifications and simulation results of the low-pass SC filter.

| | | $F_{passlow}$ | $F_{cutoff}$ | $F_{specific}$ | $F_s$ / 2 |
|---|---|---|---|---|---|
| | | 10 kHz | 1 MHz | 6 MHz | 50 MHz |
| (A) | Specifications | ≤ 0.01 | ≥ -3.01 | ≤ -30 | ≤ -59 |
| (B) | Equations/Cadence using ideal components | 0.00 | -2.95 | -30.78 | -59.87 |
| (C) | Cadence using real amplifier and ideal switches | 0.01 | -2.94 | -30.78 | -59.87 |
| (D) | Ngspice real circuit before parasitic compensation | 0.00 | -2.91 | -30.73 | -59.89 |
| (E) | Ngspice real circuit after optimization complete | 0.00 | -3.00 | -31.47 | -60.63 |
| (F) | Cadence real circuit after optimization complete | 0.00 | -3.03 | -31.50 | -60.61 |

In the last step, after 12 generations, the capacitor values obtained were $C_{R1}$ = 53.14 fF, $C_{R2}$ = 47.78 fF, $C_1$ = 4754.51 fF, $C_2$ = 97.29 fF, $C_B$ = 459.30 fF, $C_{B2}$ = 27.71 fF. Although a solution that satisfies all the specifications can be found after a single generation in the top-level adjustment, using equation (4), the optimization process continued for another 11 generations in order to try to find an even better solution than the one obtained after the first generation.

## 6 Conclusion

A design methodology for SC filters based on a GA using hybrid cost functions with varying goal specifications was proposed. The cost functions first use equations to obtain approximate solutions, and once all specifications are met, the GA uses the results of transient electrical simulations of the circuit in the cost functions, resulting in accurate transfer functions and allowing the compensation of parasitic capacitances within a reasonable amount of generations. Furthermore, it was concluded that using variable goal specifications reduces even further the amount of generations needed to obtain a solution within the design specifications.

## References

1. Perez, A.P., Maloberti F.: Performance enhanced op-amp for 65nm CMOS technologies and below. In: IEEE Int. Symp. Circuits and Systems (ISCAS), pp. 201–204 (May 2012)
2. Serra, H., Paulino, N., Goes J.: A switched-capacitor biquad using a simple quasi-unity gain amplifier. In: Proc. IEEE Int. Symp. Circuits Systems (ISCAS), pp. 1841–1844 (May 2013)
3. Santos-Tavares, R., Paulino, N., Goes, J.: Time-Domain Optimization of CMOS Amplifiers - Based on Distributed Genetic Algorithms. LAP LAMBERT Academic Publishing (2012)
4. Figueiredo, M., Santos-Tavares, R., Santin, E., Ferreira, J., Evans, G., Goes, J.: A two-stage fully differential inverter-based self-biased CMOS amplifier with high efficiency. In: IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, pp. 1591–1603 (May 2011)
5. Santos-Tavares, R., Paulino, N., Goes, J., Oliveira, J.: Optimum sizing and compensation of two-stage CMOS amplifiers based on a time-domain approach. In: Proc. IEEE Int. Conf. on Electronics, Circuits Systems (ICECS), pp. 533–536 (Dec. 2006)
6. Nenzi, P., Vogt, H.: Ngspice users manual version 25. http://ngspice.sourceforge.net/ [Online; Accessed 8-October-2013]
7. de Melo, J. L. A., Nowacki, B., Paulino, N., Goes, J.: Design methodology for sigma-delta modulators based on a genetic algorithm using hybrid cost functions. In: Proc. IEEE Int. Symp. Circuits Systems (ISCAS), pp. 301–304 (May 2012)