A 0.5 V Ultra-low Power Quadrature Ring Oscillator

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Abstract. In this paper we present a CMOS quadrature ring oscillator operating at 0.5 V. Due to this very low voltage conditions, new project technique using the available terminal of the transistors (bulk) is used in order to reduce the threshold voltage of the transistors, thus improving the voltage headroom. The technique is applied in a conventional inverter-based ring oscillator with a feedback topology capable to generate quadrature signals. Simulations results in a 130 nm CMOS technology shows that a very simple VCO in the GHz range can be obtained, by changing the bulk voltage of transistors (NMOS or PMOS). The circuit operates with less than 50 µW achieving a FoM of about -115 dBc/Hz at 10 MHz offset.

Keywords: Quadrature RC oscillator, CMOS circuit, Low voltage, Ultra-low power.

1 Introduction

Nowadays there is a huge demand on ultra-low power circuits for portable equipment, in wireless communication applications. Moreover, designers try to reduce the production cost, reducing the circuits die area (avoiding the use of on-chip inductors) and using standard CMOS technology. Thus, they try to obtain high frequency performance, with low supply voltage and low power.

This is the motivation for use modern receivers receiver architectures such as Low-IF Intermediate Frequency (IF) or Zero-IF, which can be used to further reduce the cost since they do not require eternal image reject filters and can be designed in a single chip using standard CMOS technology without inductor [1]–[3]. Typical applications are in biomedical bands, such as Wireless Medical Telemetry Services (WMTS) and Industrial, Scientific, and Medical (ISM), since the main requirements are low power consumption and low cost [4]. The oscillator that is a key block in these systems will be investigated in this paper.

Quadrature Ring oscillators are key blocks on the design of these architectures since they can be fully integrated, they do not have inductors and thus occupying very low area. They have higher tuning range (useful to cover several bands) and are able to provide quadrature signals with low quadrature error [5].

In this paper, we present a CMOS ring oscillator [6] capable to achieve quadrature outputs for very low voltage operation (in our case 0.5 V). A circuit design in a 130 nm CMOS technology proves that changing the voltage of the bulk node in NMOS and PMOS transistors allows the reduction of the transistor threshold voltage (V_{th}) [7]. With that change we are able to increase the transistor transconductance (g_m) (in comparison with the original), and therefore, designing a Voltage Controlled Oscillator (VCO) for the GHz range with very low power and high Figure Of Merit (FoM). The tuning of the oscillator in the GHz range can be achieved by changing the bulk voltage, while keeping a low supply voltage, with a FoM of -114.7 dBc/Hz at 10 MHz offset.

In section 2, we describe the contributions of this paper for the conference theme. In section 3, we describe low voltage techniques for CMOS inverter. In section 4, we present the proposed circuit and we present the simulation results, and finally, in section 5 we draw the conclusions.

2 Contributions for Technological Innovation for Collective Awareness Systems

Nowadays, the emergence of collective awareness systems is pushing the performance of end user interactive objects. These devices are embedded with sensors and actuators with the ability to communicate and exchange information, in a global cloud environment “Internet of the future” or “Internet of Things”. The physical communication plays a critical role in portable wireless devices equipped with very low power modern receivers with very low noise, and accurate and stable frequencies signals to ensure a reliable and efficient communication in a crowded channel environment. With this goal in mind the design of Radio Frequency (RF) front-end blocks for low power applications, in CMOS technology, will contribute towards the achievement of more cheap and robust devices. In this paper we will focus on the design of low power wideband CMOS quadrature oscillators.

3 Low Voltage Technique for a CMOS Inverter

A basic ring oscillator is composed by and odd number of single-ended blocks in a feedback topology [1]-[2]. In the work proposed in [6] they combine 4 blocks of 3 inverter stages in a quadrature ring oscillator. In this work we use the circuit topology proposed in [6], but with the inverter operating in ultra-low power voltage (0.5 V) for very low power consumption. The basic inverter cell is shown in Figure 1.

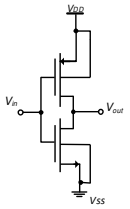

Fig. 1. Basic CMOS Inverter.

This cell is composed by two MOSFETs. The top MOSFET is a PMOS transistor and the bottom is a NMOS transistor. The bulk is linked to the respective sources, PMOS source is linked to V_{DD}, NMOS source is connected to Vss, reducing the value of the threshold voltage, V_{th}, to V_{T0} (V_{th} voltage at V_{BS}=0V). Interestingly, this threshold voltage, can be further reduced by directly biasing the bulk-source junction, as shown in [1]-[2]

$$V_{th} = V_{T0} - \gamma \cdot \left(\sqrt{\phi_o} - \sqrt{\phi_o - V_{BS}} \right) \tag{1}$$

where ϕ_F is the Fermi potential, γ is the body-effect coefficient, $\Delta \phi \approx 6\ kT/q$ and $\phi_0 = 2\phi_F + \Delta\phi$.

The first modification for the basic CMOS inverter is to add a voltage different than zero to the bulk of transistor NMOS, V_{CTRL}, as shown in Figure 2-a). This is possible since we are using CMOS triple well process.

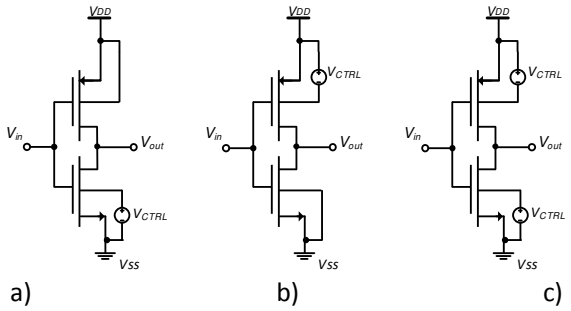

Fig. 2. Voltage source added to: a) bulk of the NMOS b) bulk of the PMOS c) both NMOS and PMOS.

The second change is to perform the same modification to the transistor PMOS, as shown in Figure 2-b). Thus, the final circuit is shown in Figure 2-c), with the objective of changing simultaneously both bulk voltages (in the range of 0 to 0.5 V) in order to reduce the transistor's V_{th}. The final configuration of the inverter represented in Figure 2-c), is formed by PMOS transistor with width of 3 µm and a length (L_{min}) of 120 µm while for the NMOS transistor the width is set to 1 µm maintaining L_{min} in 120 µm. In every single schematic the results were similar in the sense of reducing the values of V_{th}. But more effective changes are achieved by changing simultaneously the bulk voltages of both devices. In Figure 3 it is shown that the reduction curve of V_{th} varying the bulk voltage between 0 and 0.5 V.

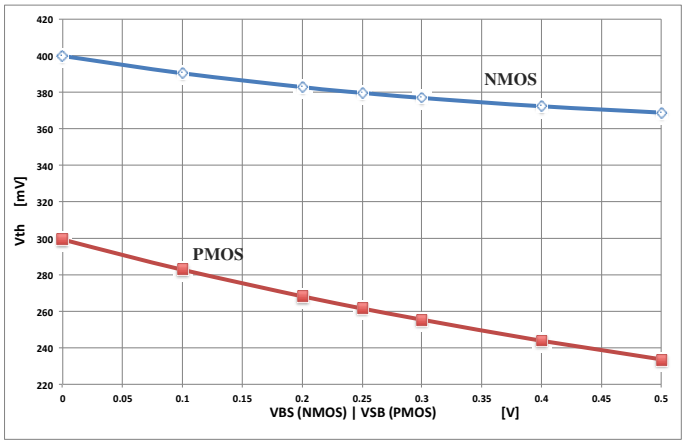

Fig. 3. V_{th} reduction for the NMOS and the PMOS transistors.

4 Proposed Circuit for a 0.5 V Ring Oscillator

The proposed low-voltage circuit is shown in Figure 4. It consists of a ring oscillator with quadrature outputs formed with eight inverters, powered by a 0.5 V source voltage with the objective of achieving low power consumption. Low voltage operation is achieved by reducing the V_{th} through the bulk, as explained in section 3. The inverter transistors sizing was done in order to minimize the power consumption and L_{min} has been chosen ensuring that the inverters operate at 1 GHz. Due to the transistors mobility differences in UMC BSIM3V3 130 nm, the PMOS have width three times higher than NMOS transistors.

The simulations revealed that the optimal results were obtained with 0.5 V in bulk V_{CTRL}. PMOS and NMOS respectively have the bulk driven by an external source voltage in a similar process like the work proposed in [7].

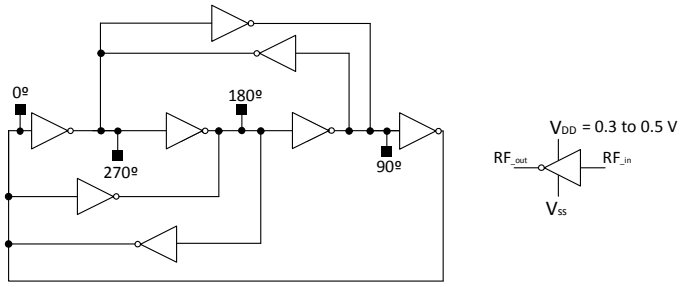

Fig. 4. Quadrature four-stage ring oscillator.

To evaluate the performance of the overall circuit, it is used the accepted FoM given by,

$$\mathrm{FoM} = L_{\mathrm{measured}} + 10 \cdot \log\left[\left(\frac{\Delta f}{f_{OSC}}\right)^2 \cdot \frac{I_{\mathrm{core}} \cdot V_{DD}}{1mW}\right], \qquad (2)$$

where, $L_{measured}$ is the value of the phase noise measured at 10 MHz, Δf is 10 MHz and I_{core} is the current consumption of the circuit core.

Using the traditional inverter in the quadrature ring oscillator, represented in Figure 1, and varying the supply voltage between 0.3 and 0.5 V, it is possible to see that the FoM has a variation smaller than 1.4 dB, as shown in Figure 5. Other important result is the current consumption that rises when the FoM reach higher values, as shown in Figure 6.

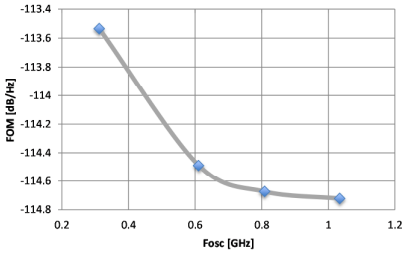

Fig. 5. FoM versus oscillation frequency

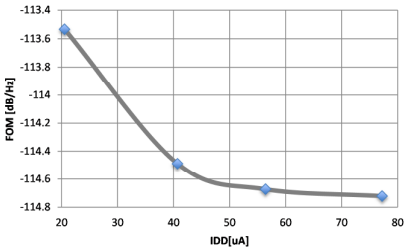

Fig. 6. FoM versus current supply

The result in Figure 7 was chosen from the range of FoM variations, a range over 3 dB, for the case of schematic in Figure 2-c). Clearly the best situation in Figure 8 is the first one, were the FoM has the best value and the current is the smallest one.

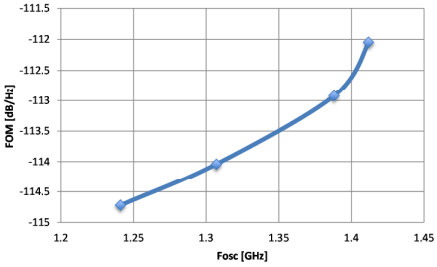

Fig. 7. FoM versus oscillation frequency

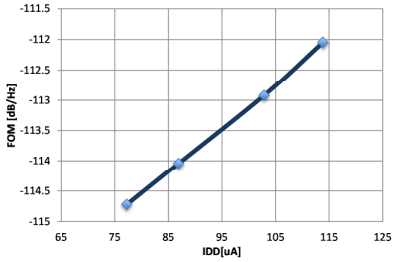

Fig. 8.FoM versus current supply.

Figures 9 and 10 show the results obtained when changing the threshold voltage of both transistors.

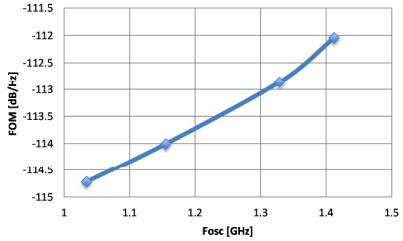

Fig. 9.FoM versus oscillation frequency.

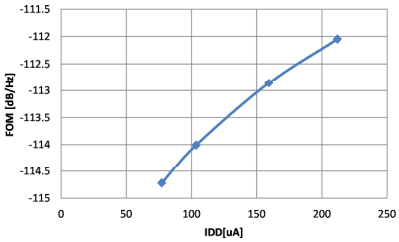

Fig. 10. FoM versus current supply.

In Table 1 is possible to visualize the advantages and disadvantages from each schematic presented previously (Figure 2-a), b) and c)). The best results are obtained using the inverter with both reduced V_{th}, were the FoM varies up to 3 dB. Moreover, this simultaneous V_{th} reduction in both transistors enables the operation of the oscillator at very low voltage supply, with reduced current supply.

Table 1 – Summary

Schematic Model	Advantages	Disadvantages
Original Inverter	Lowest values of current	V_{th} results are very limited Can only oscillate main source voltage
VCTRL added to NMOS transistor	Low values of current	V_{th} value don't lower enough to get an earlier functioning
VCTRL added to PMOS	Low value of current; the best V_{th} values 3 dB's FoM difference The circuit works with less voltage	Only V_{th} drops considerably
VCTRL added to both PMOS and NMOS	Low values of current More than 3 dB's FoM difference Both V_{th} values drops considerably	Since both bulks are used (can not operate as VCO)
Bulk conected to ground in both MOSFETs	FoM is constant in the VCO tuning range	V_{th} doesn't drop almost maintain constant

5 Conclusions

In this paper we present a low voltage and low power wideband CMOS quadrature ring oscillator with feedback to ensure accurate quadrature outputs. A circuit design at 0.5 V is presented in a 130 nm CMOS technology, which validates the proposed methodology. Simulation results show that changing the bulk voltage named V_{CTRL} can control the oscillator frequency. Therefore, this circuit can be used as VCO in Phased Locked Loop (PLL) block, under low voltage supply. V_{CTRL} can be reduced to 0.4 V or 0.3 V with very low power consumption, less than 50 µW, with a FoM of -114.7 dBc/Hz at 10 MHz offset. The proposed circuit is especially useful for low power and low voltage operation in biomedical applications.

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