Analysis of a Multi-Ratio Switched Capacitor DC-DC Converter for a Supercapacitor Power Supply

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Abstract. An energy harvesting system can use a supercapacitor in order to store energy; however, a voltage regulator is required to obtain a constant output voltage as the supercapacitor discharges. A Switched-Capacitor DC-DC converter allows for complete integration in CMOS technology, but requires several topologies in order to obtain a high efficiency. This paper presents the complete analysis of these topologies in order to determine expressions that allow to design and determine the optimum input voltage ranges for each topology. These expressions are verified using electrical simulations.

Keywords: DC-DC power converters, Switched capacitor circuits, Supercapacitors, Performance analyses, Design optimization, Efficiency.

1 Introduction

In order to achieve infinite operation, electronic systems must obtain their energy directly from the surrounding environment [1]. This kind of procedure is commonly known as energy harvesting. Depending on the environment where the system is located at there are different energy sources that can be harvested [2]. In the case of systems with small size, the available energy is necessarily reduced, typically only providing a fraction of the necessary power needed for the operation of the system. Therefore, such a system has to be powered down while it harvests enough energy in order to work during a short time and then this cycle is repeated. This type of operation is useful for wireless sensor nodes, where the node only needs to report data periodically. This operation requires an energy storing device, which can be either a rechargeable battery or a supercapacitor. A rechargeable battery has the advantage of having a larger energy storing capacity, but its lifetime is seriously reduced by the number of charge/discharge cycles (typically the maximum number is around 1000 cycles). A supercapacitor has the advantage of having limitless charge/discharge cycles and being less expensive than a battery, but it stores much less energy than a battery for the same volume [3]. Depending on the mode of operation of the energy harvesting system, a battery, a supercapacitor or both can be used as the energy storing device. In the case of low power remote sensor that uses a power-down power-up cycle, it makes more sense to use a supercapacitor as the energy storage.

The energy stored in a capacitor is given by $E_c = 1/2 \cdot C \cdot V_c^2$, this means that as the capacitor supplies energy to the circuit its output voltage drops. As an example a 1 F supercapacitor charged to its maximum voltage (usually 2.3 V) can store 2.645 J, if this capacitor supplies energy for a circuit with a supply current of 20 mA during 10s, its output voltage would drop $\Delta V_c = I \cdot C = 200$ mV. Since the power supply voltage of the circuit should be constant it is necessary to have a voltage regulator between the supercapacitor and the circuit. In order to maximize the energy retrieved from the supercapacitor it is necessary for the voltage regulator circuit be able to both down-convert and up-convert the input voltage with an efficiency as high as possible. This prevents the use of a linear voltage converter because it can only step-down the voltage and its efficiency is reduced when the input voltage is much larger than the output voltage. The voltage regulator can be implemented using either an inductor based or a capacitor based DC-DC converter. The first option requires an inductor which is not feasible to implement in a CMOS integrated circuit. The second option can be fully integrated in a CMOS integrated circuit; however, switched-capacitor (SC) based DC-DC converters have maximum efficiency for a specific input output voltage ratio. This means that in order to maintain a high efficiency the SC voltage converter circuit has to change its topology as the input supercapacitor voltages decreases [4]. Therefore a careful analysis of each converter topology should be carried out in order to determine its efficiency as a function of the input voltage and the different parasitic capacitance of the circuit. This analysis will determine the voltages values that will result in a change in the voltage conversion factor.

2 Relationship to Cloud-based Solutions

Cloud-based solutions rely on several servers, which are connected together through specialized connections, to distribute data processing tasks among them to overcome limitations in environments where the processing and information storage capability is lacking.

Wireless sensor networks which are integrated into cloud services, e.g. wireless sensor networks for real-time data collection, usually rely on batteries to supply energy to the nodes of the network. Due to the limited lifecycle of batteries, the long term sustainability of the wireless sensor network is compromised. An alternative is to use supercapacitors that acquire energy through energy harvesting systems. Unlike a battery, supercapacitors can charge/discharge an unlimited amount of times, however, a voltage regulator is needed to obtain a constant output voltage as the supercapacitor discharges. This paper analyses several SC DC-DC converters topologies in order to determine the optimum input voltage ranges for each topology.

3 Analysis of the SC DC-DC Converter Topologies

As previously mentioned, a SC based DC-DC converter has maximum efficiency for a given conversion factor between its input and output voltage. This means that as the supercapacitor discharges and its output voltage drops while the output voltage

remains constant, it is necessary to use different topologies for the SC converter circuit in order to maintain high efficiency. There is a compromise between the number of different topologies and the complexity of the circuit. In this case the input voltage can vary from 2.3V to 0 V and the output voltage should be held constant around 1 V. Assuming that a supercapacitor with 1F is used, the available energy, for the maximum voltage, will be 2.645 J. When the capacitor voltage is equal to 1 V the energy remaining in the capacitor is still 0.5 J and when it is equal to 0.7 V the remaining energy is only 0.245 J. This means that there is a small payoff in trying to up-convert input voltages smaller than 0.7 V, which would require a circuit with a voltage conversion factor larger than 2. After analyzing the efficiency of several voltage conversion circuits for the different input voltages, it was decided to use only 4 SC capacitor voltage converter circuits. These are depicted in Fig. 1 and correspond to the voltage conversion factors of 1/2, 2/3, 1 and 3/2 [4]. Each of these converters is responsible for a given range of the input voltage (where its efficiency is maximized) and its clock frequency is adjusted in order to obtain an output voltage of 1 V at its output, independently of the input voltage and of the load. These 4 topologies can be combined into a single circuit with 3 capacitors that can be configured to any of the 4 topology using switches. In order to determine what are the input voltage ranges that maximize the efficiency for the different topologies it is necessary to analyze the behavior of each SC converter circuit to determine its operating parameters (efficiency and output voltage) as function of the different design parameters (capacitance values, clock frequency, etc) and the different non-ideal effects (e.g. parasitic capacitance, switch ON resistance).

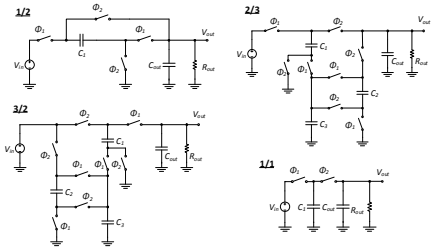

Fig. 1. Simplified schematics of the selected topologies for the SC converters

3.1 Analysis of the Efficiency of the 1/2 SC Converter

Assuming that the clock frequency is adjusted in order to have the desired output voltage (e.g. $V_{out} = 1$ V) and that output decoupling capacitor C_{out} is large enough, it is reasonable to assume that the output voltage value is constant. In this case, the schematics of the 1/2 SC converter circuit during phase ϕ_1 and ϕ_2 are shown in Fig. 2 and Fig. 3 respectively. In these schematics, C_B and C_T represents the bottom and top plate parasitic capacitances of C_1 and C_G represents the gate capacitance of all the CMOS switches in the circuit. In each clock cycle, the switches drain a charge (ΔQ_{in2}) from V_{in} through the clock buffers. Using conventional switched-capacitor circuit analysis techniques [5] (Chapter 5) it is possible to determine the charge in

each capacitor at the end of each clock phase. The resulting equations are shown in (1) and these allow to determine ΔQ_{in1}, ΔQ_{in2}, ΔQ_1, and ΔQ_2.

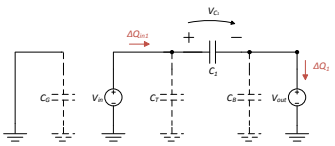

Fig. 2. Simplified schematic of the 1/2 SC converter during phase $\boldsymbol{\phi_1}$

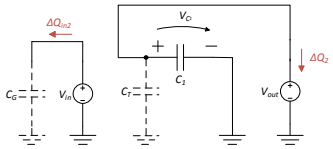

Fig. 3. Simplified schematic of the 1/2 converter during phase ϕ_2

$$\begin{cases} (V_{in} - V_{out})\, C_1 + V_{in}\, C_T = V_{out}\, (C_1 + C_T) + \Delta Q_2\,, \\ 0 = V_{in}\, C_G + \Delta Q_{in2}\,, \\ -V_{out}\, C_1 = (V_{out} - V_{in}) C_1 + V_{out}\, C_B + \Delta Q_1\,, \\ V_{out}\, (C_1 + C_T) = (V_{in} - V_{out}) C_1 + V_{in}\, C_T + \Delta Q_{in1}\,. \end{cases} \tag{1}$$

The input (P_{in}) and output (P_{out}) power are calculated using ΔQ_{in1}, ΔQ_{in2}, ΔQ_1, and ΔQ_2 and the values of V_{in} and V_{out} and are given by

$$\begin{cases} P_{in} = I_{in}\, V_{in} = V_{in}\, (\Delta Q_{in1} + \Delta Q_{in2})\, F_{CLK}\,, \\ P_{out} = I_{out}\, V_{out} = V_{out}\, (\Delta Q_1 + \Delta Q_2)\, F_{CLK}\,. \end{cases} \tag{2}$$

The efficiency (η) is defined as the ratio between P_{out} and P_{in},with $V_{out} = 1$ V , it is given by.

$$\eta_{1/2} = \frac{C_B + C_T - C_T\, V_{in} - 2\ C_1\, (V_{in} - 2)}{V_{in}(-Vin\ \ (C_1 + C_G + C_T) + 2\, C_1 + C_T} \tag{3}$$

The 1/2 SC converter circuit was simulated in Spectre with ideal switches and capacitors for different input voltages between 2 to 2.5 V and with V_{out} fixed at 1 V. From these transient simulations its efficiency was calculated and compared to the efficiency calculated using (3) for different parasitic capacitance values. The resulting efficiency values as a function of V_{in} and of the parasitic capacitance ($C_G = C_T = C_B$) assuming 0%, 1%, 5% and 10% are plotted in

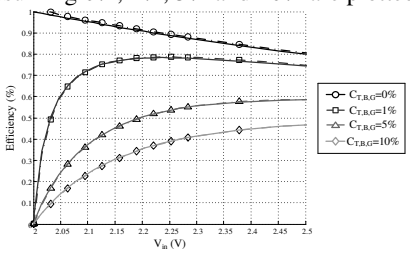

Fig. **4**. These simulation results prove that (3) accurately describes the behavior of the efficiency of the converter and validates the theoretical analysis.

3.2 Analysis of the Output Voltage of the 1/2 SC Converter

A similar analysis can be performed in order to determine the output voltage of the SC converter, assuming that its output is connected to a load resistor (R_{out}) and a decoupling capacitor (C_{out}) with a very large time constant compared to the clock period ($C_{out} \times R_{out} \gg T_{CLK}$). In this case V_{out} is constant during each clock cycle.

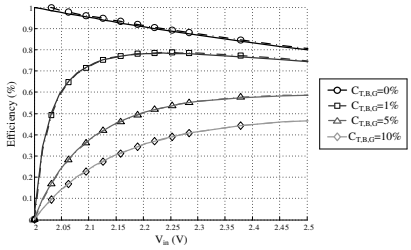

Fig. 4. Efficiency of the 1/2 SC converter circuit as a function of V_{in} and of $C_G = C_T = C_B$.

$$\begin{cases} (V_{in} - V_{out}[n-1])\, C_1 + V_{in}\, C_T + V_{out}[n-1]\, C_{out} = \\ \qquad = V_{out}\left[n - \frac{1}{2}\right]\left(C_1 + C_T + C_{out} + \frac{T_{CLK}}{2\, R_{out}}\right) \\ -V_{out}\left[n - \frac{1}{2}\right] C_1 + V_{out}\left[n - \frac{1}{2}\right] C_{out} = \\ \qquad = (V_{out}[n] - V_{in})\, C_1 + V_{out}[n]\left(C_B + C_{out} + \frac{T_{CLK}}{2\, R_{out}}\right) \end{cases} \tag{4}$$

The resulting equations are shown in (4). Solving in order to $V_{out}[n]$ and then considering the steady state condition ($V_{out}[n] = V_{out}[n-1] = V_{out}$), allows to calculate V_{out} (5). In order to simplify (5) it is possible to assume that $C_{out} \gg C_1$ resulting in (6).

Fig. 5 represents V_{out} as a function of the frequency for $V_{in} = 1V$: the solid lines are the plot of (6) and the marks correspond to the simulation results. These validate expression (6). This graph shows that it is possible to control the value of V_{out} by adjusting the clock frequency.

$$V_{out} = \frac{2\, V_{in}\, F_{CLK}\, R_{out}(C_1 + 2\, C_{out}\, F_{CLK}\, R_{out}\, (2\, C_1 + C_T))}{1 + 2\, F_{CLK}\, R_{out}\left(2\, C_1 + C_B + 2\, C_{out} + C_T + 2\, F_{out}\, R_{out}\left(C_{out}\, C_T + C_B\, (C_{out} + C_T) + C_1\, (C_B + 4\, C_{out} + C_T)\right)\right)} \tag{5}$$

$$V_{out} = \frac{(2\, C_1 + C_T)\, F_{CLK}\, R_{out}\, V_{in}}{1 + (4\, C_1 + C_B + C_T)\, F_{CLK}\, R_{out}} \tag{6}$$

Using (6) to calculate the clock frequency for a given V_{out} results in

$$F_{CLK} = \frac{V_{out}}{R_{out}(2\, C_1\, (V_{in} - 2\, V_{out}) + C_T\, (V_{in} - V_{out}) - C_B\, V_{out})} \tag{7}$$

Fig. 6 shows the plot of (7) for $V_{out} = 1V$, $P_{out} = 10$ mW ($R_{out} = 10\ \Omega$) and $P_{out} = 100$ µW ($R_{out} = 10$ KΩ) . As V_{in} approaches the conversion ratio ($V_{in} = 2V$), the clock frequency becomes infinite.

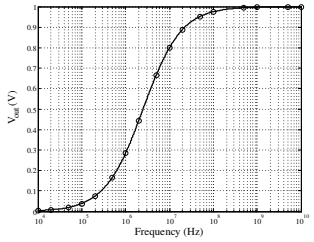

Fig. 5. V_{out} as function of the clock frequency

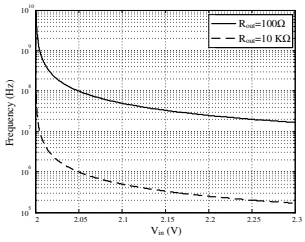

Fig. 6. Clock frequency as function of $\mathbf{V_{in}}$ for $\mathbf{V_{out} = 1V}$

4 Circuit Design

In the previous section a theoretical study of the 1/2 converter was carried out. The behavior of the other three converters was determined using the same methodology.

The 1/1 converter, C_1 is only affected by the top plate parasitic capacitance (C_T), because the bottom plate capacitance is shorted to ground in both phases. Since C_T is charged and discharged in parallel with C_1, there is no charge lost to ground through C_T. This means that the efficiency of this converter is not degraded by C_T. Only the gate capacitance from the switches causes a decrease in the efficiency.

The 2/3 and 3/2 converters have a similar topology except for the switches that connect to V_{in} and to V_{out}. In these converters, there are five parasitic capacitances: C_{T1}, C_{B1}, C_{T2}, C_{B2} and C_{T3}. Where the number 1, 2 and 3 refers to C_1, C_2 and C_3, respectively. The analysis showed that C_{T3} has no impact on the efficiency. Similarly to the 1/2 converter, this is because C_{T3} charges and discharges in parallel with C_3 in both phases. The other four capacitances result in a decrease in η.

In order to better understand the design constraints of the circuit, the circuit will be designed using a 130nm CMOS technology and the capacitors are implemented using MIMCAP including parasitics. Limiting the total area for the capacitors to 1 mm^2 results in a maximum capacitance value of 1 nF this means that 1/2 and 1/1 converters will have a capacitor of 1 nF; and the 2/3 and 3/2 converters will have 3 capacitors with 0.33 nF. This type of capacitors have a top and bottom plate parasitic capacitance of, approximately, 0.4% and 0.6% of the nominal value, respectively.

Equivalent equations to (6) were obtained for the remaining 3 converters using the same methodology. These equations are used to calculate V_{out} for the 4 converters for $P_{out} = 10$ mV ($R_{out} = 100\ \Omega$), V_{in} is 2, 3/2, 1 and 2/3, according to the converter ratio. V_{out} is plotted in Fig. 7 using the parasitic capacitances values of the selected technology. This plot shows that the 2/3 and 3/2 converters need a higher clock frequency to have $V_{out} = 1V$, these higher frequencies will lead to lower efficiency due to the power needed to drive the larger switches.

The analysis described in section 3.1 was applied to the remaining 3 converters and their efficiency was calculated. Fig. 8 shows the plot of $\boldsymbol{\eta}$ in function of $\boldsymbol{V_{in}}$. The solid lines are obtained from the equations and the shapes are simulation results. These plots were obtain for $\boldsymbol{C_G = 0}$. The efficiency graph of Fig. 8 was calculated independently of the clock frequency and ignoring the charge lost through the gate capacitance of the switches. Since the gate capacitance increases with the CMOS switch size, which increases with the clock frequency value, the efficiency also depends on the clock frequency. The clock frequency value for each converter as a function of the $\boldsymbol{V_{out}}$ in order to have $\boldsymbol{V_{out} = 1\ V}$ is shown in Fig. 9. This graph was obtained using similar expressions to (7) calculated for all the converters.

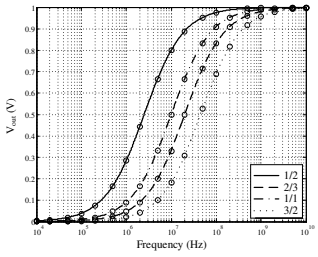

Fig. 7. $\mathbf{V_{out}}$ as function of the frequency clock, with $\mathbf{C_B = 0.6\%\ C_1}$, $\mathbf{C_T = 0.3\%\ C_1}$, $\mathbf{R_{out} = 100\ \Omega}$ and $\mathbf{V_{in}} = \{\mathbf{2, 1.5, 1, 0.67}\}$ according to the converter ratio.

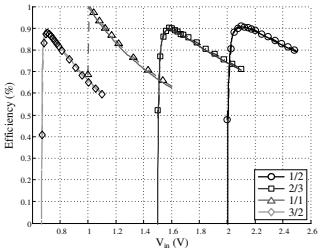

Fig. 8. $\boldsymbol{\eta}$ as function of $\mathbf{V_{in}}$ for the four converters with $\mathbf{C_B = 0.6\%\ C_1}$ and $\mathbf{C_T = 0.3\%\ C_1}$

The CMOS switches are constituted by NMOS and PMOS devices in parallel. These transistors are sized in order to have an ON resistance (R_{ON}) value that results in a time constant compatible with the clock frequency value. In [6] it is shown that R_{ON} and C_G for a settling error ($error$) and a frequency clock (F_{CLK}) and the capacitance coupled to the switch (C_1) are given by:

$$R_{ON} = \frac{1}{2\ C_1\ F_{CLK} \ln\left[\frac{1}{error}\right]} \tag{8}$$

$$C_G = 2\ k_R\ k_C \ln\left[\frac{1}{error}\right]\ F_{CLK}\ C_1 \tag{9}$$

Where $k_R = 806.24\ \Omega \cdot \mu m$ and $k_C = 7.1\ fF/\mu m$ are coefficients derived by simulation Spectre [6]. Replacing (9) in (3) results η as function of V_{in}, V_{out}, $error$, R_{out} and F_{CLK}. This now takes into account the effect of the frequency in the parasitic capacitances of the switches. Replacing (7) in this new expression results in η in function of V_{in}, V_{out}, $error$, R_{out}. This final equation describes the efficiency with the frequency adjusting to the value necessary to maintain $V_{out} = 1$ V and the extra power consumed by the switches due to this adjustment. Fig. 10 shows the plot of η as function of V_{in} with $P_{out} = 10$ mW ($R_{out} = 100\ \Omega$), $V_{out} = 1$ V, settling error of 1%, $C_B = 0.6\%\ C_1$ and $C_T = 0.3\%\ C_1$, for the 1/1 and 1/2 $C_1 = 1$ nF; and for the 2/3 and 3/2 $C_1 = 0.33$ nF. The plot shows the maximum achievable efficiency and the corresponding value of V_{in}. Through this it is possible to determine the range

of operation for each converter. For example, in this case the 1/2 converter works from 2.3 to 2.07 V, with a maximum of 84% and a minimum of 64% efficiency. The 2/3 converter works from 2.07 to 1.76 V, with a maximum of 65% and a minimum efficiency of 57%. The 1/1 converter works from 1.76 to 1.05V, with a maximum of 83% and a minimum efficiency of 57%. Finally, the 3/2 converter works from 1.04 to 0.67 V, with a maximum efficiency of 84%.

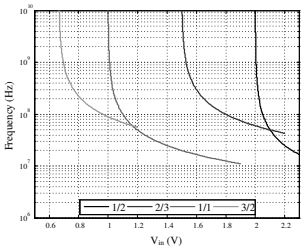

Fig. 9. Frequency clock as function of $\mathbf{V_{in}}$, for a $\mathbf{P_{out} = 10}$ mW ($\mathbf{R_{out} = 100\ \Omega}$) with $\mathbf{V_{out} = 1}$ V.

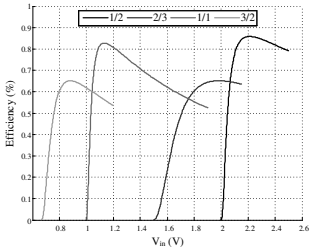

Fig. 10. η as function of V_{in} for a $P_{out} = 10$ mW ($R_{out} = 100\ \Omega$), $V_{out} = 1$ V, settling error of 1%, $C_B = 0.6\%\ C_1$, $C_T = 0.3\%\ C_1$, for the 1/1 and 1/2 $C_1 = 1$ nF; and for the 2/3 and 3/2 $C_1 = 0.33$ nF

5 Conclusion

This paper presented a theoretical analysis of a multi ratio SC DC-DC converter for a supercapacitor power supply of an energy harvesting system. The different SC circuits of the converter were analyzed in order to obtain expressions that allow computing their efficiency as a function of the input voltage. These expressions were verified using electrical simulations and then used to design the circuit for a 130 nm CMOS technology and determine the optimum input voltage ranges for each topology.

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