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Nelson Santos[1], J. Fernando Silva[2], Vasco Soares[1], Sónia F. Pinto[2], Duarte Sousa[2]

[1] Instituto Superior de Engenharia de Lisboa, INESC-ID
R. Conselheiro Emídio Navarro, 1959-007 Lisboa, Portugal
nsantos@deea.isel.ipl.pt, vesoares@deea.isel.ipl.pt
[2] Instituto Superior Técnico, Universidade de Lisboa, INESC-ID, DEEC, AC Energia
Av. Rovisco Pais, 1049-001 Lisboa, Portugal
fernando.alves@tecnico.ulisboa.pt, soniafp@tecnico.ulisboa.pt,
duarte.sousa@tecnico.ulisboa.pt

Abstract. This paper presents a high-voltage (HV) inverter to generate bipolar voltages with variable duty-cycle and frequency for HV pulsed power or HV electrical network applications. Each one of the four HV inverter switches is built with a series stack of semiconductor devices, derived from the Marx generator concept, using small capacitors to equally share the voltage among the individual series stacked semiconductors. A sliding mode control is used to control the output voltage and a delay technique is used to reduce *dU/dt* at the HV inverter output and to balance the capacitor voltages. The design and structure of the HV inverter switches is described together with the delay technique. Steady-state and dynamic behavior is evaluated. Simulation results are presented (using MATLAB/Simulink software) and discussed.

Keywords: Pulsed Power Systems, Marx Generator, Bipolar Pulses, High Voltage Inverter, Smart-grids.

1 Introduction

In power electronic applications solid state power semiconductor devices are used to transfer large amounts of power and energy, in a controlled way, sometimes for very short times, as in the case of pulsed power. In HV applications solid-state semiconductor devices are sought because they have lower power losses compared to older devices like spark gaps or vacuum tubes. However, for HV applications, a single power semiconductor device is still not able to hold-off the tens or hundreds of kV or allow the kA currents needed. Connecting power semiconductor devices in series or/and in parallel is a way to avoid these limitations [1], although issues like voltage sharing and pulse synchronization remain.

For kV applications, such as switches, inverters in smart-grids, choppers or pulsed power, the semiconductor devices like MOSFET (Metal Oxide Semiconductor Field Effect Transistor), GTO (Gate turn-OFF Thyristor) or IGBT (Insulated Gate Bipolar Transistor) can be connected in series and operated synchronously as a single switch device. To ensure proper operation of the switch it is crucial to balance the voltage between all the series connected semiconductor devices by dividing the voltage equally between them, both in steady-state and during transients.

However, even small variations of devices static and dynamic parameters, the imperfect synchronization or delay of the gate drive voltages, thermal impedance variations and asymmetrical parameters in the snubber circuits for voltage sharing [2], can impair the voltage balance among series semiconductor devices.

There are techniques to minimize the unbalanced voltages by using passive snubber circuits, active gate control circuits and voltage clamping circuits. Snubber circuits usually are RC (Resistor-Capacitor) or RCD (Resistor-Capacitor-Diode) in parallel with the collector-emitter of each IGBT of the stack, minimizing device switching losses while increasing the global losses and limiting the switching frequency. The active gate control proposes individual control of the signal gate of each device to dynamically balance the collector-emitter voltage. While this technique may not increase the switching loss or switching times, it presents some complexity in the drive circuit and may require additional small passive snubbers. Another approach, active voltage clamping, balances the voltage collector-emitter by using optimized snubbers (with low losses) and auxiliary circuits using usually extra semiconductor devices to improve the switching frequency restrictions [1].

This paper proposes a full-bridge inverter with four HV switches using IGBT, each one made of switching cells derived from the Marx generator concept [3], able to balance the voltages in the series cell stacks of each HV switch with efficiency. Performance evaluation is done using a typical inductive load at the output of the HV inverter and the voltage balancing is maintained, even with 10 % tolerance in the capacitor cells. Unsynchronized gate drive signals are used advantageously to reduce the output *dU/dt*, decreasing the load voltage stress and the electromagnetic interference problems [4].

2 Relationship to Cloud-based Solutions

Research works, like the described in paper, need computers to perform numerical calculations and simulations. Sometimes, one computer is not enough as it takes too long to finish the simulations. Cloud technology can help and increase the productivity of research teams that locally do not have powerful enough resources due to budget constraints and strict control on the distribution of funds. Additionally, the physical implementation of prototypes can benefit from cloud-based solutions by connecting several teams in real time for development, analysis and sharing in the community. In return, HV full-bridge inverters will be key players in the supply systems sustainability of cloud data centers, its integration with renewable energy resources and power quality control in smart-grids.

3 Proposed Topology

3.1 Marx Derived Switch

The original Marx generator topology charges n capacitors in parallel and discharges them in series to obtain the HV U_{HV} approximately equal to n times the charging power source U_{LV} voltage $U_{HV} = nU_{LV}$, without using step-up transformers. Figure 1(a) shows an example of Marx generator for positive HV pulses where the capacitors C_1, …, C_n are charged in parallel through the impedances Z_1, …, Z_n (resistive and/or inductive) when switches S_1, ..., S_n are turned OFF and discharged in series into the load, when switches S_1, ..., S_n are turned ON.

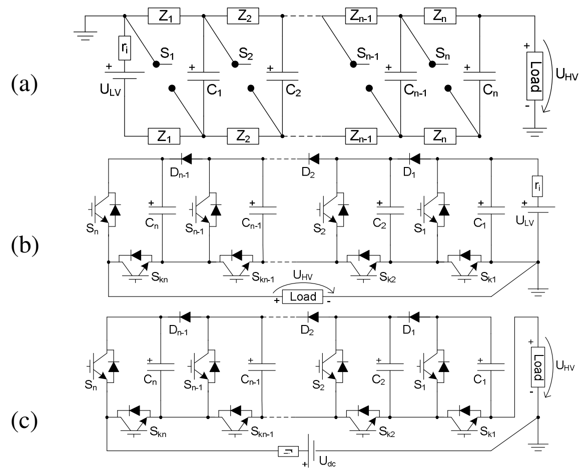

Fig.1. Marx derived topology; (a) Marx generator topology; (b) Solid-state HV positive pulse generator; (c) series switch for positive voltages.

To reduce the losses, the impedances and spark gaps are replaced by power semi-conductors, as depicted in Fig. 1(b), increasing the efficiency, the performance and the pulse frequency. To use the Marx generator concept as a switch, it is necessary to charge the capacitors in series (diodes of S_1 to S_n), to hold-off the HV, and to balance the capacitor voltage connecting them in parallel (diodes D_1 to D_{n-1}). Therefore, in the Fig. 1(b) circuit load and HV source are interchanged (Fig. 1(c)) to obtain a series stack of switching cells for positive HV pulses. This technique provides HV handling using U_{LV} (kV) rated semiconductor devices [3].

3.2 Full-Bridge Inverter Topology

The full-bridge inverter uses four HV Marx generator based switches Fig. 1(c), each switch denoted by S_{Mk} with $k \in \{1, …, 4\}$. The inverter outputs bipolar HV pulses from a single HV source U_{dc} (Fig. 2(a)). Each HV switch is composed by n series connected cells $n > U_{HV}/U_{LV}$. Each cell contains two IGBT S_{kn}, S_{Cn} with anti-parallel diodes (Fig.

2(b)). IGBT/diode hold-off voltages are imposed by capacitor C_n. The inter-cell diode D_n balances the C_n voltages.

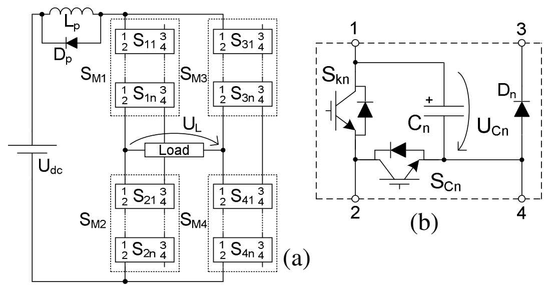

Fig.2. Proposed Circuit; (a) HV Inverter; (b) single cell based in Marx generator

Assuming the IGBTs S_{k1}, …,S_{kn} at each switch S_{Mk} are driven simultaneously, the inverter output voltage U_L depends on the states of S_{M1}, S_{M2}, S_{M3} and S_{M4}, obtaining three voltage levels, according to (1).

$$U_L = \delta(t)U_{dc} = \begin{cases} U_L = U_{dc} \ \text{ for } \delta(t) = +1 \ (S_{M1}, S_{M4} \ ON) \\ U_L = 0 \text{ for } \delta(t) = 0 \ (S_{M1}, S_{M3} \ ON \ or \ S_{M2}, S_{M4} \ ON) \\ U_L = -U_{dc} \text{ for } \delta(t) = -1 \ \ (S_{M2}, S_{M3} \ ON) \end{cases} \quad (1)$$

A sliding mode modulator [6], [7], [8] and [9] will be used to obtain the gate drive signals for the IGBT stacks S_{M1}, …, S_{M4} in order to control the output voltage U_0.

3.3 Operation of the Switch

Each switch S_{Mk} has two modes of operation, charging mode, if S_{kn} are OFF and S_{Cn} are ON, and balancing mode, if S_{kn} are ON and S_{Cn} are OFF. In the charging mode, the S_{Mk} switch is OFF and all capacitors C_1 to C_n are charged in series through the S_{C1} to S_{Cn} by HV source U_{dc}. Series charging leads to some voltage imbalance. Under the balancing mode operation (the S_{Mk} switch is ON) all the capacitors are connect in parallel through S_{k1} to S_{kn} and D_1 to D_n, therefore equal voltage sharing is achieved. Assuming that an upper stack capacitor exhibits a voltage higher than those on the bottom, a current path is established that balances the voltages among the capacitors on the switch S_{Mk} (Fig. 3(a)). However, under opposite conditions, a lower stack capacitor cannot discharge to the remaining ones. This issue can be avoided by the replacement of diodes D_1 to D_n by IGBTs (thus increasing the cost and control system complexity). Other options include the use of balancing resistors (which decrease the efficiency) or using, as in the present paper, an unsynchronized gate drive signal technique approach. A sequential gate driver delay (5 µs) on each one of the cells (S_{k1}, S_{C1} to S_{kn}, S_{Cn}) is used on every transition mode operation, similar to the technique adopted on multilevel inverters, but for a short period of time. Figure 3 exemplifies the sequence delay technique adopted for one arm of the inverter to turn OFF S_{M1} and turn ON S_{M2} with $I_L > 0$ and $n = 3$.

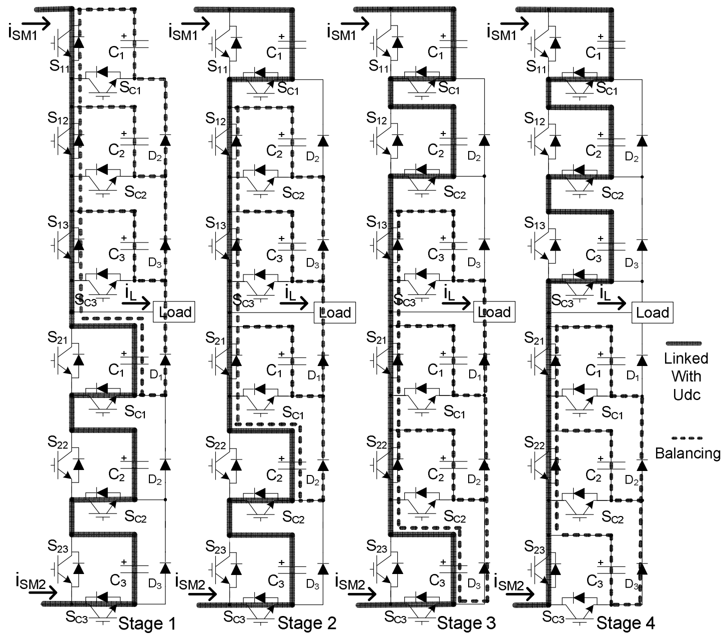

Fig.3. Sequence delay technique for turn OFF S_{M1} and turn ON S_{M2} for $n = 3$ and $I_L > 0$

The sequence delay technique begins at Stage 1 (St1) where the capacitors C_1, C_2 and C_3 of S_{M2} are linked in series with U_{dc}, and at same time C_1, C_2, C_3 of S_{M1} and C_1 of S_{M2} are connected in parallel for voltage balancing. Sequentially, follows the St2, then the St3 and finishes with St4 where the capacitors C_1, C_2 and C_3 of S_{M1} are linked in series with U_{dc} and C_1, C_2 andC_3 of S_{M2} are connected in parallel for voltage balancing purposes. All the states for S_{M1} and S_{M2} for $I_L > 0$ are resumed in Tab. 1.

Table 1. Stages transition for S_{M1} and S_{M2} for $I_L > 0$

Stage	ON at S_{M1}	OFF at S_{M1}	ON at S_{M2}	OFF at S_{M2}	I_{SM1}	I_{SM2}
1	S_{11}, S_{12}, S_{13}	S_{C1}, S_{C2}, S_{C3}	S_{C1}, S_{C2}, S_{C3}	S_{21}, S_{22}, S_{23}	I_L	0
2	S_{12}, S_{13}, S_{C1}	S_{11}, S_{C2}, S_{C3}	S_{21}, S_{C2}, S_{C3}	S_{22}, S_{23}, S_{C1}	$2/3I_L$	$-1/3I_L$
3	S_{13}, S_{C1}, S_{C2}	S_{11}, S_{12}, S_{C3}	S_{21}, S_{22}, S_{C3}	S_{23}, S_{C1}, S_{C2}	$1/3I_L$	$-2/3I_L$
4	S_{C1}, S_{C2}, S_{C3}	S_{11}, S_{12}, S_{13}	S_{21}, S_{22}, S_{13}	S_{C1}, S_{C2}, S_{C3}	0	$-I_L$

To turn ON S_{M1} and turn OFF S_{M2} for $I_L > 0$ there is the need to invert the initial sequence, that is, to operate the stages from St4 to St1. If $I_L < 0$ it is necessary to change the drive sequence, leaving a slightly higher voltage on the C_1 of S_{M1} and S_{M2} in order to guaranty the proper equalization.

3.4 Design Parameters

It is considered that the HV inverter provides energy to a resistive load through one low-pass filter (LC). Also, the system is design for a specific efficiency parameter η_T by assuming P_0 as the nominal output power, P_{LC} the filter power losses and P_{CS} the switches power losses. Since the majority of the losses are due to IGBT switching effects, its relationship with maximum switching frequency and goal efficiency is (2).

$$\frac{1-\eta_T}{\eta_T} = \frac{P_{LC}}{P_0} + \frac{P_{CS}}{P_0} \tag{2}$$

a) The filter is designed to reduce harmonic voltage content. Its contribution to the overall losses shouldn't be greater than 0.3 % of the nominal output power. For a cut-off frequency f_c and a damping ratio ξ the filter parameters are $\omega_0 = 2\pi f_c$, $Z = \frac{2\xi {U_0}^2}{P_0}$, $C = \frac{1}{Z\omega_0}$, where the ω_0 is the angular frequency and Z is the characteristic impedance of the load output. The corresponding filter parameters for the inductance and capacitor values are $L = \frac{\xi {U_0}^2}{\pi f_c P_0}$, $C = \frac{P_0}{4\xi\pi f_c {U_0}^2}$. It is considered that the losses in capacitor are negligible because most of them are due to the output current ripple Δi_L [10]. With r_C and r_L as the equivalent serial resistance of the capacitor and the inductor the power ratio can be calculated (3).

$$\frac{P_{LC}}{P_0} = \frac{r_L P_0}{{U_0}^2} + \frac{r_C \Delta {i_L}^2}{12 P_0} \tag{3}$$

To achieve a specific performance losses criteria r_L should obey the relationship presented in (4).

$$r_L < \frac{P_{LC} {U_0}^2}{{P_0}^2} \tag{4}$$

b) The efficiency of the IGBT is related to the semiconductor ON state and switching losses. The ON state losses P_{C1} are a function of the device ON state voltage U_{ce}, the anti-parallel diode voltage drop U_f and the maximum current output I_0. Assuming one single IGBT and the duty cycle δ', it can be written $P_{C1} = U_{ce} I_0 \delta' + U_f I_0 (1-\delta')$. Considering $\delta' = 1/2$ the total ON losses P_C for the four switches with n cells each is (5).

$$P_C = 2nI_0 \left(U_{ce} + U_f\right) \tag{5}$$

The switching losses P_{S1} are related with the rise time t_r, the fall time t_f, and the switching frequency f_s. Since the IGBT voltage is $U_c = U_{dc}/n$ and I_0 represents its current, in a single device the switching losses are $P_{S1} = U_c I_0 f_s \frac{(t_r + t_f)}{2}$.Taking into account the voltage U_{dc} and the previous equation the total switching losses P_S for the four switches with n cell each are (6).

$$P_S = 2U_{dc} I_0 f_s \left(t_r + t_f\right) \tag{6}$$

Since P_{CS} should be no more than 1.7 % of P_0, so (7).

$$\frac{P_{CS}}{P_0} = \frac{2U_{dc} I_0 f_s \left(t_r - t_f\right) + 2nI_0 \left(U_{ce} + U_f\right)}{P_0} \tag{7}$$

For a specific target efficiency the average switching frequency f_s must obey (8).

$$f_s < \frac{\frac{P_{CS}}{P_0} - \frac{2nI_0(U_{ce}+U_f)}{P_0}}{\frac{2U_{dc}(t_r-t_f)}{P_0}} \quad \textbf{(8)}$$

c) The C_n value on each cell is important to the proper operation of the stack and voltage protection purposes by limiting the *dU/dt*. Additionally, the inductance L_p must consider the *dI/dt* IGBT limitations. Assuming variations of ΔU_C (%) on capacitor nominal voltages, on C_1 to C_n, equations (9) and (10) can be presented. Equation (10) is also function of time delay t_d.

$$L_p = \frac{\Delta U_C \frac{U_{dc}}{n} t_r}{2I_0} \quad \textbf{(9)}$$

$$C_n = \left(\frac{(n-1)!}{n}\right) \frac{t_d I_0}{\Delta U_C \frac{U_{dc}}{n}} \quad \textbf{(10)}$$

It should be noted that the energy stored in L_p boosts the voltage in capacitors C_1 to C_n so a freewheel diode was added.

4 Simulation Results

The circuit presented in Fig. 2(a) was simulated using MATLAB/Simulink considering four HV switches with five cells each, $n = 5$. On the HV inverter output there is a LC filter with a cut-off frequency of f_c = 500 Hz. For other general parameters it is considered $P_0 = 1$ MW, $U_0 = 10$ kV, $R_0 = 100\ \Omega$, $\eta_T = 98$ % and $\Delta U_C = 2$ %. Figure 4(a) presents the inverter output voltage U_L and the voltage U_0 applied to the output resistor R_0.

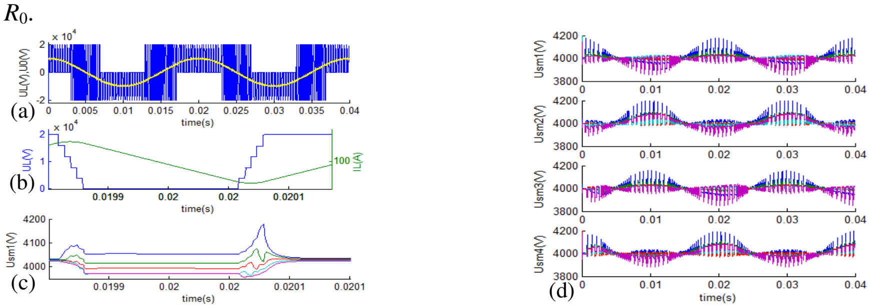

Fig.4. Temporal evolution; (a) voltage output inverter U_L and voltage U_0; (b) voltage U_L and current I_L at output of inverter; (c) voltages cell of switch S_{M1}; (d) voltages present in each cell in all four switches S_{M1}, S_{M2}, S_{M3} and S_{M4}

The capacitor voltages (Fig. 4(d)) are very similar and balanced around 4 kV, even using randomly chosen capacitor values within the typical tolerance of 10 %. In Fig. 4(b) it is shown an improvement of 80 % (for $n = 5$) reduction in the inverter output *dU/dt* regarding the synchronized gate driver technique. The output filter current exhibits smooth transitions around 100 A.

The voltage variation at Fig. 4(c) is higher at C_1 of S_{M1}. At turn OFF there is a voltage increase of 2.5 % relative to its nominal value. At turn ON the voltage in C_1 is 4.5 % higher to the same nominal value. Besides all the voltages sharing is achieved.

5 Conclusion

The full-bridge inverter proposed in this paper uses HV switches based on the Marx generator concept. Marx topology well-known toughness is suited for HV pulsed power or electrical network applications. A good voltage balancing was attained on each switch, with just 5 % difference even using 10 % of tolerance for the capacitors due to the use of just one extra diode (D_n) per cell. This is advantageous as the absence of resistors for balancing or capacitor discharging purposes means an improved efficiency. The inverter output *dU/dt* was also reduced and controlled using the proposed delay time unsynchronized gate drive technique.

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