Design, Fabrication and Testing of Assembly Features for Enabling Sub-micron Accurate Passive Alignment of Photonic Chips on a Silicon Optical Bench

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Abstract. In this paper, we report on passive alignment with sub-micron precision of two photonic chips on a silicon optical bench. An effective design principle to minimize the tolerance chain is presented and applied to a case study. The chips have been successfully manufactured and individual characterization of the chips revealed that all critical dimensions were within or close to specs. Sub-pixel analysis of images of assembled chips showed that a repeatability of 0.3 µm from a single photonic chip to the silicon optical bench can be achieved. Moreover, it was demonstrated that passive alignment features defined in the waveguiding layers are robust enough to function as mechanical endstops.

Keywords: Micro-Assembly, Passive Alignment, Photonics, Flip-Chip, Sub-micron Accuracy, Silicon Optical Bench (SiOB).

1 Introduction

Passive alignment of photonic components is a high-volume assembly method. However, its precision performance relies completely on the dimensional accuracies of the geometrical alignment features. Passive alignment of single mode fibers in V-grooves has been researched for several decades [1]. Accuracies down to 1 µm have been demonstrated [2], which is usually sufficient compared to the approximate 8 µm mode field diameter for a single mode fiber. For chip to chip coupling, the required alignment accuracy can be as precise as 0.1 µm [3]. However, with current passive alignment methods, 0.5 - 1 µm accurate waveguide to waveguide alignment is about the best that can be achieved [3, 4, 5]. Frequently, the more time-consuming alternative of active alignment is used when sub-micron accuracy is required [6, 7, 8, 9].
In this paper, we propose design rules to achieve sub-micron accurate passive alignment. Minimizing the tolerance chain is crucial [10]. The way to do that is to define the alignment features in the same masks, the same layers and the same processes as the waveguides. We report about the application of this principle to the design and manufacturing of such features for 0.1 µm accurate passive waveguide to waveguide alignment for a specific case study. Then, the critical dimensions of the individual chips are characterized. After that, the alignment performance in terms of absolute accuracy and repeatability is evaluated with the aid of image processing.

2 Case study

The object of the case study (figure 1) consists of two photonic chips, flip-chip mounted on a common silicon substrate. An indium phosphide (InP) chip forms the photonic heart of the assembly. InP as a photonic platform offers a wide variety of possibilities for integration of active optical components [11]. The major drawback is, however, the mismatch in spotsize between the InP waveguides and a single-mode fiber. Therefore, an interposer chip named TriPleX [12] is used. Both photonic chips are mounted with their active side facing down (flip-chip) to a silicon optical bench (SiOB) that functions as common substrate. This case study focuses on the passive alignment of the InP chip with respect to the TriPleX interposer. For that purpose the two photonic chips have been equipped with passive alignment features, while the SiOB is populated with corresponding counter features.

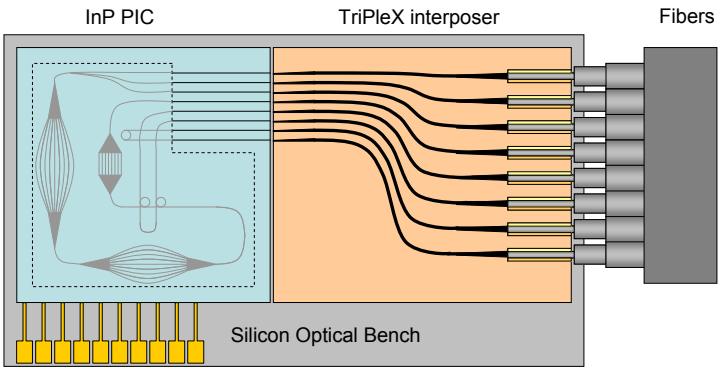

Fig. 1. Case Study

The photonic platform TriPleX (figure 2) consists of a silicon wafer with 8 µm thermally grown oxide. A silicon nitride box was formed on this oxide using one single lithography and several deposition and etching steps . This box is again filled with silicon dioxide. The topcladding is formed by deposited oxide. The effective index of the core can be tuned by changing the nitride and oxide layer thicknesses. The waveguides for this project consist of 550 nm oxide, surrounded by 170 nm nitride.

Different types of waveguides are available for the photonic platform of indium phosphide (figure 2). The type of waveguide as used in this project is a slab waveguide. The undercladding is formed by an InP wafer. The waveguiding layer is created by growing a 550 nm thick InGaAsP layer on top of the InP. The optical modes are confined by an InP layer, which is etched to 2 × 2 µm slabs. The topcladding therefore consists of InP and air. The slabs are 100 nm overetched into the InGaAsP layer.

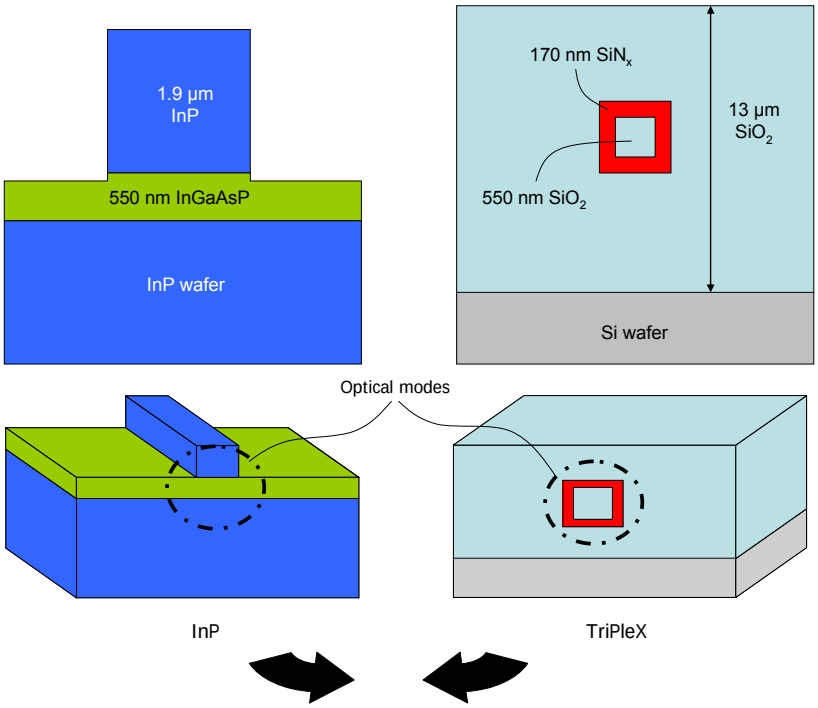

Fig. 2. TriPleX and InP waveguides

3 Design of passive alignment features

Fabricating the passive alignment features on the TriPleX and InP chips was conceived such that they fit the process steps, which already existed for these chips, while the SiOB was designed from scratch.

3.1 TriPleX

As shown in figure 2, a TriPleX waveguide consists of a silicon nitride box, both filled and surrounded by silicon dioxide. The thicknesses of the several layers and therefore the height of the waveguides are more or less fixed. Altering layer thicknesses will change the optical properties of the waveguide. However, the width of these boxes can easily and individually be varied in the mask in order to build passive alignment features within the same layers as the waveguide were made of. One drawback is that the waveguides are buried in the topcladding. Exposing the features therefore requires an additional lithography and etching step. The feature in the TriPleX is shown in figure 3.

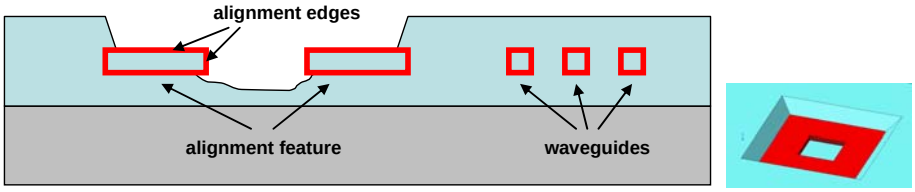

Fig. 3. Design of alignment feature in TriPleX

A surface with a square hole is made out of the same silicon nitride box as the waveguides. The alignment feature will therefore have the same height (thickness) as the waveguides, but is of course much larger in the in-plane (IP) directions.

3.2 InP

The thickness and etch depth of the InGaAsP layer together with the thickness of the silicon nitride pad determine the out-of-plane (OOP) position of the waveguide centre, while the width and location of the InP slab defines the in-plane position. The passive alignment features on the InP chip are made from an InP slab with a concave shape as shown in figure 4.

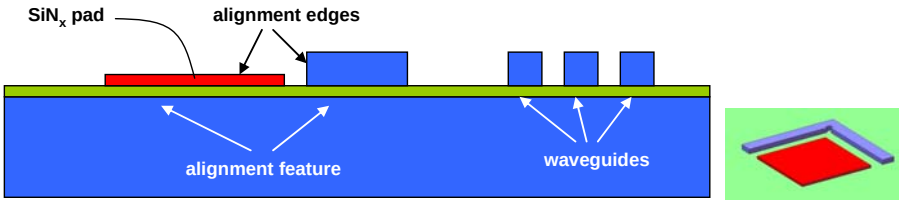

Fig. 4. InP Design

The concave slab assures alignment in the IP directions. For the OOP direction, the positioning is done by a silicon nitride pad with a well defined height. This latter layer requires an additional mask and a few additional process steps.

3.3 Silicon Optical Bench

The SiOB only contains the counter parts of the InP and TriPleX features. The substrate with the two photonic chips assembled on top, is shown in figure 5. The TriPleX counter feature consists of two pedestals with different heights, while the InP counter feature is just one pedestal. For the OOP alignment, it is important that the lower pedestal of the TriPleX counter feature is at the same height as the pedestal for the InP. For the IP alignment, it is essential that the sidewalls of both counter features are accurate with respect to each other, i.e. defined in the same process steps. Moreover, there should be a height difference between the higher tower and the lower tower of 1 – 1.5 µm.

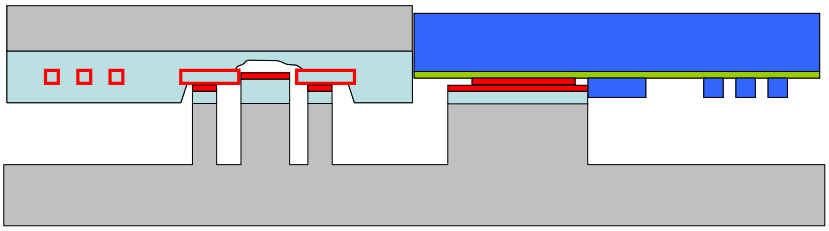

Fig. 5. SiOB design

Processing of the substrate is shown in figure 6. It starts with a normal p-type, prime-grade silicon wafer (1). After making the zero-layer markers, a 4 µm silicon oxide layer is deposited (2). Next, the silicon oxide is etched down to approximately 2.5 µm almost everywhere, except where the higher tower will come (3). Afterwards, the whole wafer is covered with 500 nm thick silicon nitride (4). Now, the lower tower and the final shape of the higher tower are patterned (5). To do so, a 6 µm resist coating is applied, because it will also be used for the next step. The oxide and the nitride are etched. Overetching is not a problem, since it will be immediately followed by etching 65 µm Si by means of the Bosch process (6) that uses the same mask and the same resist.

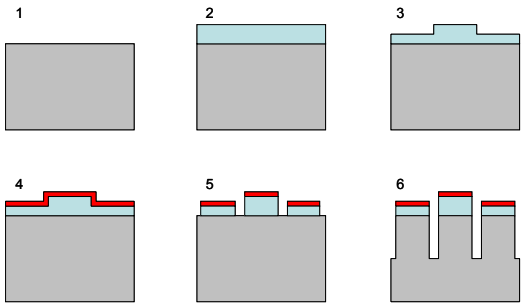

Fig. 6. SiOB manufacturing steps

4 Manufacturing Results

Directly after manufacturing and dicing, the alignment features were inspected with scanning electron microscopy (SEM). An SEM image of the manufactured TriPleX features as well as the corresponding SiOB counter feature is shown in figure 7. The alignment features of the TriPleX chip are positioned near the edge of the chip. Hence, the surface of the SEM sample holder is also visible on the picture. The edges of the inner hole are used to align against, while the outer hole was necessary to expose the feature itself, since TriPleX waveguides are buried in the cladding. For the SiOB counter feature, the inner and outer tower are visible. The height difference between the towers as well as their nominal height are important.

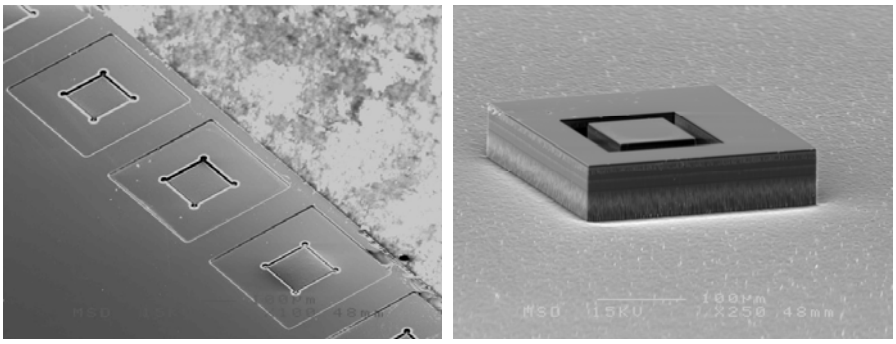

Fig. 7. SEM image of the TriPleX alignment features (left) and the SiOB counter feature (right)

Figure 8 shows an SEM image of the InP features together with an array of waveguides as well as the corresponding SiOB counter feature. The dark square on the left picture is the 250 × 250 µm silicon nitride pad needed for out-of-plane alignment. Above and to the right of the pad, a 50 µm wide and 2 µm high InP slab is visible. This slab takes care of the alignment in the in-plane directions.

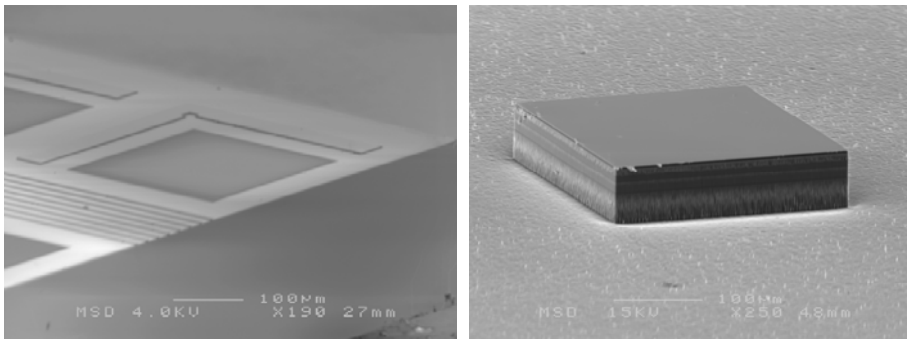

Fig. 8. SEM images of an InP alignment feature (left) and the SiOB counter feature (right)

Secondly, the critical features and dimension of the chips (figure 9) were individually characterized by means of atomic force microscopy and white light interferometery. The results are listed in table 1. It can be concluded that all critical dimensions were manufactured within specifications, except for one (parameter *d* in the table, representing the SiN_x layer thickness on the InP chip). This deviation will result in a systematic misalignment of 85 nm in the out-of-plane direction.

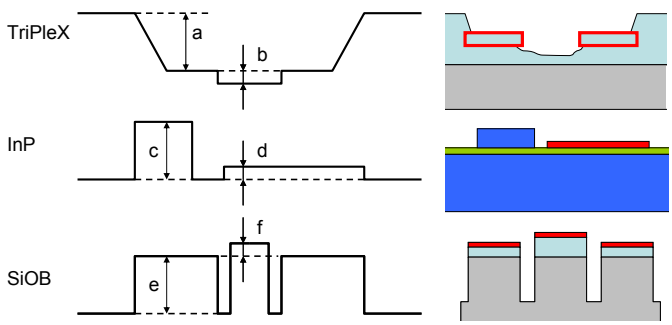

Fig. 9. Schematic overview of the critical dimensions in the several chips

Table 1. Measurement of critical dimensions

Chip	Critical Dimension	Required value	Measured value	Measurement method
TriPleX	a	none	5 µm	AFM*
	b	> f	2 µm	AFM
InP	c	1.9 µm	1.9 µm	WLI**
	d	245 nm	330 nm	AFM
SiOB	e	50 – 70 µm	65 µm	WLI
	f	< b	1.1 – 1.7 µm	WLI

* AFM = Atomic Force Microscopy
** WLI = White Light Interferometry

5 Assembly results

After having individually characterized both the TriPleX and the InP chip, they were assembled on the SiOB, which was monitored with a video camera. Initially, the SiOB was placed on a holder in the field of view of the camera. Then, the TriPleX or InP chip was placed upside-down (flip-chip) on the SiOB, after which it was gently pushed towards its respective intended position. Afterwards, image processing was used to compare the actual position of the chips with there nominal intended positions (figure 10).

At this stage of research, repeatable assembly was achieved only with the InP chip. (See discussion). Therefore, further image analysis has been conducted solely with the InP chip.

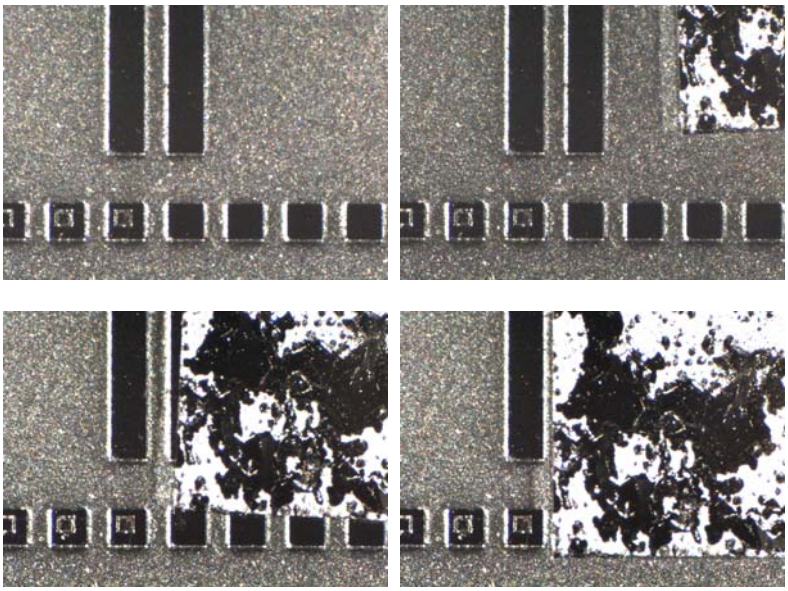

Fig. 10. Assembly sequence of the InP on the SiOB. One such square, black-colored alignment feature measures 400 × 400 µm.

Image analysis with Matlab was performed to compare the InP's final position with its nominal position. The assembly shown in figure 10 was repeated several times with the same chips. 9 out of 9 times, the edges of the InP chip were exactly found at the intended pixels or position respectively. This proofs that an edge of no more than 2 µm high can be used as a mechanical endstop. However, since one pixel represents about 3.4 µm, an absolute positioning performance more accurate than 3.4 µm cannot be concluded from just these images. Therefore, also the relative positioning of the InP chip (i.e. repeatability) was evaluated with sub-pixel analysis, the method described below.

First, two clearly distinguishable features were identified; in this case the edge of the chip and the edge of an alignment feature (figure 11a). At the edge of the alignment feature, the grey-value changes suddenly from white (255) to black (0) (figure 11b). A similar transition can be observed at the edge of the chip. The edges are then arbitrarily defined at the location where it has a specific grey-value (chosen threshold value of 150 in our case). This interpolated position is computed for a large amount of rows along both edges, resulting in the distribution shown in figure 11c. This computation is repeated for all 9 pictures or experiments resp. and the mean value for every experiment is taken. These mean values finally define the deviation between the several pictures, i.e. the repeatability of the assembly (figure 11d). From this graph, it can be concluded that the assembly is repeatable within ±0.09 pixel, which corresponds to about ±300 nm.

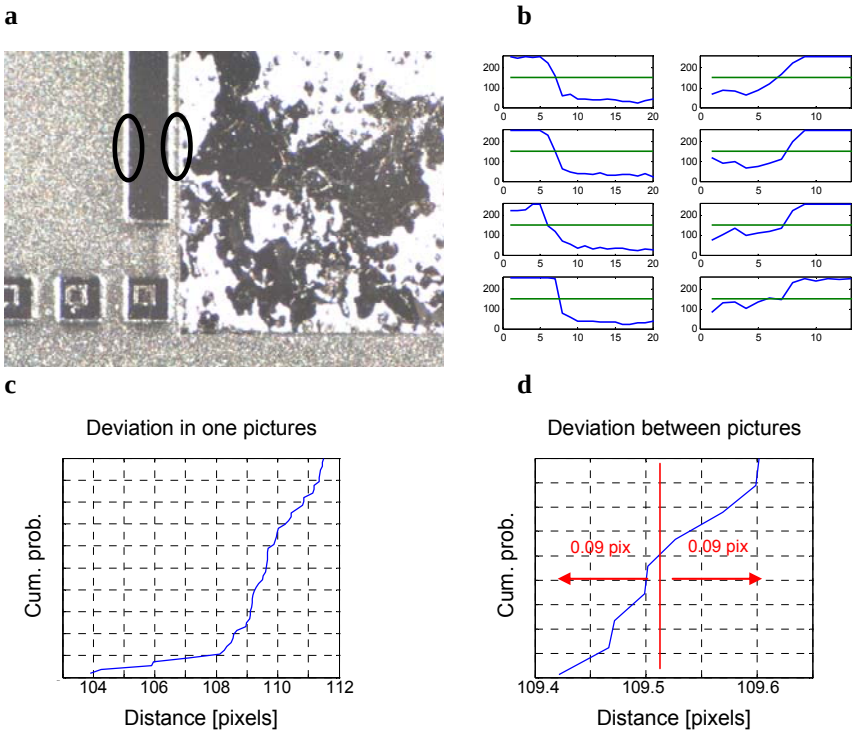

Fig. 11. Sub-pixel analysis of assembly performance

Due to the rather large variation in grey-scale intensity on the surface of the InP chip, the edge of the InP chip was difficult to define by the method described above. Figure 15 top-left already indicated that there was only a small part of the vertical edge suitable for this analysis. For the horizontal edge, however, it appeared impossible to find a clearly defined edge of sufficient length, most probably caused by the illumination direction. Therefore, the analysis has not been conducted along the horizontal edge.

6 Discussion

Based on various measurements during and after the manufacturing of the individual chips, it was concluded that all critical dimensions of the alignment features were manufactured within specs, except for the thickness of the nitride layer on the InP chip. It is 330 nm thick, while it should have been 85 nm. This gives a systematic error (misalignment) of 85 nm in the out-of-plane direction.

The assembly of the TriPleX chip on the SiOB was unsuccessful in the sense that the TriPleX chip did not always end on the intended position. In many occasions, the TriPleX chip hits its counter feature not with the edge of the square silicon nitride “donut”, but with the edge of the exposure hole instead. This effect can be prevented

by performing a more accurate initial placement of the chip. While the initial placement of the InP chip was found to be not critical, the TriPleX chip should be placed coarsely within ±20 µm before pushing it towards its endstops.

The assembly of the InP chip was successful in 9 out of 9 trials. Every time, the edges of the chips were found at the intended pixels. However, since one pixel covers 3.4 × 3.4 µm in the object plane, the absolute positioning could not be verified to an accuracy of better than 3.4 µm. The alignment itself is probably more accurate, but it can just not be concluded from these images. Moreover, we have looked at the edge of the chip, which is not very accurately defined with respect to the actual waveguides on the chip. Therefore, the absolute alignment performance will be evaluated by means of optical coupling measurement in the near future.

Nonetheless, the relative positioning, or the repeatability, can be evaluated more accurately by means of sub-pixel analysis. It turned out that the InP chip was positioned within ±0.3 µm every time. Although it is worse than the intended 0.1 µm, it is considered promising. So far, the chips have been pushed against their end stops with a pair of tweezers. Positioning the chips with vacuum chucks mounted on an xyz-stage is likely to yield an even better repeatability. Unfortunately, the sub-pixel analysis could only be conducted in one direction due to the image quality. Nonetheless, the alignment feature for the other in-plane direction is exactly the same and there is therefore no reason to assume any different performance.

The alignment in the out-of-plane direction is also very important. Due to the limitations of the assembly setup, it was not possible to evaluate the performance in this direction. This can be done by measuring the optical coupling [4].

7 Conclusion

This paper reports on the design, fabrication and testing of assembly features for sub-micron accurate passive alignment of photonic chips on a silicon optical bench. From the various results and discussions, the following conclusions can be drawn.

First of all, the alignment edges on the various counter features on the SiOB could be manufactured within the same lithography and etching steps as the actual waveguides. Also, it was demonstrated that edges being not more than 2.0 µm high can be used as mechanical endstops for passive alignment. This proofs the principle that it is possible to create sufficiently robust and reliable alignment features in the same lithographic and etching steps as the waveguides. Furthermore, an absolute positioning accuracy (in-plane) of at least 3.4 µm (1 pixel) of the InP chip with respect to the SiOB was achieved. Finally, an in-plane position repeatability of 0.3 µm for the InP chip on the SiOB was achieved.

Acknowledgements

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