Parallel Packaging of Micro Electro Mechanical Systems (MEMS) Using Self-alignment

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Abstract. Packaging is one of the major cost drivers for MEMS devices. Currently wire bonding is the dominant method for electrically connecting MEMS chips to substrate. Using self-alignment a method for packaging multiple MEMS at the same time has been developed. The presented process achieves high throughput and precise alignment at low cost. The Controlled Collapse Reflow Chip Joining (C-4) process has been adapted to the specific requirements of MEMS. The combination of coarse robotics and liquid solder self-alignment guarantees precise positioning and alignment of the individual MEMS chips to the respective substrates. The new method has been implemented in a case study. In the study force sensors have been packaged. Precise angular alignment of the sensors is critical for receiving accurate measurements. Results of the case study are presented.

Keywords: flip-chip, C-4, self-alignment, MEMS, MOEMS, no clean, force sensor, solder paste, bismuth, FemtoTools, wafer level packaging, WLP, chip scale packaging, CSP, direct chip attach, DCA, DRIE, SOI

1 Introduction

A large part of MEMS manufacturing costs (60% to 80%) originates from packaging [1, p. 6]. This work deals with reducing these costs. In particular a novel bonding method is presented.

The bonding methods used in MEMS are largely adopted from the integrated circuit (IC) industry. This comes as no surprise since these methods have been highly optimized, are well understood by chip foundries and, furthermore, have been certified for various uses. In fact, MEMS devices are often produced on depreciated CMOS manufacturing equipment. While *Controlled Collapse Reflow Chip Joining* (C-4) or *flip-chip* [2] has seen widespread adoption in IC packaging, this is not the case in MEMS packaging. Here *wire bonding* is still largely preferred. This is due to several factors: Wire-boding is a flexible technology that is easy to adapt to new designs. It is easier to reduce shear stress caused by thermal expansion mismatch (TEM)

when using wire bonding. Finally, flip-chip cost savings increase with pin count. [3] However, most MEMS devices typically have a low pin count. By using wire-bonding, MEMS devices cannot take advantage of C-4 characteristics such as:

- Free placement of pads resulting in excellent space utilization (up to chip scale packages (CSP)).
- Shorter connections leading to better electrical performance (low inductance and resistance of connections) and excellent thermal performance.
- No separate mechanical fixation.

This work presents a way to use C-4 in MEMS packaging. The C-4 process is adapted to the specific properties of MEMS devices. By doing so it becomes possible to package multiple MEMS devices simultaneously with a single machine. The number of devices that can be packaged in parallel is only limited by the ratio of substrate space to device space and the size of the device wafer. The novel method also *reduces the precision requirements* of the pick and place robotic manipulator. The above improvements are achieved by relying on liquid solder surface forces causing chip and substrate to *self-align*.

Attempts to assemble individual micro devices in parallel generally rely on one of two approaches:

- a *deterministic* one requiring multiple manipulators and sensory feedback (thereby being very similar to the multiplication of serial processes),
- or a *stochastic* one relying on self-assembly which offers low equipment costs but severely limits the size and complexity of the parts that can be assembled [4,5].

The approach presented in this paper combines the advantages of both: It has the deterministic properties of the robotic placement of the chips while not requiring multiple manipulators. It uses classical robotics for coarse positioning and self-alignment for the precise positioning that is required for many MEMS and MOEMS.

2 Parallel C-4 Bonding

In the C-4 process substrate and chip have a matching array of solder bumped contact pads. During the assembly the chip is flipped upside-down and placed at the desired position on the substrate. The solder is liquefied and bridges the facing pads. When the solder cools down, lasting *mechanical* and *electrical* connections are formed. Due to the flipping operation this process is often referred to as a *flip-chip* process. [2] Currently a parallel C-4 process is not feasible since each chip needs to be precisely aligned to a substrate. The combined use of deterministic and stochastic assembly methods presented in this work lowers that requirement.

2.1 Process Overview

Our process also relies on solder bump joining. One of its essential features is that the chips are not flipped, however. Instead they are connected to the substrate when

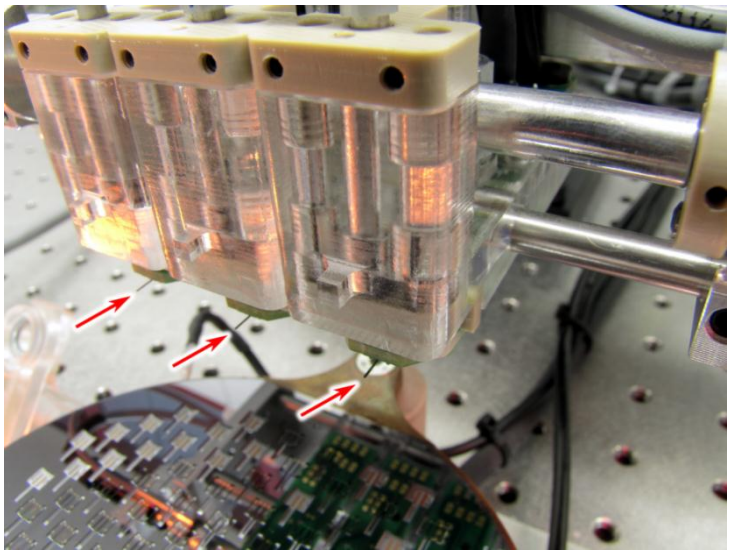

Fig. 1. On the bottom the wafer table is depicted. Above that identical substrate holding devices that are attached to a robotic actuator are located. The arrows are pointing onto the measuring tips of three MEMS chips that have just been separated from the wafer. The separation of the MEMS chips from the wafer is assisted by suction needles that are reaching through the substrate.

they are already separated from the wafer (by means of dicing or etching) but still located at their original position. A robotic manipulator places several substrates above the wafer. The substrates are spaced out at an interval matching the spacing of chips in the wafer or a multiple thereof. As the robotic manipulator lowers the set of substrates, the corresponding pads of substrate and chip are connected through the liquefied solder. The substrate is then lifted pulling the chips along. Once the chips are free hanging the surface forces of the molten solder will work towards minimizing the distance between matching pads and align the chips (see fig. 1).

Maximum alignment precision can be achieved by adding differently sized (not necessarily electrically connected) pads on substrate and chip as suggested by [6,7].

2.2 Required robotic precision

Assuming that the solder bumps form a spherical shape when molten, the maximum placement precision required is half the size of the solder pad diameter. Once the solder wets, surface forces finely align the pads and, thereby, the MEMS chips.

2.3 Space saving

MEMS chips typically require very few electrical connections. The individual pads can be larger and more spread out than the ones found on ICs. Since they can be placed freely on the chip, little chip real estate is lost. Because the pads on the sub-

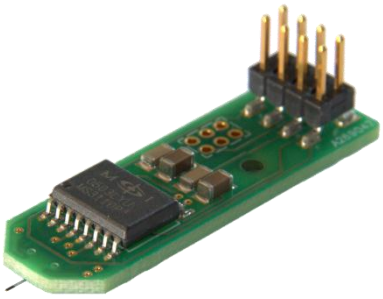

Fig. 2. FemtoTools FT-S260 force sensor

strate are placed underneath the chip rather than around the chip, the total package size can be reduced compared to wire bonding in most cases.

3 Case Study

The invented method was verified in a case study. A demonstrator was built to bond FemtoTools FT-S260 force sensors (see fig. 2) to substrates. The chip is directly attached (DCA) to an organic substrate. The substrate is an FR-4 printed circuit board (PCB). Apart from the MEMS chip the PCB additionally contains readout electronics. For the final device to produce accurate measurements it is essential that the sensor is exactly orientated with regard to the substrate.

The sensor is manufactured from a Silicon on Insulator (SOI) wafer using reactive ion etching (RIE) and deep reactive ion etching (DRIE) processes. Because the force sensor must directly contact its environment, it does not receive protective packaging. The transducer fabrication process does not require dicing of the wafer. Instead the device wafer is placed on a support wafer. During the etching process the individual chips are completely separated from the device wafer. The chips can move freely in a 200 µm gap created by the etching process, and their *precise position is no longer defined*. The chip as well as the substrate feature square pads with a side length of 380 µm. The maximum diagonal distance between pads is 3.6 mm.

The force sensor chip converts the force to be measured into a deflection using elastic flexures. The deflection is detected by two capacitor electrode arrays (differential comb drives). Liquid coming into contact with the comb drive electrodes will cause the electrodes to permanently stick together. Flux cleaning solutions can, therefore, not be used. [8]

Prior to this work the devices have been manually wire bonded. The pad layout of the chip and substrate were slightly modified for the new process to maximize self-alignment torque and to balance chip support.

Before being assembled the individual devices are in-wafer tested for defects using the resonance method described in [9]. Only known good dies (KGD) are assembled.

In the demonstrator implementing the described method, batches of only three devices[1] are bonded at a time. This keeps machine and tooling costs low while still proving the viability of the approach.

3.1 Under Bump Metallurgy (UBM)

The pads and traces on the substrate are made of copper. The pads are plated with 3-6 µm of nickel and 50-150 nm of gold. The contact pads of the MEMS chip are also gold plated (200 nm) to prevent oxidation and guarantee good solder wettability. The adhesion layer consists of 10 nm of titanium.

3.2 Solder

The solder used in this flip chip application has to fulfill several requirements:

1. It has to be soft enough to limit the stress exposed on the contact pads and thereby the MEMS chip.
2. The melting point has to be lower than that of the solder used to assemble the other parts on the substrate. The other components are assembled to the PCB first, since the sensor is the most fragile part. A low melting point also reduces the stress that results from the mismatch of coefficients of thermal expansion (CTE) during the cool-down after the assembly process.
3. Since the precise alignment of chip and substrate is achieved by self-alignment, the solder has to provide large surface forced in the liquid state.
4. It has to wet the contact pads well.

A solder paste containing the eutectic Bismuth (46 wt.%), Tin (34 wt.%), Lead (20 wt.%) alloy (Indium Technology Indalloy 42) was selected for this work. It features a melting point of 96°C. According to Indium Technology, the maximum operating temperature of the solder is 90% of the absolute melting point temperature [10]. In the case of the alloy used this is 59°C. Flux contained in the solder paste guarantees good wetting of the pads and removes the need for cleaning of the pads or a controlled assembly environment.

Gold embrittlement. The large amount of tin contained in the solder leads to high surface forces in the liquid state. However, it can create an intermetallic bond with the protective gold layers of the contact pads. This in turn tends to accelerate solder joint fatigue. To prevent this from occurring, the thickness of the gold layer has to be limited to approximately 380 nm. [11]

[1] When there are not enough devices left in a row, or chips have found to be faulty during in-wafer testing, fewer devices are bonded in one batch.

3.3 Process Steps

Solder dispensing. Due to the relatively large pads used it is not necessary to use expensive solder bumping methods such as vacuum metallization to obtain tinning of the chips' contact pads. Instead, solder paste is dispensed onto the substrate prior to the actual assembly taking place. For batches of significant size mask printing of solder paste is feasible.

Wafer Registration. The wafer is placed onto a holding device. The position of the devices is not necessarily well defined with regard to the wafer. Two alignment marks are located by a custom image processing system [12]. Relative to the marks the position of each chip contained in the wafer is known.

Pre-Heating. The wafer holding mechanism contains a closed loop heating system that pre-heats the wafer to a temperature slightly below the melting point of the solder. This reduces the time required to heat the individual chips.

Heating and Chip Pick-up. A robotic manipulator moves an array of substrates to a position above the wafer with the corresponding substrate and chip pads coarsely aligned. The solder on the substrates' pads is liquefied by heating and then brought into contact with the pads of the chips. Once the chips' pads are wetted, the substrate is lifted again pulling the chips along. Depending on the weight of the chips, their adhesion to the wafer, the geometry and number of the solder pads and the surface tension of the solder, the lifting forces exerted by the solder may not be sufficient. This has been observed in the case study. To produce the forces required to achieve separation of the chip from the wafer, retractable vacuum pipes reaching through holes in the substrate have been introduced. These vacuum pipes are retracted as soon as the chip is separated from the wafer and the solder is molten.

Self-Alignment. Substrate, the free hanging chip and solder are heated in a temperature controlled way. Once the solder is molten and the chips are free-hanging, self-alignment takes place. When this is completed the device is cooled down and lasting electrical and mechanical connections are formed.

4 Results

The demonstrator is operational and has produced several batches of devices (see fig. 3). The devices have been functionally tested and perform as desired. The selected low-temperature solder as well as the relatively large height of the solder connections guarantees a level of shear stress that does not impact the performance of the sensor.

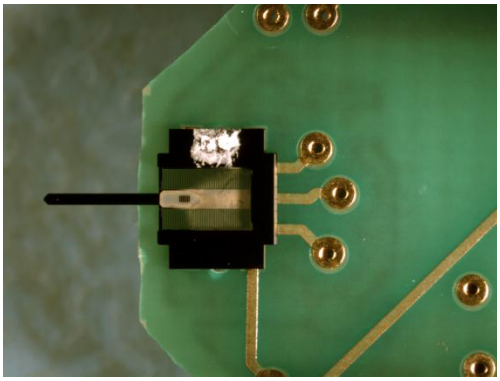

Fig. 3. Assembled device. The white spot on the chip is an artifact of chip production.

One of the critical points of this assembly method was the flux reaching comb drive, leading to the destruction of the device (see section 3). This has not been observed for any of the manufactured devices.

Shear tests on the devices have shown the connection to withstand a force of up to 10 N. These measurements, the good electrical connections and cross sections (see fig. 4) demonstrate good wetting of the contact pads. The alignment of the chip to the substrate is within the specification of FemtoTools.

Cycle time of the assembly is 18 s per batch of three devices. While this compares favorably with manual wire bonding (15 s per device for wire bonding alone, e.g. excluding mechanical fixation), it is not exceptionally fast. However by increasing the batch size (by means of additional substrate holders), the throughput can be increased substantially. For the devices used in this case study the theoretical minimum assembly time per device is below one second. This could be drastically improved by switching to a larger wafer or smaller substrate. However, this has not yet been experimentally verified.

5 Conclusions and Outlook

This work presents a method providing high-throughput and precise-placement packaging of MEMS at low cost. The method requires only limited changes to existing MEMS designs. By building on C-4 technology many of the potential advantages become available to the MEMS designer: chip scale packaging (CSP), stacking of MEMS and electronics chips, improved electrical and thermal performance are just some of them.

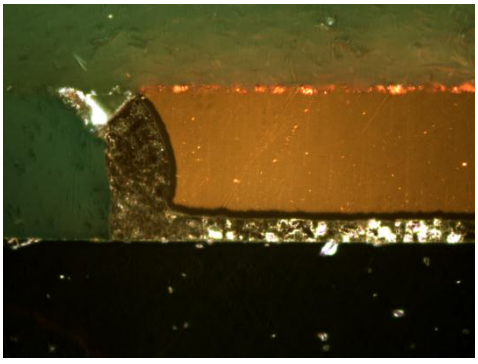

Fig. 4. Micrograph of a cross section through a solder connection The PCB is located at the top, the MEMS chip on the bottom.

The presented method also features properties that may prove beneficial to new designs. Contrary to regular flip chip approaches the MEMS chip is handled from one side only. This gives the chip designer the option of placing very fragile structures on most of the underside of the chip. Owing to the parallel processing of the assembly, good throughput can be achieved at relatively low handling acceleration. This can be desirable for very sensitive devices.

Due to tooling requirements, the cost of a machine implementing the bonding method will highly depend on the amount of parallelization chosen. The manufacturer can select the appropriate amount of parallelization to match the desired throughput. This significantly reduces the cost for producing small to medium size batches as found in specialized devices.

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