Design of Robust CMOS Amplifiers Combining Advanced Low-Voltage and Feedback Techniques

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Fábio Januário and João Goes

Centre for Technologies and Systems (CTS) - UNINOVA
Dept. of Electrical Engineering (DEE), Universidade Nova de Lisboa (UNL)
2829-516, Monte da Caparica, Portugal
S.Abdollahvand@ieee.org

Abstract. This paper describes and tries to demystify the use of different low-voltage operation devices, such as dynamic threshold MOS transistors (DTMOS) with feedback techniques such as regulated-feedforward (RFF) and self-biasing (SB). Traditionally, DTMOS devices are only used when nominal supply voltages below 0.7 V are envisaged. Moreover, RFF and SB techniques are normally avoided since engineers designing high-performance amplifiers are afraid of additional stability concerns. This work demonstrates, through exhaustive simulation results over process, temperature and supply (PVT) corners using a standard 130 nm 1.2 V CMOS technology that, employing DTMOS in some specific devices can improve some performance parameters such as the open-loop low-frequency gain and, simultaneously, reduce significantly the variability over PVT corners. Moreover, it is also demonstrated that, there is no risk of operating at supply voltages higher than 1.2 V. Combining DTMOS with RFF and SB allows achieving reasonable gain-bandwidth products (GBW) even operating at low-voltage (down to 0.7 V), together averaged power savings of the order of 8% and highly simplifies the design of the circuit (since no biasing circuitry is required).

Keywords: Operational transconductance amplifier; Single-stage amplifiers; Fully-differential; DTMOS; Self-biasing; Regulated-feedforward.

1 Introduction

There has been an ongoing tendency in lowering the operating supply voltages in analog and mixed-signal circuits, mainly due to reliability reasons (e.g., to prevent gate oxide breakdown) in the continuous downscaling of transistors' feature size in nanoscale CMOS technologies. This tendency is equally justified by the need of low power dissipation circuits for longer lasting battery-powered systems. These systems usually integrate complex building blocks such as analog-to-digital converters and continuous or discrete-time analog filters. Additionally, these blocks usually require amplifiers for the signal processing in voltage mode, which tend to be the most power-hungry circuits of the entire system and the most difficult to design. Hence, for

decades, amplifiers have been one of the most active research areas in the broad field of electronics [1].

Multi-stage amplifiers can achieve high DC gains by cascading several common-source stages. However, they suffer from reduced efficiency and higher noise, since they require proper compensation. In single-stage operational transconductance amplifiers (OTAs), higher DC gain is usually achieved at the expense of using cascode devices to increase the output impedance (r_{out}). The gain-bandwidth product, GBW (usually a requirement: achieve high GBW), is given by GBW(I) ≈ $gm_{1,2}(I)/C_L$, where $gm_{1,2}$ represents the transconductance of the input differential pair, C_L, the compensation capacitance, and I, the biasing current of the input stage. Admitting that the opamp is biased with constant current, I, and with C_L being mainly defined by the application, then, one way of achieving higher GBW relies on using an inverter structure in the input stage. This type of input stage, if properly sized, effectively doubles the transconductance, for now $gm_{1,2} = gm_{1P,2P} + gm_{1N,2N}$, where $gm_{1P,2P}$ and $gm_{1N,2N}$, respectively, represent the transconductance of the PMOS and NMOS transistors that constitute the inverter structure. Therefore, all OTAs throughout this paper rely on the fully-differential single-stage inverter-based folded-cascode topology.

Fig.1 shows the inverter-based folded-cascode amplifier (FCA) used as the reference circuit. The core of the amplifier is made of devices M_1-to-M_{11}. Input inverters are implemented with devices $M_{1P,2P}$ and $M_{1N,2N}$. M_3-to-M_6 are the common-gate (cascode) devices. As in telescopic-cascode and in mirror-cascode OTAs, the FCA also requires a biasing circuit comprising many transistors (M_{B1} to M_{B7}).

One possible technique improve OTA performance at nominal voltage consists on removing the body-effect (BEF), in some specific devices in which the source (S) is at a different potential of the body or bulk (B) terminal. A first commonly used possibility is to short both terminals, i.e., connect the B terminal to the S one, rather than to V_{SS} or to V_{DD}, respectively for an NMOS or a PMOS device. A much more interesting approach consists of implementing a dynamic-threshold MOS device (DTMOS). This can be achieved very easily, only by connecting the B terminal to the gate terminal (G).

A second powerful approach that can be used to improve performance and reduce both, area and power dissipation, consists in removing completely the biasing circuitry. This idea basically relies in two combined techniques, namely regulated-feedforward and self-biasing techniques. Any feedback network always introduces a delay during the voltage regulation process [7]. If this time delay is reduce by employing regulated-feedforward, it becomes possible to significantly increase its operating speed [7]. Additionally, the advantages of employing self-biasing techniques are also well known [6]: 1) they simplify the implementation of amplifiers by removing biasing circuitry, thus saving power and die area; 2) any mismatches and variations in circuits performance due to deviations in biasing voltages are highly attenuated; 3) they enable circuits to be more insensitive to process, supply voltage, and temperature (PVT) variations [1], [9].

In this paper we study, simulate and compare the improvements obtained when using, either separately or combined, standard MOS transistors configured as DTMOS devices and regulated-feedforward and/or self-biasing techniques. For comparison purposes, the three techniques are demonstrated using the original 'case-study' FCA shown in Fig. 1. Section II briefly points out the contributions of this work for value creation. Section III presents the different techniques and it describes how they should

be implemented in the original FCA. Section IV presents the electrical simulation results obtained by combining the different techniques. Finally, in section V, a performance comparison among the different proposed topologies is carried out and the main conclusions are drawn.

2 Contribution to Value Creation

Electrical engineering orientation is toward value creation such as generating new knowledge, converting knowledge to the innovation with commercial value. The widely use of amplifiers in wireless communication equipment has motivated analog circuit designers to reduce the power consumption of the equipments in order to reduce the cost of energy. The low voltage, low power value which offer by designing a novel amplifier with DTMOS and feedback techniques is an effort for value creation.

3 Low-Voltage Techniques

3.1 Considerations of using DTMOS

Low voltage operation has been relying on the scaling down of CMOS technology. During the technology progresses to the nanometer era, the progressive reduction rate of the threshold voltage of the MOSFET devices is slower than the down scaling of the power supply. Therefore, the low power operation deteriorates the propagation delay and signal amplitude [2] and, consequently, the operation speed of digital circuits is degraded [3]. The DTMOS device becomes more beneficial for low power operation at very low voltages [4].

Most of the advanced deep nanoscale and standard CMOS technologies provide separate source, drain, gate and body contacts either for PMOS or NMOS devices (in this last case, normally the process has a deep-NWELL or a triple-well option). To operate as a DTMOS device, the MOS transistors should have their floating body and gate terminals tied together. This is not a new configuration as [2-5] have already suggested it. However, either they have tried to avoid the effect of the parasitic lateral bipolar transistor (supplying the circuit with a voltage below 0.6 V) or they even have exploited the extra current produced by this parasitic device. The first idea we propose in this paper is entirely different. Since the FCA amplifier (as well as the other single-stage cascode topologies) have always four devices in stack, if DTMOS is used only in the input and in the cascode devices, the amplifier can be safely supplied with a nominal supply voltage of 1.2 V and the body voltage of the devices configured as DTMOS never exceeds 0.6 V (the voltage required to activate the bipolar parasitic device).

Fig. 2 shows the modified FCA shown in Fig. 1 after employing DTMOS techniques in both, input ($M_{1P,2P}$ and $M_{1N,2N}$) and in the common-gate transistors (M_3-to-M_6). There are several advantages when doing this: 1) in DC, the BEF of the

modified devices is highly reduced since the threshold voltage of a given DTMOS transistor is properly adjusted taking into account the gate voltage (notice that for all devices in which we propose to use DTMOS, there is almost no signal swing at the gate terminal, if we assume that the amplifier will always be used in inverting configuration); 2) Since the threshold voltage is reduced, the device can be sized smaller for a given V_{DS} saturation voltage, which translates in smaller area and lower parasitic capacitances; 3) In small-signals (AC) the parasitic body-source transconductance (g_{mb}) adds with the main transconductance (g_m). Hence and, as stated before, since the GBW product of a single-stage amplifier is proportional to the main transconductance(s) of the input device(s), employing DTMOS can lead, for the same power dissipation, to speed enhancements in the GBW of the order of 20-to-25% (depending on how much the BEF is attenuated). Moreover, since DTMOS is also used in the common-gate (cascode) devices, the non-dominant poles (defined by the time-constants at the sources of these devices) also are pushed into higher frequencies leading to a more stable amplifier.

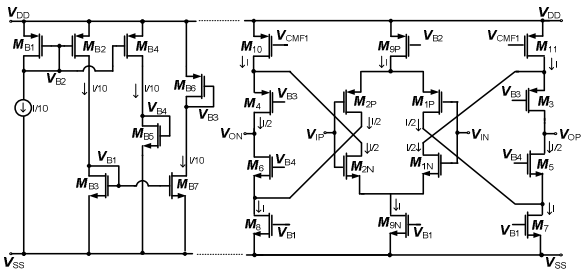


Fig. 1. Proposed inverter-based single-stage folded-cascode OTA (FCA).

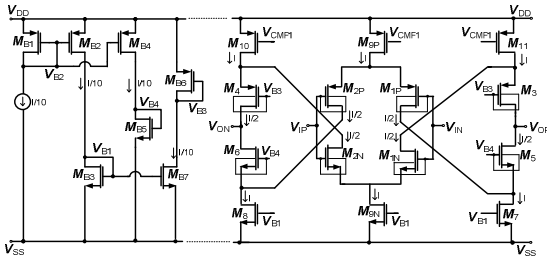


Fig. 2. Proposed inverter-based single-stage FCA employing DTMOS in the input and cascode devices.

3.2 Using Regulated-Feedforward and Self-Biasing Techniques

In amplifiers, self-biasing techniques have been mainly applied to complementary folded-cascode and single stage inverter-based topologies [6]. Fig. 3 shows a proposed modified amplifier that employs, simultaneously, regulated-feedforward (RFF) and self-biasing (SB) techniques [7]. This modified FCA amplifier (FCA + RFF + SB) adds an interesting feature which is self-biasing. The advantages of amplifier self-biasing techniques are well known [6]: 1) they simplify the implementation of amplifiers by removing all biasing circuitry, thus saving power and die area (notice that the modified FCA in Fig. 3 is much simpler than the original FCA shown in Fig.1;

2) any mismatches and variations in circuits performance due to deviations in biasing voltages are highly attenuated; 3) they enable circuits to be more insensitive to PVT variations [9], [1]. This circuitry is similar to the circuitry shown in Fig.1 but without the biasing circuit and with regulated-feedforward technique.

In cascode OTAs using regulated common-gate devices through negative feedback (usually called "regulated-cascodes"), the feedback network always introduces a delay during the voltage regulation process [7]. In the circuitry shown in Fig.3, is used instead a regulated-feedforward approach (a sort of adding a small amount of positive feedback) to diminish time delay in the regulation of the common-gate devices and, thereby, significantly increase its operating speed [7]. It has differential inputs and differential outputs, which allows the circuit to be used in both positive and negative feedback system configurations [7].

A fourth modified FCA amplifier is shown in Fig.4. It is precisely the same as the one depicted in Fig.3 but now using also the DTMOS technique (used in the FCA shown in Fig. 2) in both, input ($M_{1P,2P}$ and $M_{1N,2N}$) and in the common-gate transistors (M_3-to-M_6).

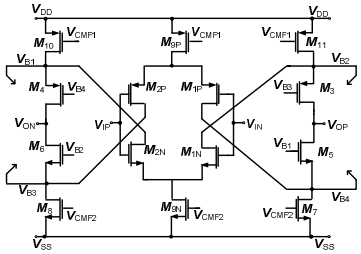


Fig. 3. Proposed inverter-based single-stage FCA employing RFF and self-biasing (SB).

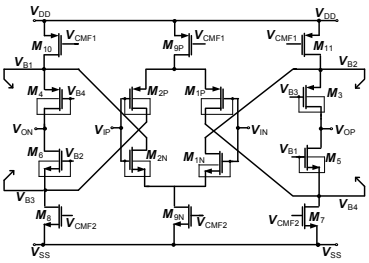


Fig. 4. Proposed inverter-based single-stage FCA combining RFF with self-biasing (SB) and using also DTMOS devices.

4 Simulation Results When Combining the Different Techniques

All four amplifiers have been carefully optimized and designed targeting a 0.13-µm 1.2V CMOS technology (L_{min} = 0.12 µm). Only standard-VT devices have been used. For comparison purposes, the four amplifiers have been sized to achieve, in nominal conditions (V_{DD} = 1.2 V, T = 27 ºC and typical process, TT), a low-frequency (DC) gain $A_d \geq$ 60dB and a gain-bandwidth product GBW $\geq$ 50 MHz while minimizing the total power dissipation.

Fig. 5(a) shows the simulated DC gain for different positive (V_{DD}) supply voltage conditions (ranging from 0.4 V to 1.5 V), for the conventional FCA (Fig. 1) and for the modified amplifiers shown in Fig. 2 (DTMOS FCA), Fig. 3 (FCA + RFF + SB) and Fig. 4 (DTMOS FCA + RFF + SB). From this graphic two main conclusions can be drawn:

1) For supply voltages close to the nominal values of the 130 nm CMOS process (i.e., V_{DD} = 1.2 V ± 10 %), the FCA with DTMOS devices (the modified amplifier shown in Fig. 2) reaches higher DC gain than the original (conventional) FCA shown in Fig. 1;
2) If a low voltage design is targeted (i.e. V_{DD} << 1. 2 V; $V_{DD} \approx$ 0.7 V ± 5 %) it is much more efficient to combine RFF and SB techniques as suggested in the circuit topology shown in Fig. 3. However, in this case of reduced V_{DD}, there is no advantage of employing DTMOS in some devices (as suggested in the modified FCA shown in Fig. 4).

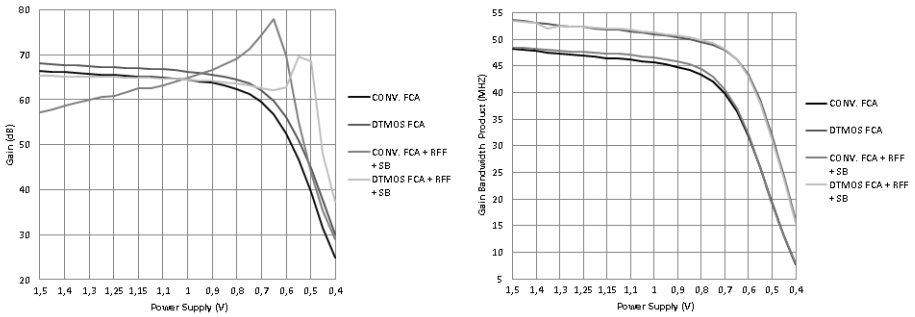
Fig. 5(b) shows the simulated gain-bandwidth product (GBW) for different positive (V_{DD}) supply voltage conditions (ranging from 0.4 V to 1.5 V), for the conventional FCA (Fig. 1) and for the modified amplifiers shown in Fig. 2 (DTMOS FCA), Fig. 3 (FCA + RFF + SB) and Fig. 4 (DTMOS FCA + RFF + SB). From this graphic a single conclusion can be derived: The use of DTMOS is the most efficient way of enhancing the GBW of an amplifier in a wide range of the supply voltage. However, there is no visible advantage of using either RFF or SB techniques.

5 Performance Comparisons and Main Conclusions

The performance of this circuitry has been evaluated through exhaustive simulations in different PVT corners (13 combinations of: 1) process: slow, typical, fast; 2) V_{DD}: 1.14 V, 1.2 V, 1.26 V and also 0.665, 0.700, 0.735 V; 3) temperature: -40, 27 and +85 ºC). Summarized key results are presented in Tables 1, 2 and 3. From these Tables we can extract the following two conclusions.

From Tables 1 and 2 one can conclude that, if high DC gain with low variability and high GBW are envisaged the FCA with DTMOS (topology shown in Fig. 2) is the best choice. Hence, there is no relevant advantage in using either RFF or/and SB techniques. Moreover, the results in Table 3 demystify the idea that the use of DTMOS at nominal supply voltages will enable the parasitic lateral bipolar transistors, thus boosting the current consumption. We demonstrate here that, there is no risk, if we use DTMOS only in the suggested devices.

From Table 3 one can conclude that, when RFF and SB techniques are used (FCAs in Fig. 3 and in Fig. 4) the power dissipation is minimum (either using or not DTMOS devices). Average power savings of the order of 8% can be achieved if RFF and SB techniques are used since the complete biasing circuitry can be removed. Therefore, we also demonstrate in his paper that, the RFF technique, in particular, is not so useful for reaching higher GBW and speed performances but, rather, to simplify the biasing circuitry when combined with a SB technique allowing significant power savings.



(a) (b)

Figs. 5. Simulated DC gain (a) and Simulated gain-bandwidth product (b) for different positive (V_{DD}) supply voltage conditions (ranging from 0.4 V to 1.5 V), for the conventional FCA (Fig. 1) and for the modified amplifiers shown in Fig. 2, Fig. 3 and Fig. 4.

Table 1. Simulated DC gain for the 4 amplifier topologies and for 13 different PVT corners.

Topologies	Measures			
	V_{DD}	$\overline{Gain}$ (dB)	$Gain_{min}$ (dB)	$\Delta\ Gain_{min}$ (dB)
CONVENTIONAL FCA	0.7	57.04	47.28	+/- 6.895
	1.2	64.81	62.68	+/- 1.825
DTMOS FCA	0.7	60.75	56.57	+/- 3.515
	1.2	66.6	65.42	+/- 0.95
CONV. FCA + RFF + SB	0.7	62.74	42.28	+/- 17.465
	1.2	62.42	54.39	+/- 7.58
DTMOS FCA + RFF + SB	0.7	44.86	23.82	+/- 19.595
	1.2	61.03	52.54	+/- 7.365

Table 2. Simulated GBW for the 4 amplifier topologies and for 13 different PVT corners.

Topologies	Measures			
	V_{DD}	$\overline{GBW}$ (MHz)	GBW_{min} (MHz)	$\Delta\ GBW_{min}$ (MHz)
CONVENTIONAL FCA	0.7	36.49	19.25	+/- 14.145
	1.2	46.88	40.55	+/- 6.645
DTMOS FCA	0.7	45.97	36.22	+/- 9.5
	1.2	52.47	45.24	+/- 7.4
CONV. FCA + RFF + SB	0.7	36.97	18.97	+/- 14.66
	1.2	47.73	41.74	+/- 6.19
DTMOS FCA + RFF + SB	0.7	45.52	36.4	+/- 8.95
	1.2	52.39	46.0	+/- 6.57

Table 3. Simulated power for the 4 amplifier topologies and for 13 different PVT corners.

Topologies	Measures	
	$\overline{P}$	P_{max}
CONVENTIONAL FCA	213	378
DTMOS FCA	215	379
CONV. FCA + RFF + SB	196	364
DTMOS FCA + RFF + SB	198	365

References

1. Figueiredo, M., Tavares, R., Santin, E., Ferreira, J., Evans, G., Goes, J.: A Two-Stage Fully Differential Inverter-based Self-Biased CMOS Amplifier with High Efficiency, IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, pp. 1591--1603, (2011)
2. Hsu, H., Lee, T., Fu, G.: A 90 nm DT-MOS Transistor for High Speed Operation," in Proc. 4th European Microwave Integrated Circuits Conference, (2009)
3. Hsu, H., Lee, T.: Compact Layout of DT-MOS Trasistor With Source-Follower Subcircuit in 90-nm CMOS Technology", IEEE Electron Devices Letters, vol. 29, pp. 392--395, (2008)
4. Assaderaghi, F., Sinitsky, D., Park, S.A., Bokor, J., Ko, P. K., Hu, C.: Dynamic Treshold-Voltage MOSFET (DTMOS) for Ultra.Low Voltage VLSI," IEEE Trans. Electron Devices, vol. 44, pp. 414--422, (1997)
5. Chatterjee, S., Tsividis, Y., Kinget, P.: 0.5-V Analog Circuit Techniques and Their Application in OTA and Filter Design, IEEE J. Solid-State Circuits, vol. 40, pp. 2373--2387, (2005)
6. Bazes, M.: Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers, IEEE J. Solid-State Circuits, vol. 26, pp. 165--168, (1991)
7. Santin, E., Figueiredo, M., Goes, J., Oliveira, L.B.: CMOS Fully Differential Feedforward-Regulated Folded Cascode Amplifier, DoCEIS'10, Portugal, (2010)
8. Zheng, Y., Saavedra, C.: Feedforward-Regulated Cascode OTA for Gigahertz Applications, IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, pp. 3373--3382, (2008)
9. Figueiredo, E.S., Goes, J., Tavares, R., Evans, G., Two-Stage Fully Differential Inverter-based Self-Biased CMOS Amplifier with High Efficiency, in Proc. IEEE Int. Symp.Circuits Syst. (ISCAS), pp. 2828--2831, (2010)