Compact and Power Efficient MOS-NDR Muller C-Elements

Juan Núñez, María Avedillo, José Quintana

Compact and Power Efficient MOS-NDR Muller C-Elements

Juan Núñez , María J. Avedillo and José M. Quintana

Instituto de Microelectrónica de Sevilla (IMSE-CNM-CSIC) & Universidad de Sevilla
Av. Américo Vespucio s/n, 41092, Sevilla (Spain)
{jnunez, avedillo, josem} @ imse-cnm.csic.es

Abstract. Recently there is a renewed interest in the development of transistor circuits which emulate the Negative Differential Resistance (NDR) exhibited by different emerging devices like Resonant Tunneling Diodes (RTDs). These MOS-NDR circuits easily allow the prototyping of design concepts and techniques developed for such NDR devices. The importation of those concepts into transistor technologies can result in circuit realizations which are advantageous for some functionalities and application fields. This paper describes a Muller C-element which illustrates this statement which is inspired in an RTD-based topology. The required RTD is implemented by means of the MOS-NDR device. A 4-input Muller C-element has been fabricated and experimentally validated. The proposed circuit compares favorably with respect to a well-known conventional gate realization.

Keywords: Resonant Tunneling Diode (RTD), Negative Differential Resistance (NDR), Muller C-Element, Power Consumption.

1 Introduction

Resonant tunnelling diodes (RTDs) are considered today as one of the most mature types of quantum-effect devices, already operating at room temperature, and being promising candidates for future nanoscale integration. RTDs exhibit a negative differential resistance (NDR) region in their current-voltage characteristics, which can be exploited to significantly increase the functionality implemented by a single gate in comparison to MOS and bipolar technologies. Most of the reported working circuits have been fabricated in III-V materials while Si-based tunnelling diodes compatible to standard CMOS fabs are currently an area of active.

Circuit ideas coming from RTD-based designs can be interesting even in an "all CMOS" environment [1], [2]. To prove this, we have designed a Muller C-element, which can be very efficiently implemented by using one RTD, and we have substituted it by a MOS circuit able to emulate its NDR characteristic: the MOS-NDR device [2]. A Muller C-element is a circuit widely used in the design of self-timing circuits to perform the functions "and" of events (transitions 1→0 or 0 → 1). Its output is made equal to the value of the inputs after all of them reach the same value; on the contrary, the output remains the same. The equation which defines a Muller C-element of N inputs is given by $Q=\{x_1 \cdot x_2 \cdot \ldots \cdot x_N\}+\{x_1 + x_2 + \ldots + x_N\} \cdot q$, where x_i,

(i=1,…, N) are the primary input, Q the next state variable, and q the present state variable.

In this paper, a novel multi-input Muller C-element circuit is proposed and analysed, concluding that the CMOS implementation of the original RTD-based idea for its realization is more efficient than other conventional C-element structures.

2 Contribution to Value Creation

Currently, the reduction of power consumption is considered as one of the main challenges of the design of high-speed integrated circuits, and thus, great efforts are devoted in this direction to improve their performances.

The extension of circuit design ideas based on NDR devices implies, for certain applications, advantages over conventional CMOS design styles. In particular, for high-speed circuits in which the number of components is high, design techniques using NDR devices can reduce power consumption. From our point of view, this issue represents a research with great potential for value creation.

3 Proposed Muller C-Element

The current-voltage characteristic of RTDs makes them suitable to implement circuits in which the output logic level must be maintained under certain conditions. A RTD-based Muller C-element only requires one RTD device and as many active elements as inputs signal. Fig. 1a and Fig. 1b show the circuit diagram of a basic RTD-based Muller C-element of 2 inputs [3] along with load curves plots illustrating its operation principle, respectively. When both transistors are biased such that their total current is smaller than the valley current of the RTD (I_V), output voltage "L_1" is obtained. When the total current through the input stage is larger than the peak current (I_p) of the RTD, solution corresponds to "H_1". Finally, when the current through the transistors is between the peak and the valley currents, output levels "L_2" or "H_2" could be obtained. Solution "L_2" corresponds to a situation in which originally the output was "L_1" and one input changes its state. Similarly, "H_2" comes from an original situation in which solution "H_1" was active. Solutions "H_1" and "H_2" are associated to a high level of the output, whereas "L_1" and "L_2" corresponds to a low level. In the structure proposed in Fig. 1a the input stage consists of PMOS transistors so states "L_1" is obtained when the logic level of all the inputs is high and "H_1" when the input set is grounded. This configuration leads to an inverted Muller C-element structure. This operation principle can be extended to a multi-input circuit by adding as many transistors in parallel to the input branch as input signals needed.

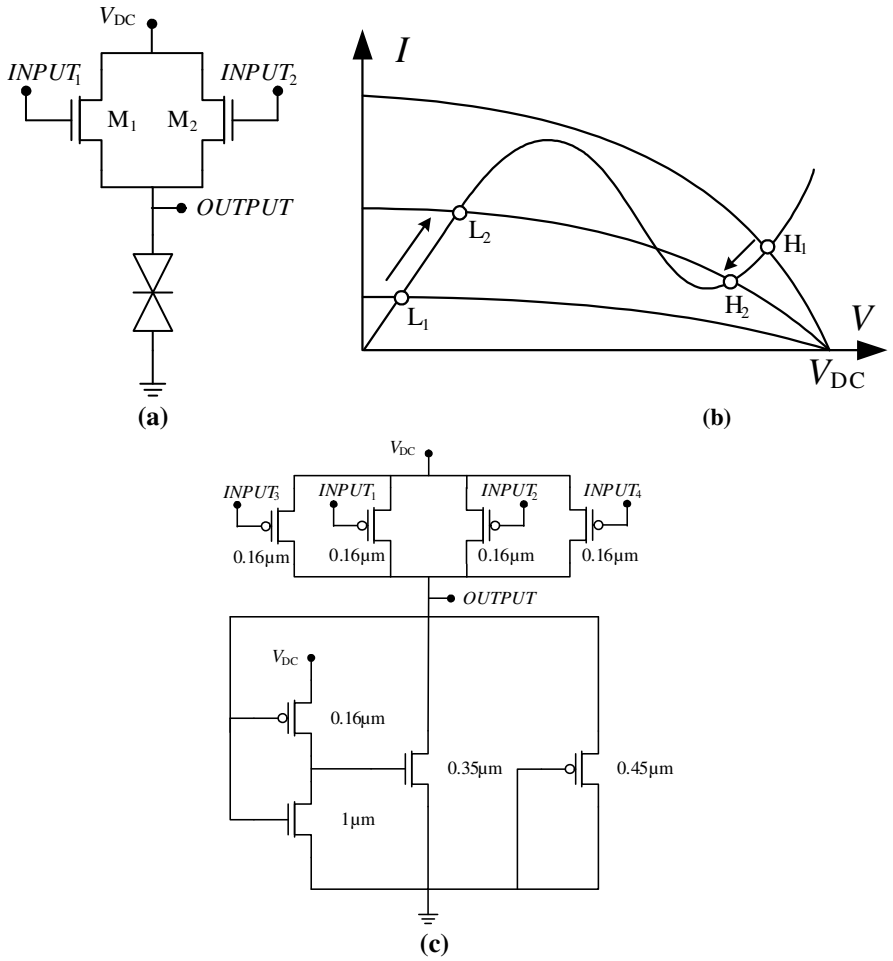
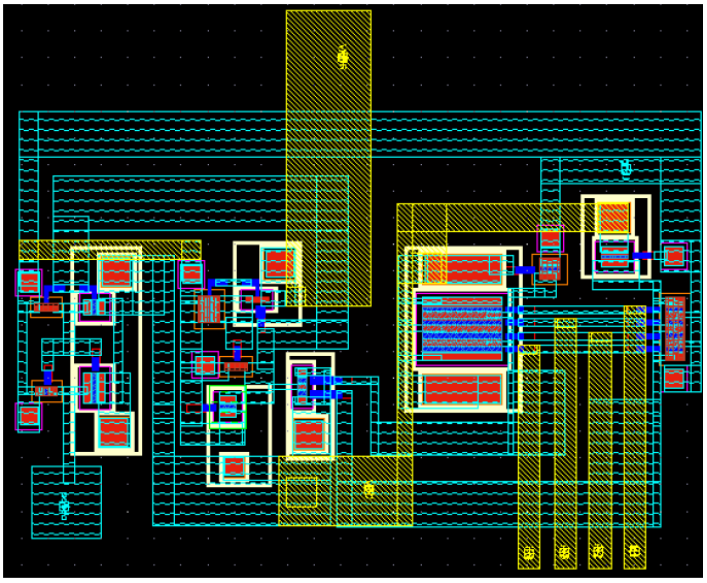


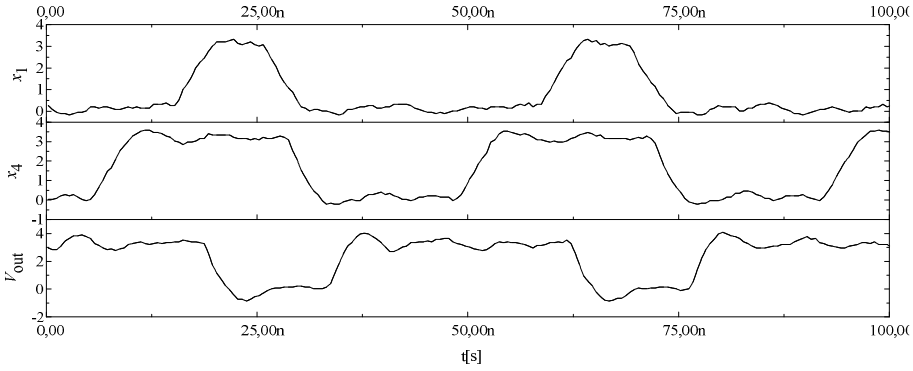
Fig. 1 RTD-based Muller C-element of two inputs: (a) Schematic. (b) Operation principle. (c) Schematic of the fabricated Muller C-element of four inputs implemented with a general NDR device

The NDR current-voltage characteristic of the RTD can be emulated using the transistor circuit described in [2], called the MOS-NDR device. We have designed and fabricated a 4-input inverted Muller C-element (shown in Fig. 1c) in a 1.2V UMC 130nm commercial technology (layout is shown in Fig. 2a). The robustness of our design have been checked through 3-sigma mismatch and process MonteCarlo simulations, corner analysis and taking, as well, variations of the bias voltage of ±10% around its nominal value into account. Fig. 2b depicts measured waveforms showing correct operation of the fabricated circuit. We have applied an input set consisting of four digital pulses in which the last signals to switch from '0' to '1' and from '1' to '0' logic states are x_1 and x_4, respectively. Thus, when x_1 increases its

value, all the inputs are '1' and the output voltage, V_{out}, goes down (state "L_1", in Fig. 1b). In a similar way, when x_4 switches to '0', all the inputs PMOS transistors are activated and the output rises to the high level (state "H_1" in Fig. 1b). Note that the high logic level of the inputs and the output correspond to 3.3V since they have been measured on an encapsulated sample with digital pads from an standard logic library, thus, measured delays does not correspond to the real timing characteristic of the circuit.



(a)



(b)

Fig. 2. Proposed Muller C-element structure: (a) Layout (b) Experimental waveforms

4 Evaluation and Comparison

Simulation results using the Cadence® Toolset have been obtained to evaluate the performance of the proposed circuit. We have considered the typical input waveforms shown in Fig. 3a and a bias voltage of 1.2V, and we have measured the average power consumption for different values of the switching frequency of the inputs, 1/T. The structure has been loaded with one CMOS inverter. In order to evaluate the efficiency of our structure, we have compared it with the 4-input Muller C-element circuit proposed by Wuu and Vrudhula [4]. This circuit consists of a combinational part made of a NOR tree and a NAND tree which are connected to a latch that keeps the value of the output until the next change occurs. To make comparisons as fair as possible, we have simulated it by using transistors from the same technology and loaded with the same CMOS inverter. Fig. 3b shows the simulation results obtained, where it can be observed that our circuit is more efficient when the switching

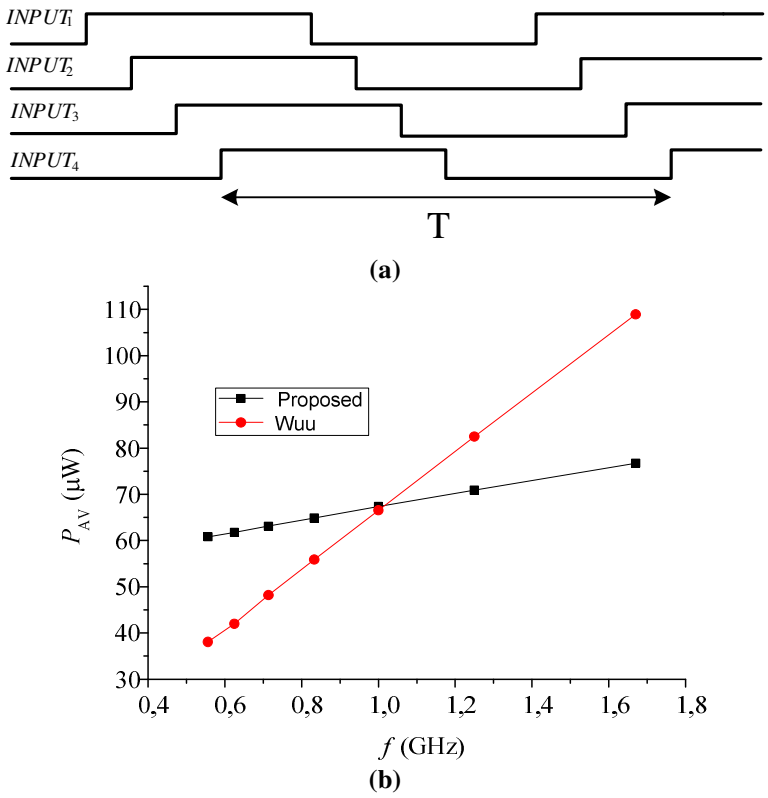


Fig. 3. (a) Simulation setup of the input set. (b) Simulation results showing the variation of the power consumption with the switching frequency of the inputs for the proposed and the circuit reported in [4]

frequency is above 1GHz. Note that the power consumption measured in our structure is not as significantly affected by variations of the frequency as the proposed in [4].

Area efficiency is one of the main characteristics of our design: 6 PMOS transistors (4 for the inputs and 2 for the MOS-NDR device) and 2 NMOS transistors are needed, which corresponds to a total area of $0.312\mu m^2$. On the other hand, the circuit proposed by Wuu has been designed using 2-input NOR and NAND gates with the minimum width and length allowed in this technology. A total area of $1.728\mu m^2$ for the combinational block and $0.778\mu 1m^2$ for the latch is needed. It implies that the total area for this structure ($2.506\mu m^2$) is eight times larger than the required by our design.

The proposed Muller C-element circuit also overcomes one main drawback of other single gate implementations which require stacking many transistors (a 4-input Muller C-element has 8 transistors stacked). Unlike this, a single parallel transistor is added per input in our realization. Our study has been completed with the design of a 6-input Muller C-element which has been validated by the same robustness checking protocol. Its power consumption is smaller than the one exhibited by the 4-input Wuu Muller C-element for input frequencies over 1.25GHz.

Conclusions

A compact realization of the Muller C-element circuit has been presented which takes advantages of the shape of the I-V characteristic of NDR devices. In spite of exhibiting a sequential behaviour it does not require feedback paths nor rely on charge loading in floating nodes. It has been demonstrated to improve power performance over a well-known structure when the switching frequency of the inputs increases.

Acknowledgments. This work has been funded in part by the Spanish Ministry of Education and Science with support from ERDF under Project TEC2010-18937.

References

1. Núñez, J., María J. Avedillo, José M. Quintana: Efficient realization of MOS-NDR threshold logic gates. IET Electronics Letters, vol. 45, no 23, pp.1158--1160, November 2009.
2. Gan, K.-J. et al.: Four-valued memory circuit using three-peak MOS-NDR devices and circuits. IET Electronics Letters, vol. 42, no. 9, pp. 514--515, April 2006.
3. Lin, C.-H. et al.: InP-based high speed digital logic gates using an RTD/HBT heterostructure. In: Proceedings of the Eleventh International Conference on Indium Phosphide and Related Materials, pp. 419--422, 1999.
4. Wuu, T.-Y. and Vrudhla, S.B.K.: A design of a fast and area efficient multi-input Muller C-element. IEEE Transaction on Very Large Scale Integration (VLSI) Systems, vol 1, no. 2, pp. 215-.219, Jun. 1993.