Dynamic Behavior of Resistive Random Access Memories (RRAMS) Based on Plastic Semiconductor

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Abstract. Resistive Random Access Memories based on metal-oxide polymer diodes are characterized. The dynamic behavior is studied by recording current-voltage characteristics with varying voltage ramp speed. It is demonstrated that these organic memory devices have an internal capacitive double-layer structure, which inhibits the switching at high ramp rates (1000 V/s). This behavior is modeled and explained in terms of an equivalent circuit.

Keywords: Resistive Random Access Memory (RRAM), Switching, Electrical Bistability, Non-Volatile Memory, Negative Differential Resistance (NDR).

1 Introduction

Organic memory devices are becoming interesting candidates for electronic applications in information technologies [1]. One emerging candidate is the resistance random access memory (RRAM) based on metal oxides [2,3] and organic semiconductors [4-6]. These RRAMs have shown electrically induced resistive switching effects and have been proposed as the basis for future non-volatile memories. They associate the advantages of Flash and DRAM (dynamic random access memories) such as higher packing density, faster switching speed and longer storage life.

Although, several metal-oxides structures exhibited resistive switching properties, the measured switching parameters vary in a wide range, which calls for a more consistent and uniform characterization methodologies. Furthermore, reported switching speeds vary by orders of magnitude [7-14]. The values range from nanoseconds to milliseconds. The inconsistencies might be due to different semiconductors, device geometries, or measurement procedures. In order to clarify these discrepancies, we characterize the switching speed of a metal-oxide memory device using dynamic measurements and equivalent circuit modeling.

The dynamic characterization of the metal-oxide polymer structure through a double RC circuit provides insight on the switching phenomenon. It is demonstrated the relevance of the oxide layer and its role on limiting the switching speed.

2 Contribution to Value Creation

Organic based memory devices provide a simplified manufacturing process yielding low-cost, flexible, and light-weight area approaching the nano-scale dimensions. However, the technology development is hampered by the lack of understanding about the switching mechanism.

This study shows that switching is located in the oxide layer. A critical field across this high capacitance oxide layer is therefore needed to switch the memory between on and off states. The associated scan frequency of which the voltage does not exceed the critical field is called the voltage transfer frequency.

The knowledge gain with this study will allow us to optimize the device structure for faster switching speed.

3 Device Description

The organic memory used consists on a diode structure (Fig. 1) with an Al bottom electrode, a sputtered layer of Al_2O_3 (20 nm), a spirofluorene polymer (80 nm), and a Ba/Al (5 nm/100 nm) top electrode that forms an Ohmic contact with the polymer. The devices with an active area of 9 and 1 mm^2 were encapsulated to exclude O_2 and H_2O. The main difference in the device structure between the memory and a bipolar organic light emitting diode (OLED) is the Al bottom contact instead of an ITO contact.

In all cases, positive bias voltage refers to the bottom aluminum electrode being positive with respect to the top Barium electrode. The memories were formed, by applying a sweeping voltage from 0 to 12 V. Quasi-static current–voltage (J–V) curves were obtained using a Keithley 487 picoammeter. The dynamic behavior of the J-V curves was recorded using a signal generator and an oscilloscope combined with a low noise amplifier. The experimental arrangement is shown in Fig. 1. Device modeling was done using Agilent Advanced Design System (ADS).

4 Experimental Results

The memory device structure and the experimental setup are illustrated in Fig. 1.

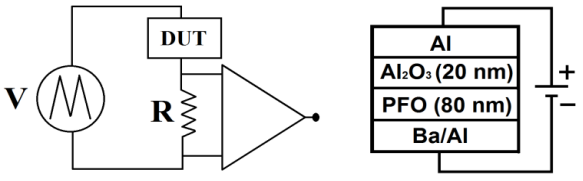

Fig. 1. On the left it is represented the experimental setup. On the right it is represented the device layout

The current-voltage (J-V) characteristics for both conductance states are illustrated in Fig. 2. The most salient feature of the on-state is a step-like decrease in current or negative differential resistance (NDR) region, at a certain threshold voltage (4-5 Volts). Reliable switching is obtained by applying a voltage pulse at the top and at the bottom of the NDR [7,8]. The memory switches to the low resistance on-state with a pulse of 2-4 V. A pulse of 7-10 V, corresponding to the end of the NDR regime, switches the memory to the high resistance off-state.

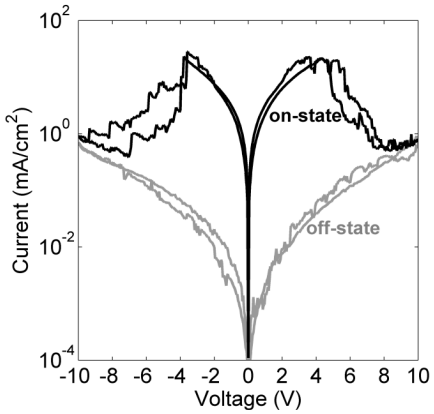

Fig. 2. J-V characteristics in both high (on-state) and low (off-state) conductance states

In off-state the RRAM behaves as a capacitor. In the on-state, the J-V characteristics exhibit a sharp NDR as shown in Fig. 3. As the frequency of the input signal increases, the current decreases. The magnitude of the NDR also gradually decreases and vanishes at 1000 V/s.

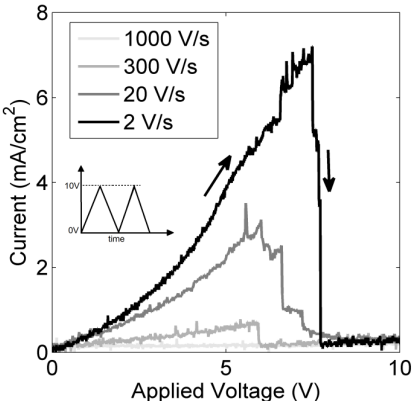

Fig. 3. On-state J-V characteristics recorded at different scan rates showing the NDR disappearance. The inset shows the input signal

In order to understand the mechanism which limits the ability of the RRAM to switch, the dynamic behavior of both states was studied as function of the voltage scan

rate. The off-state characteristics show a typical behavior. The current increases as the voltage scan rate increases. This is expected due to the effect of increasing displacement current. The off-state behaves as leaky capacitor. Intriguingly the on-state shows a very different behavior. Upon increasing voltage scan rate the current decreases, the NDR region becomes less defined and eventually disappears at high voltage scan rates. This behavior is counterintuitive because in similar way as the off-state an increase in current at high scan rates is expected. This peculiar behavior of the on-state is the reason why the RRAM cannot be programmed on and off at high rates.

We propose that the reason for this counterintuitive behavior of the J-V characteristics relies on the internal diode structure. The device is a double-layer comprised of a thin oxide layer (20 nm) with a high capacitance, in series with a polymer bulk region (80 nm) with a comparatively small resistance and capacitance. The response of this double-layer to a high sweeping voltage ramps is conveniently modeled by a double RC circuit. The equivalent circuit model is shown in the inset of Fig. 4 where C_{ox} and R_{ox} represent the oxide layer and C_{poly}, R_{poly} represent the polymer layer. Previously, we have shown that this double-layer model adequately describes the frequency response of the diode [15]. Here, we will describe the behavior of this network when a ramp voltage is applied.

Fig. 4 shows the internal voltage across the polymer layer as function of the voltage sweeping speed. Device parameters used were based on typical values estimated by modeling the frequency response [15]. We use C_{poly} = 3 nF, R_{poly} = 300 kΩ, C_{ox} = 30 nF, R_{ox}= 80 MΩ. These are in line with the theoretically values estimated on geometrical parameters.

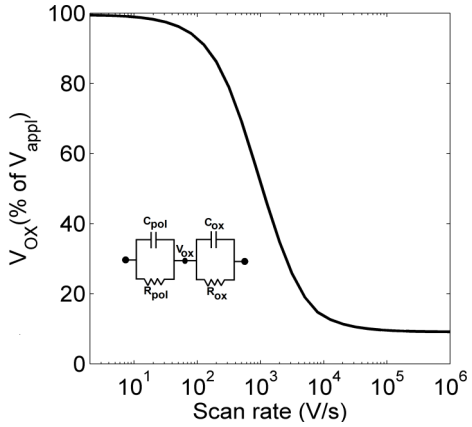

Fig. 4. Voltage drop across the oxide layer (in %) as a function of the voltage scan rate. Data obtained through Agilent ADS using the equivalent double RC network in the inset with the following parameters: C_{poly} = 3 nF, R_{poly} = 300 kΩ, C_{oxide} = 30 nF, R_{ox} = 80 MΩ

For a low ramp rate most external voltage drop is across the high impedance layer (the oxide) and only a small fraction of the external voltage is dropped across the polymer. When the sweeping frequency increases the oxide capacitance begins to be shortened and the applied voltage will rapidly increase across the polymer layer. The increase in the voltage sweeping speed has then the effect of moving the voltage drop

from the oxide to the polymer layer. Using a simple voltage divider circuit, the fraction of the voltage across the oxide V_{ox} in respect to the total applied voltage V_{appl} is given by:

$$\frac{V_{ox}}{V_{appl}} = 1 - \frac{Z_{poly}}{Z_{poly} + Z_{ox}} \quad (1)$$

Where Z_{poly} and Z_{ox} are the polymer and the oxide impedances respectively.
In terms of individual circuit components we can write.

$$\frac{V_{ox}}{V_{appl}} = \frac{C_{ox}}{C_{ox} + \frac{C_{poly}}{C_{ox}}\left(\frac{1 + j\omega C_{ox} R_{ox}}{1 + j\omega C_{poly} R_{poly}}\right)} \quad (2)$$

where j is the imaginary unit and ω the angular frequency. The device internal structure is then basically a voltage divider. However, because the oxide capacitance is much higher that the polymer capacitance, the way the applied external voltage is split between the two layers dependents on the voltage scanning speed or repetition rate. Fig. 4 shows the voltage V_{ox} in percentage of V_{appl} as function of the scan rate. At low frequencies most of the V_{appl} is across the oxide, however as the frequency increases above 20 V/s, V_{ox} decreases rapidly and at 1000 V/s, 55 % of V_{appl} is now across the polymer layer. This underlines the importance of the field across the oxide layer in terms of switching ability, and strongly suggests that increasing the thickness of the oxide layer will speed-up the dynamic response.

5 Conclusion

The electrical behavior of the memory in both resistive states was dynamically characterized. In the off-state, current increases as the voltage scan rate increases, due to the effect of increasing displacement current. As for the on-state, upon increasing voltage scan rate the current decreases, the NDR region becomes less defined and disappears at high voltage scan rates. This is explained through the device internal structure. Under high repetition rates, the applied voltage moves out from the oxide. This emphasizes the oxide importance in speeding up the dynamic response of the RRAMs.

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