Low-Power Low-Voltage ΔΣ Modulator Using Switched-Capacitor Passive Filters

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Abstract. A low-voltage low-power fourth-order active-passive ΔΣ modulator with one active stage is presented. The input-feedforward architecture is adopted, which improves the voltage swing prior to the quantizer. This enables a simpler comparator design and cascade of three passive filters. The passive integrator, as an alternate option to its power-hungry active counterpart, and the non-idealities associated with it are investigated. The active integrator used at the input stage provides most of the loop gain, which suppresses the thermal noise from the succeeding stages and minimizes the non-idealities in the comparator, such as noise and offset. The active integrator employs a two-stage amplifier with load compensation, whose DC-gain is boosted by a partially body-driven technique. The modulator, operated from a 0.7 V supply and clocked with 256 kHz sampling frequency, achieves 84 dB SNR and 80.3 dB SNDR over a 500 Hz signal bandwidth, while it dissipates only 400 nW power.

Keywords: Passive integrator, delta-sigma modulator, low-voltage, low-power, active-passive modulator, feedforward architecture

1 Introduction

Biomedical electronics including portable medical devices, ambulatory and in-site hospital equipments and body implantable devices, in particular, have gained significant attention in healthcare. Low energy consumption is one of the major design concerns for prolongation of the battery lifetime or other limited source of energy. The analog-to-digital converters (ADCs) are the key building blocks of such devices. Delta-sigma modulator is a powerful ADC technique because of its higher accuracy in low-speed applications (e.g., medical applications).

Passive integrator, as an alternative to the power-hungry active integrator, is a significant approach in the design of low-power and low-voltage delta-sigma (ΔΣ) modulators for reducing the analog power consumption [1-6]. However, due to the

lack of DC gain inside the passive filter (or integrator), the modulator is sensitive to noise coupling, thereby affecting the signal-to-noise ratio (SNR). Modulators in [1] and [2] employ switched-capacitor (SC) gain-boosted passive filter to somewhat compensate for the lack of gain. However, achieving very high gain requires unrealistically large capacitive area as well as high sensitivity to parasitic capacitances [3]. In [4] no DC gain is used in the second-order loop filter. Instead, a three-stage preamplifier is exploited before the comparator to compensate for the gain, which is a power consuming solution.

Due to no gain, the signal experiences a large suppression inside the passive filter, making the comparator design a challenging task. The comparator non-idealities including noise, DC offset, and hysteresis directly limit the modulator resolution [5, 6]. The third-order modulator in [5] makes use of the passive filter in the first and third stages and an active Gm-C filter in the middle stage in order to compensate for the loop gain and to mitigate the comparator's offset and noise. In addition, the Gm block is to isolate the two pole sectors from each other and to prevent inter-stage loading between them. The fourth-order active-passive modulator in [7] utilizes a low-power amplifier topology in the first integrator, which can suppress the comparator non-idealities and the thermal noise from the succeeding passive stages, resulting in significant reduction of the capacitive area.

This chapter introduces a new approach for power reduction in the $\Delta\Sigma$ modulators. It describes the design of the basic passive filter and the non-idealities associated with it. The traditional passive modulators using cascade-of-integrators feedback (CIFB) architecture are briefly reviewed and their advantages and disadvantages are explained in details. Then, a fourth-order feedforward active-passive modulator is presented using only one active stage, which mitigates some of the fundamental problems associated with the traditional passive ADCs.

The input feedforward architecture has an extra path from the input of the modulator to the quantizer [8, 11]. This small architectural modification eliminates the signal component inside the loop filter; therefore the filter only processes the quantization noise [11]. This distinct feature of the feedforward modulator structure encourages the cascading of three power-efficient SC passive filters despite their large attenuation. Moreover, the voltage swing at the quantizer input is the sum of the input signal and the suppressed quantization noise (processed by the filter), which eases the comparator design without requiring any preamplifier circuit. Significant power reduction can thus be achieved due to (i) the reduced sampling clock frequency by employing a fourth-order active-passive loop filter; (ii) the removal of the power-consuming preamplifier prior to the comparator, unlike the traditional passive modulators with feedback architecture; (iii) the use of power-efficient passive integrators; (iv) the relaxed amplifier design requirements in the full input-feedforward modulator structure [8, 9]; (v) an accurate and low attenuation passive adder for summation of the input and feedforward paths, and (vi) last, but not least, the reduced supply voltage helped to scale down the power consumption from digital blocks.

The rest of the chapter is organized as follows. Section 2 discusses the issues associated with the design of passive modulators using feedback structure. Section 3 describes both the architecture-level and circuit-level design of the proposed fourth-

order active-passive modulator, followed by the simulation results in section 4. Section 5 presents the performance comparison of this modulator with respect to the previously reported passive modulators. The chapter is then summarized in section 6.

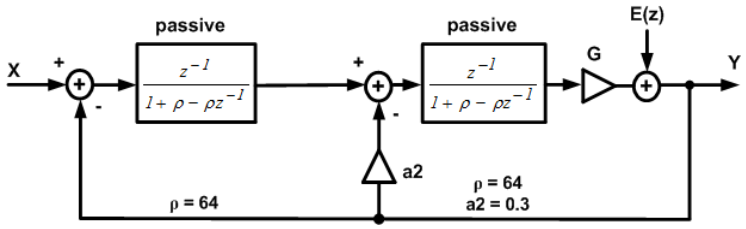

Fig. 1. The linearized model of the 2nd-order passive ΔΣ modulator using distributed feedback topology [7] (Courtesy of IEEE)

2 Passive Modulator Design Using CIFB Topology

In this section we take a closer look at the challenges concerning the design of passive modulators implemented by the CIFB architecture. The CIFB topology has no forward connections to the quantizer input, unlike the CIFF topology, but requires internal digital-to-analog converters (DACs) which are fed back to the input and the intermediate filters. In other words, a fourth-order CIFB modulator topology needs four feedback DAC branches to each integrator's input, while a CIFF modulator structure needs only one feedback DAC from the output to the input. Thus, the DAC circuitry is much simpler in a CIFF modulator structure.

2.1 System-Level Considerations

The linear model of the second-order passive ΔΣ modulator with two-pole lowpass filter and single-bit quantizer is shown in Fig. 1. To determine the signal and noise transfer functions (STF and NTF), a linear model is used for the quantizer. It is a gain stage, G, followed by additive white quantization noise. The gain factor G in a conventional active modulator is estimated as unity [12] assuming the integrators swing is maintained close to the reference voltage. In a passive modulator the signal swing at the quantizer input is much weaker than the reference level, due to the successive attenuation by the passive filters [1-3], resulting in a non-unity G. This gain is lumped into the comparator input, according to Fig. 1, and is a function of the passive filter's pole location [3]. An estimate of this gain is given by [2, 4] in which the overall loop gain is approximated to be unity at half of the sampling clock frequency, $f_s/2$. For an overall loop filter transfer function H_T, the estimated G can be calculated as $1/|H_T(f_s/2)|$. On the other hand, since the modulator is a nonlinear system, an accurate value of the quantizer gain can only be obtained from the nonlinear simulations [13].

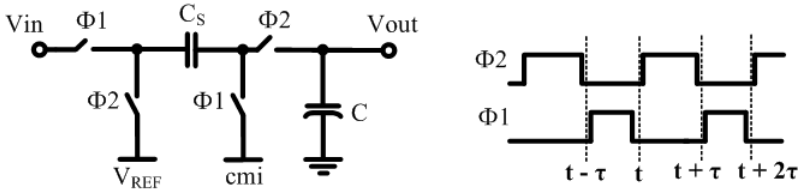

Fig. 2. Passive lowpass filter in a single-ended form together with two-phase non-overlapping clocks [7] (Courtesy of IEEE)

For a simple passive filter shown in Fig. 2, the ideal transfer function can be given in the *z*-domain as

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{-z^{-1}}{1+\rho-\rho z^{-1}} \tag{1}$$

where $\rho = C/C_s$. The low-frequency gain is unity and the -3 dB cut-off frequency can be calculated from equation (1) as

$$f_{-3dB} = \frac{f_s}{2\pi(\rho+1)} \tag{2}$$

where f_s is the sampling clock frequency. Taking f_s = 500 kHz, C_s = 2 pF, determined from the thermal noise requirement, and C = 128 pF, placing the -3 dB bandwidth around 1 kHz, the NTF and STF of the second-order passive modulator shown in Fig. 1 can be approximated as:

$$NTF(z) = \frac{1}{1+0.3GH+GH^2} = \frac{1.36-2.77z+1.41z^2}{1-2.38z+1.41z^2} \tag{3}$$

$$STF(z) = \frac{GH^2}{1+0.3GH+GH^2} = \frac{0.02z^2}{1-2.38z+1.41z^2} \tag{4}$$

Figure 3 depicts the magnitude of the NTF and STF. As expected, the passive modulator suffers from the limited in-band quantization-noise suppression due to lack of gain in the passive loop filter, resulting in low SNR. Unlike the conventional active ΔΣ ADCs which has unity-gain STF at low frequencies, some signal attenuation is obtained in the passive modulator. As clearly seen, this attenuation (or loss) is -3.5 dB

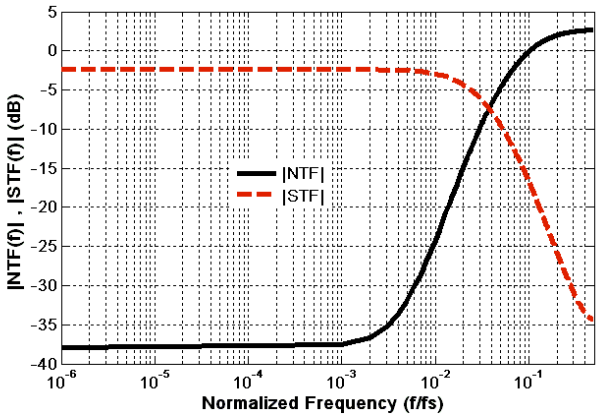

Fig. 3. The magnitude of NTF and STF of a 2nd-order passive modulator with $\rho = 64$ [7] (Courtesy of IEEE)

at low-frequency, which can also be obtained by substituting $z = 1$ into STF equation (4). This is the fundamental problem of the passive filters and the major performance limiting factor in the passive modulators, which terminates to an extremely low voltage swing at the quantizer input. For the second-order passive modulator presented in [3], as an example, the integrators output swing is in the order of 10 mVrms and 100 μVrms, respectively, for a full scale (FS) input that the comparator has to detect it. A highly sensitive comparator is then required to distinguish the signal from the noise coupled inside the loop. Therefore, the comparator in this design employs a three-stage preamplifier circuit in order to compensate for the required loop gain, dissipating a large amount of analog power in this block. To the best of our knowledge, most of the existing passive ADCs have been designed based on the CIFB topology [1-4], which rely only on second-order loop filter. Cascading more than two passive filters is impractical because the very large signal attenuation inside the loop demands multi-stage power-consuming preamplifier circuit prior to the comparator.

2.2 Low-Voltage Compatibility

One of the most significant advantages of the passive filter is that it can function at very low supply voltage as long as the gate of the switches is driven adequately. Utilizing advanced switches developed to date, the switch overdriving problem can simply be alleviated. Low-V_{TH} switch [8, 14], gate-boosted [15-16] or boot-strapped switches [17] are several examples of such modern switches. Energy harvesting and biomedical implant systems are two applications where ultra low-voltage circuit design is compulsory and highly demanding. Conventional analog circuit topologies are no longer useful in these systems. Therefore, new circuit techniques have been developed recently, which have enabled ultra low-voltage operation of the ΔΣ ADCs [15-16]. Body-input operational transconductance amplifiers (OTAs) and body-input gate-

clocked comparator operating at 0.5 V in [15] eliminated the constraint on the threshold voltage. Moreover, inverter-based integrators were realized by overdrive voltages near the V_{TH} in the modulator presented in [16] using a switched-capacitor (SC) biasing scheme, where charge pump clock boosting scheme were utilized for sufficient switch overdrive. These combinations have made it possible to develop a ΔΣ modulator operated from a power supply below 0.3 V. Both modulator prototypes rely on power-hungry active integrators at which analog circuit design is a challenging task at such low supply voltages, due to the limited headroom and small available signal swing. For a given gm, a body-input OTA requires several times larger bias current than a typical gate-input OTA, thereby preventing the target modulator to achieve a high power-efficiency. In addition to charge-pump clock boosting, the inverter amplifier biased near V_{TH} needs special biasing and common-mode feedback (CMFB) circuitries that can operate with a 0.25 V supply voltage, imposing circuit overhead and additional power consumption.

An alternative approach for designing low-voltage low-power ΔΣ modulator is the substitution of power consuming OTAs by the power-efficient passive integrators [1, 3]. Despite the lack of gain and therefore larger sensitivity to noise coupling inside the loop filter, the passive integrators suggest significant power reduction and ability to operate at low supply voltages. A 0.7 V second-order modulator was implemented in [3] using a fully passive filter and the standard feedback topology. It only consumes 430 nW power while obtaining 70 dB peak SNR. Due to very low signal swings of the passive integrators, high dynamic range signals can be applied at the modulator input. Since digital power is the dominant source of the power consumption in the aforementioned design, scaling down of the power supply could significantly contribute in the overall power reduction. A 0.5 V fully passive modulator was presented in [1] based on the design in [3] using a charge-redistributed gain-boosted passive filter in the second stage, a body-driven gain-enhanced preamplifier prior to the comparator, and a low-voltage comparator circuit. The switch overdrive problem was mitigated by low-V_{TH} transistors while the non-linear sub-V_{TH} leakage current of the critical switches was suppressed by an analog T-switch scheme [14]. The modulator achieves 71 dB peak signal-to-noise-and-distortion (SNDR) from a supply voltage of 0.5 V, while dissipating only 250 nW power. The attained figure of merit (FOM) is 86 fJ/convertion-step, where FOM is calculated as Power/($2^{ENOB}\times 2\times BW$) with *ENOB* as the effective number of bits (or resolution) and *BW* as the input signal bandwidth.

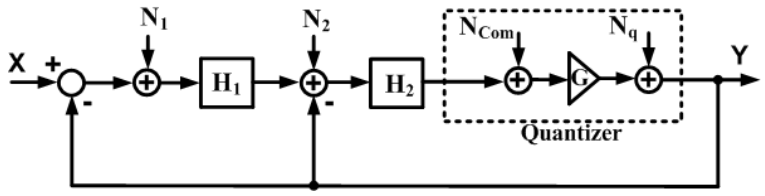

Fig. 4. Noise sources in a single-loop second-order passive modulator [7] (Courtesy of IEEE)

2.3 Performance Limiting Factors

Here the main limiting factors that avoid the passive modulators from obtaining a high-resolution will be discussed. As mentioned before, the lack of gain and significant signal suppression inside the passive loop filter make the design of high-resolution comparator a critical and challenging task. To revisit other issues concerning the comparator design, the linear model of a second-order single-loop modulator, shown in Fig. 4, is considered in which all the noise sources are specified. The base-band output signal can be approximated as:

$$Y \approx X + N_1 + \frac{N_2}{H_1} + \frac{N_{Com}}{H_1 H_2} + \frac{N_q}{G H_1 H_2} \tag{5}$$

where H_1 and H_2 are the integrators transfer functions, N_1 and N_2 are their input-referred noise, respectively, while N_{Com} and N_q represent the comparator input referred noise and quantization noise. Since both filters have no DC gain, only quantization noise obtains some lowpass filtering, due to the loop gain G provided by the quantizer. On the other hand, for a certain SNR the thermal noise (kT/C noise) of the passive filters can be mitigated by scaling up the capacitors size (area penalty). However, N_{Com} is the only noise term that is not subject to any attenuation at low frequencies simply because H_1 and H_2 have no gain. N_{Com} is any non-idealities of the comparator including the thermal noise, low frequency $1/f$ noise, and offset voltage. To alleviate these non-idealities the passive modulator in [2] utilizes a preamplifier whose input devices have a W/L ratio of 200μm/1.2μm, imposing about 0.5 pF at the comparator input. Moreover, in the passive delta-sigma ADCs due to no gain in the stages preceding the comparator, the offset of the overall ADC is defined by that of the comparator [4].

To alleviate the non-idealities of the comparator, several solutions have been tried in the past [5-6] where at least one active stage was used to suppress the input-referred noise and the dc offset.

To summarize, due to a very small signal swing at the quantizer input of the passive ADCs using CIFB topology, the comparator design is a crucial and difficult task, limiting the design scaling to higher-order modulator. In the following section, a fourth-order modulator will be presented that employs three successive passive filters using cascade-of-integrators feedforward (CIFF) topology, resulting in voltage swing improvement at the comparator input. As a result, the comparator design becomes simpler and no power-consuming preamplifier is involved.

3 4-th Order Active-Passive Modulator

In this section we describe both the architecture-level and circuit-level design of a fourth-order active-passive modulator using full feedforward topology.

3.1 Architectural Design

Full feedforward architecture has become popular in recent years for low-power and low-voltage modulator design [8]-[11], [16]. We take advantage of this architecture to improve the voltage swing at the quantizer input, a drawback of the passive modulators using traditional CIFB topology. As a result, the comparator design becomes simpler and no preamplifier stage is required prior to the comparator.

Modulator Topology. Figure 5 shows the block diagram of the single-loop fourth-order modulator topology with single-bit quantizer. An active integrator is used in the first stage, while three SC passive filters are employed in the following stages. The passive filters were described using the transfer function given by equation (1). The feedforward branches are summed at the input node of the quantizer. The optimal coefficients of the designed modulator are calculated from the behavioral simulation and are summarized in Table 1. It must be pointed out that the actual coefficients a_i for i = 2, 3, 4 is $1/(1+\rho)$ which is included into the passive filter transfer function in Fig. 5. The NTF can be calculated as

$$NTF(z) = \frac{z^4 + 2.03z^3 - 11.76z^2 + 13.42z - 4.69}{z^4 - 7.91z^3 - 5.97z^2 - 15.19z + 4.64} \tag{6}$$

The magnitude plot of the NTF is shown in Fig. 6.

Behavioral simulation indicates that the signal amplitude at the quantizer input is 40 mV for a FS input, much lower than the reference voltage, 0.5 V in this design. Since the delta-sigma ADC is a nonlinear block, the equivalent gain of the quantizer can be directly calculated from the simulation.

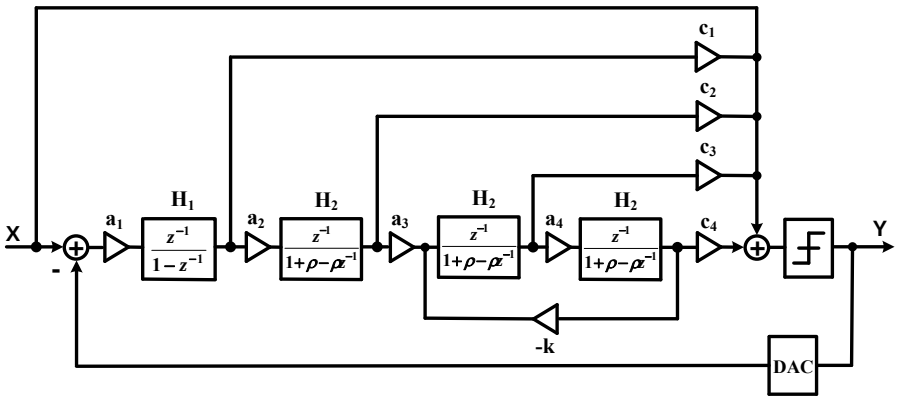

Fig. 5. Block diagram of the single-loop fourth-order full feedforward active-passive ΔΣ modulator with one active integrator in the first stage [7] (Courtesy of IEEE)

Table 1. Modulator coefficients [7] (Courtesy of IEEE)

Filter coefficients	Feedforward coefficients	Resonator coefficient
$a_1 = 0.2$	$c_1 = 2$	
$a_2 = 1$	$c_2 = 3$	$k = 1/64$
$a_3 = 1$	$c_3 = 2$	
$a_4 = 1$	$c_4 = 5$	

A local resonator feedback loop with a gain coefficient of k is used to move a pair of the NTF zeros to the edge of the signal band. In this way, some SNR improvement can be achieved.

Integrators Output Swing. A behavioral simulation with -1.94 dBFS input signal is accomplished to show the integrators output swing and the summed voltage level at the quantizer input. The reference voltage is set to 0.5 V. It is worth to be mentioned that the signal component leaks to the loop filter, due to the attenuation by the passive summation network. As can be seen from Fig. 7, the largest swing is observed at the first integrator output, however it is still within 60% of the reference voltage. The reduced voltage swing enables the OTA, the most critical and power consuming block, to have a relaxed slew-rate requirement, hence low power consumption. The output swing at the succeeding passive integrators decreases continually. As the loop filter in a full feedforward topology ideally only processes the quantization noise [13], the continuous attenuation of the passive integrators does not harm the input signal. In contrast to the feedback or CIFB topology, the feedforward topology has a signal path from the modulator input to the quantizer. Therefore, the voltage level at the quantizer input is still large enough for the comparator to detect it without requiring a stringent preamplifier circuit.

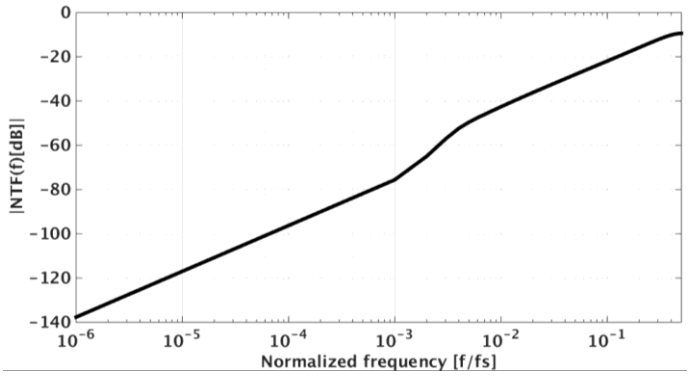

Fig. 6. The NTF magnitude of the designed 4th-order modulator neglecting the resonator

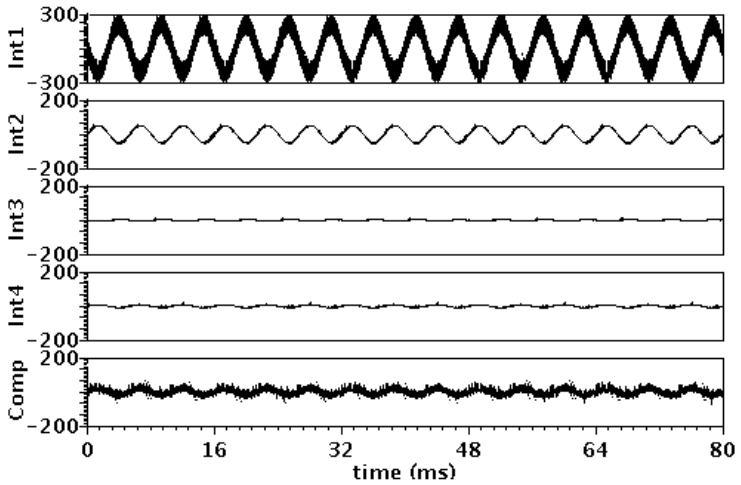

Fig. 7. Integrators output swing in mV using a -1.94 dBFS, 187 Hz input signal. Comp represents the comparator input signal, and *Inti* (*i* = 1-4) represents the *i*th integrator output [7] (Courtesy of IEEE)

More details of circuit design are explained in the following section. One thing should be noted is that, since the single-bit quantizer is used, the integrators in the full feed-forward architecture still contain the attenuated signal component, particularly in the first integrator.

3.2 Circuit-Level Design

This section describes the overall modulator circuit and its building blocks.

Passive Filter Design. The passive filter used as integrator in the second to fourth stages was shown in Fig. 2. The larger ρ places the filter pole to a lower frequency, according to equation (2). Intuitively, the overall loop gain is distributed among the first active pole sector and the quantizer gain, while the low frequency DC gain of the passive integrators is unity.

The parameter $\rho = C/C_s$, in general, is selected so that the -3 dB cut-off frequency, calculated from equation (2), to be placed near the edge of signal bandwidth. The simulation demonstrates that the voltage swing at the quantizer input is almost constant for $\rho \geq 32$, as shown in Fig. 8a. On the other hand, the parameter ρ can also be determined from the SNDR simulations, which consider both the quantization noise and distortion performance. The simulation result shown in Fig. 8b illustrates an optimal ρ of 64. The sampling and integrating capacitors are therefore selected as 0.25 pF and 16 pF, respectively.

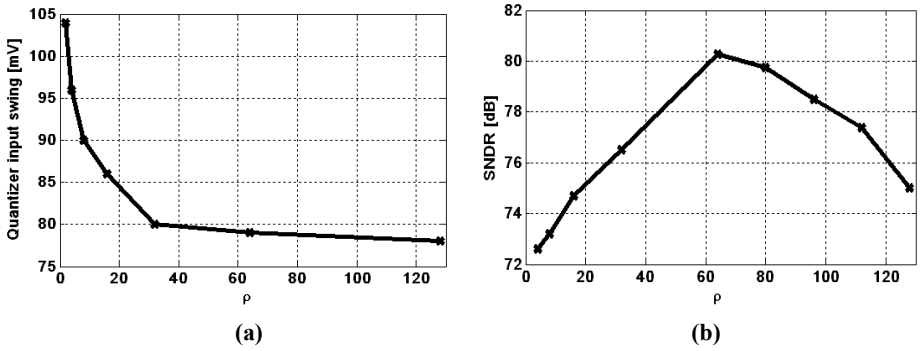

Fig. 8. (a) Simulated voltage swing at the quantizer input; (b) simulated SNDR across ρ. -1.94 dBFS, 187 Hz sinusoidal signal was applied in both cases [7] (Courtesy of IEEE)

In practical implementation of the passive filter (Fig. 2), the parasitic capacitors introduced by the top and bottom plates of the sampling and integrating capacitors can influence the filter transfer function, low frequency gain and pole location, given by equations (1) and (2). Here we examine the effect of these parasitics on the filter's and ΔΣ modulator performance. Considering the filter of Fig. 9a for which the most significant parasitic capacitors are lumped into C_P, the filter transfer function given by equation (1) can be modified to

$$H_P(z) = \frac{-z^{-1}}{1+\rho+\beta-\rho z^{-1}} \tag{7}$$

where $\rho = C/C_S$ and $\beta = C_P/C_S$. Compared to equation (1), the term $\beta = C_P/C_S$ is excessive and is created because of the parasitic capacitor at the internal node. The integrator (filter) loss and -3 dB cut-off frequency can be calculated from equation (7) as follows:

$$A_{0_P} = \left|H_p(z=1)\right| = \frac{C_s}{C_s + C_p} < 1 \tag{8}$$

$$f_{-3dB} = \frac{f_s}{2\pi} \cdot \frac{C_s + C_p}{C + C_s + C_p} \tag{9}$$

where A_{0P} is the magnitude of $H_p(z)$ at DC. Compared to equation (2), the net effect of the parasitic capacitor is the higher passband attenuation (DC gain of less than unity) as given by equation (8) and the shift of the -3 dB cut-off frequency to a higher frequency as given by equation (9), which can degrade the quantization noise suppression. As an example, with f_s = 500 kHz, C_S = 2 pF, C = 64 pF and the estimated

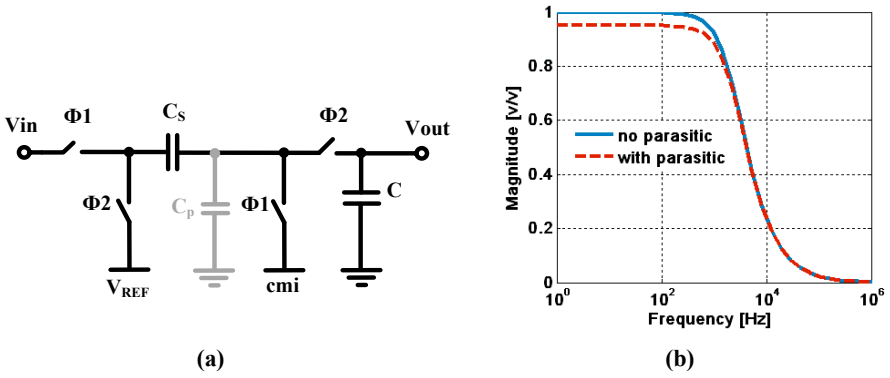

Fig. 9. (a) The basic passive filter associated with lumped parasitic capacitor; (b) the simulated transfer function with/without parasitic capacitor [3] (Courtesy of IEEE)

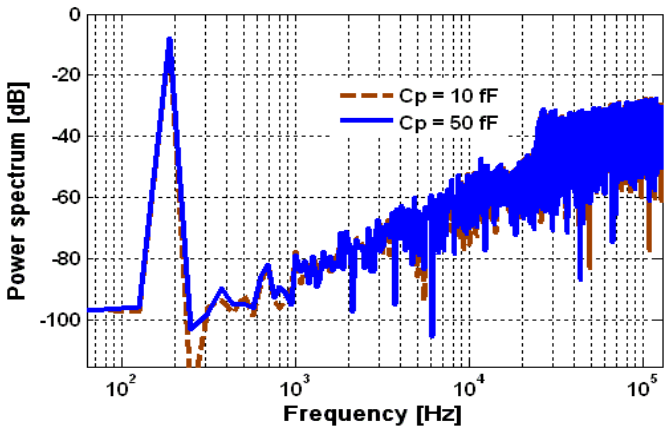

Fig. 10. Simulated output spectra of the fourth-order modulator with addition of 10 fF and 50 fF parasitic capacitor in the passive integrators of the second to fourth stages

C_P = 100 fF, the filter transfer function with/without parasitic capacitor is simulated. Figure 9b indicates that in the presence of C_P the gain decreases from unity to 0.95, while the pole shifts from 2.4 kHz to 2.54 kHz. The results can also be verified by inserting the parameters into equations (8) and (9), showing a good agreement between the simulation results and calculations.

Furthermore, the impact of parasitic capacitors of the passive filters on the overall performance of the designed fourth-order modulator was simulated. Figure 10 shows the power spectra of the modulator with 10 fF and 50 fF parasitic capacitors inserted in the internal node of the passive integrators of the second to fourth stages.

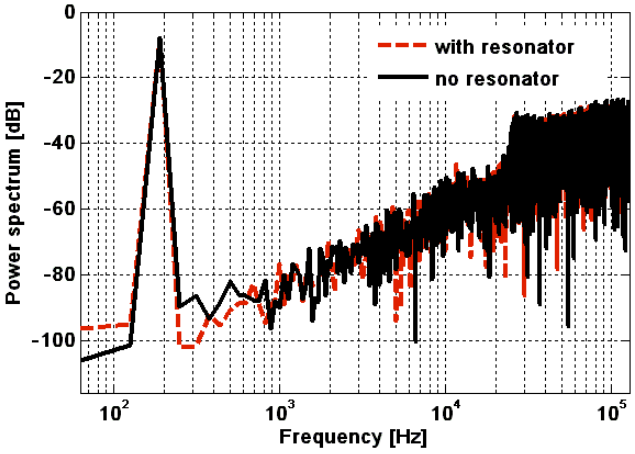

Fig. 11. Simulated output spectra with/without local resonator using a -1.94 dBFS, 187-Hz input signal [7] (Courtesy of IEEE)

The achieved simulated SNDR is 79.6 dB and 77.4 dB from 10 fF and 50 fF parasitic capacitors, respectively. The third and fifth harmonic distortions also grow by 3 dB when the parasitic capacitor value increases from 10 fF to 50 fF. Consequently, the implementation of the sampling and integrating capacitors of the passive filters is very important to avoid large internal parasitics.

Inter-Stage Loading. Another non-ideality which can influence the performance of the passive modulators is the inter-stage loading effect. To explain this, we consider the cascade of two basic passive filters, illustrated in Fig. 2, for the sake of clarity. Figure 12 shows the resulting 2nd-order passive filter and its equivalent model in the sampling phase, Φ1. Clearly seen in Fig. 12b, there is charge-sharing between integrating capacitor C_2 of the first stage and the sampling capacitor C_{S3} of the next stage. During the sampling phase, this charge-sharing may bring up a sampling error, and can reduce the integrator's accuracy. This phenomenon is also called inter-stage loading effect, i.e. the sampling capacitor of the following stage loads the previous stage. The sampled voltage corresponding to the time instance n at node x (Fig. 12b) can be written as

$$V_x(n) = \frac{C_2}{C_2 + C_{S3}} V_{out2}(n-1) \tag{10}$$

One way to prevent the 2nd-order filter (Fig. 12a) from the inter-stage loading is to fully isolate the two passive stages from each other by using a buffer or an active integrator in the middle [5, 6]. However, this is a power-consuming approach, which requires a power-hungry active integrator. Another practical solution to cope with this

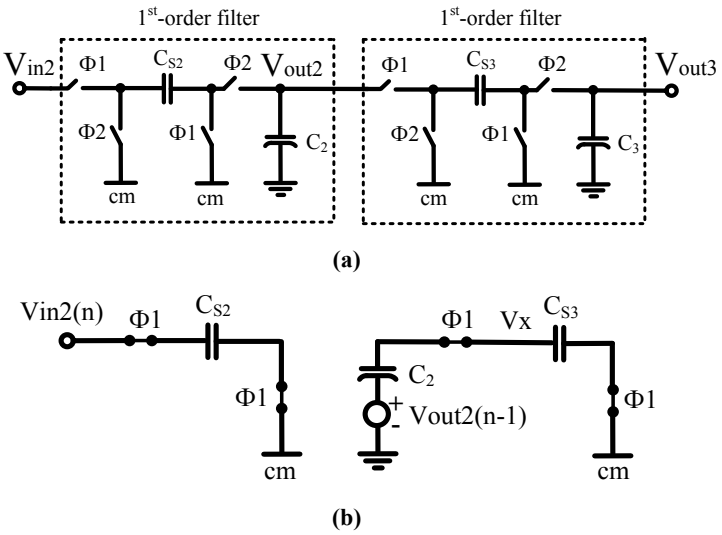

Fig. 12. (a) A 2nd-order passive low-pass filter built from the cascade of two basic passive filters, (b) Equivalent model in sampling phase Φ1

problem is the proper capacitor sizing. By keeping $C_2 >> C_{S3}$ the fraction $C_2/(C_2+C_{S3})$ in (10) approaches one. For instance, in the designed modulator C_2 and C_{S3} are 16 pF and 0.25 pF, respectively. Thus, there is only 1.5% sampling error in the second passive filter, due to charge-sharing. To further decrease the error, relatively larger integrating capacitor C_2 is required, which imposes area penalty and more attenuation. On the other hand, the value of C_2 was obtained from the -3 dB bandwidth requirement given by (2). Clearly, there exist trade-offs among sampling error, pole location, attenuation and area.

Local Resonator. The purpose of the local resonator feedback loop used in the designed modulator is to move a pair of the NTF zeros to the edge of the signal band, improving the in-band noise shaping. The resonator creates a simple negative feedback loop with a gain coefficient k of 1/64. The resonator is simple to be realized using SC implementation (two switches and one small capacitor). Figure 11 shows the simulated output spectra with/without local resonator. A 5 dB SNDR improvement was achieved in this way at the expense of a small area penalty.

Partially Body-Driven Gain-Enhanced Amplifier. Several OTA topologies were designed and carefully analyzed [18-19] for ultra-low-power delta-sigma modulators. Among them a two-stage load-compensated amplifier was selected because of its higher power-efficiency, rail-to-rail voltage swing, and minimal load for a balanced gain-bandwidth (GBW) and phase margin. While two-stage Miller amplifier and single-stage current-mirror OTA have been commonly used for low-power and low-

voltage modulators [8, 20], we exploit the two-stage load-compensated OTA topology because of its privilege in low bias current and low speed environment of the target medical application [21-22]. Due to low bias current (in the range of 100 nA) in this design, the output resistance of the OTA is intrinsically high and the dominant pole of the output load C_L is then placed at very low frequency using a minimal load capacitor value (2 pF load). Therefore, in this low clock speed application the load compensation is preferred to the Miller compensation as it prevents additional power consumption for driving the Miller capacitor.

A fully-differential partially body-driven and gain-enhanced two-stage amplifier with load-compensation was developed for the modulator's input active stage. The detailed circuit is shown in Fig. 13. To reduce the power, the input common-mode level of the OTA is set to 0.35 V (i.e., $V_{DD}/2$), which is limited by the gate-source voltage of M1a-M1b, and the drain-source voltage of M0. Low-V_{TH} transistors are used to provide more headroom for the low-voltage analog design. Meanwhile, the bodies of the p-MOS transistors (i.e., M2, M3, and M6) are tied to half of the V_{DD} (the common-mode level of the ΔΣ modulator) to further decrease the threshold voltage, providing even more operating headroom.

The cascode topologies such as telescopic or folded cascode do not exist in low-voltage analog design, which brings rail-to-rail voltage swing at the cost of restricted DC gain. A body-driven positive feedback is adopted at the output stage (M6a/M6b) to enhance the gain without significant power increase. The transistors M6a and M6b form a cross-coupled connection at their body terminals, which introduces negative

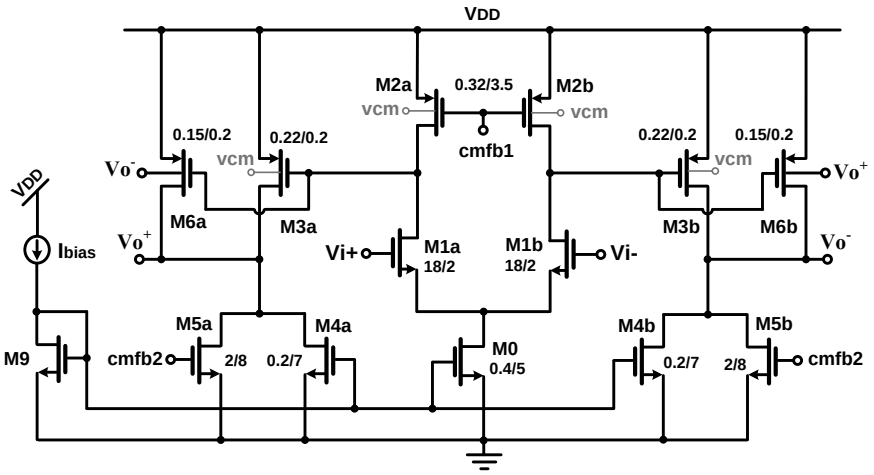

Fig. 13. The proposed two-stage load-compensated amplifier employing body-driven gain-enhancement technique; the bodies of p-MOS transistors are tied to the modulator common-mode voltage vcm = $V_{DD}/2$. Sizes are given in μm unit

conductance -gmb6 at the output nodes (Vo+ and Vo-). In this way, the overall output conductance is effectively decreased, which boosts the total DC gain. The overall DC gain can be expressed as

$$A_0 = \frac{g_{m1}}{g_{ds1} + g_{ds2}} \cdot \frac{g_{m3} + g_{m6}}{g_{ds3} + g_{ds4} + g_{ds5} + g_{ds6} - g_{mb6}} \tag{11}$$

The size of M6a/M6b is chosen such that the conductance gmb6 becomes 65% of the term gds3+gds4+gds5+gds6. With this option the amplifier is stable and gives high enough DC gain. As shown in Fig. 14, with gain-enhancement technique the typical DC gain and GBW increase from 39.6 dB and 670 kHz to 50.4 dB and 1.12 MHz, respectively. Figure 15 also shows the gain and phase plot of the OTA under process and temperature variations (-20°C to +85°C). The worst-case gain and GBW are 43 dB and 600 kHz, respectively, which are adequate for the target SNR, according to system-level simulations. Using typical simulations, the OTA achieves 50.4 dB DC gain, 60° phase margin and 1.2 MHz GBW with a 2 pF load, while dissipating 250 nW power.

Since for a given bias current the gm of the weak inversion transistor is almost five times larger than that of a strong inversion [23], the main transistors (M1, M3, and M6) are driven in the weak inversion region, while other transistors are biased in the moderate inversion region. This can also help to decrease the thermal noise of the mentioned transistors that is represented by $2kT\gamma/g_{m1}$.

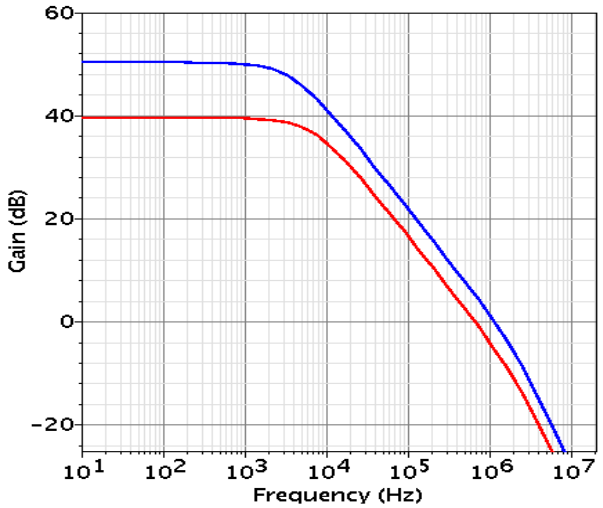

Fig. 14. The simulated typical DC gain with/without gain-enhancement technique

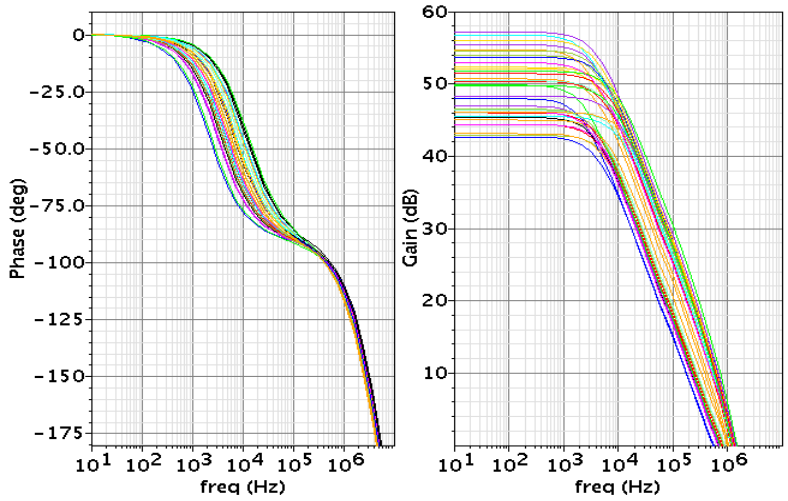

Fig. 15. Bode diagram of the gain and phase response across process and temperature variations

Passive Adder. In the designed modulator a passive SC network is employed for the summation of the feedforward branches in order to avoid power consumption due to an active adder. However, careful design consideration is needed to prevent significant voltage attenuation prior to the quantizer. Figure 16 shows the used adder in its single-ended form. In Φ1 the input and integrators output are sampled onto feedforwarded capacitors *Cf0*-*Cf4*, while in Φ2 these capacitors are discharged. Using superposition principle and the voltage divider across C_{Com}, the output voltage V_{out} can be expressed as

$$V_{Out} = \frac{Cf\,0}{Cf\,0 + C_{Com}} V_{in+} + \frac{Cf\,1}{Cf\,1 + C_{Com}} V_{o1+} + \ldots + \frac{Cf\,4}{Cf\,4 + C_{Com}} V_{o4+} \qquad (12)$$

where V_{in+} is the positive input, V_{oi+} (i = 1-4) is the i-th integrator's output, and C_{Com} models the parasitic capacitor at the comparator input. An important design consideration at this point is to keep the C_{Com} a low value in order to avoid voltage attenuation. In the designed comparator, the estimated input parasitic is less than 100 fF. With this value and the capacitor values listed in Table 2, the output voltage given by (12) reduces to

$$V_{Out} = 0.9V_{in+} + 0.95V_{o1+} + 0.97V_{o2+} + 0.95V_{o3+} + 0.98V_{o4+} \qquad (13)$$

In the modulator block diagram shown in Fig. 5, it is assumed that the input-feedforward coefficient (from input x to quantizer input) is unity. It can be shown that the corresponding STF is one in all frequencies. In modulator realization with passive

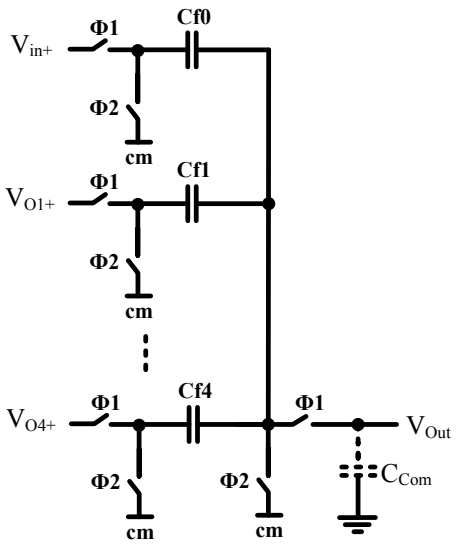

Fig. 16. Passive adder. Single-ended scheme is shown for the sake of simplicity. V_{oi+} (i = 1-4) is the i-th integrator's output, and C_{Com} represents the parasitic capacitor at the input of the comparator

adder shown in Fig. 16, however, the input-feedforward coefficient reduces to 0.9 rather than unity. As a result, the STF can be modified to

$$STF = \frac{0.9 + H}{1 + H} \tag{14}$$

It can be shown that the loop filter H is equal to $0.4H_1+0.6H_1H_2+0.4H_1H_2^2+H_1H_2^3$, where H_1 is the transfer function of the first active integrator, and H_2 is the transfer function of each passive integrator in the following stages (Fig. 5). For the sake of simplicity, the local resonator is omitted and is not considered in the function H. The magnitude plot of the STF is shown in Fig. 17. To summarize, the attenuation due to the passive summation is dealt with a low input parasitic capacitor in the designed comparator circuit. In turn, a power-consuming amplifier in an active adder is prevented, leading to a power-efficient modulator design.

Single-bit Quantizer. The existing passive ADCs [1-5] make use of the traditional CIFB architecture, which primarily suffer from the extreme signal suppression. This makes the comparator design a challenging task. The use of preamplifier stages, as a power consuming solution, prior to the comparator circuit is essential for detecting the very weak signal. As an example, 35% of the total power dissipation in the design presented by [1] comes from the preamplifier.

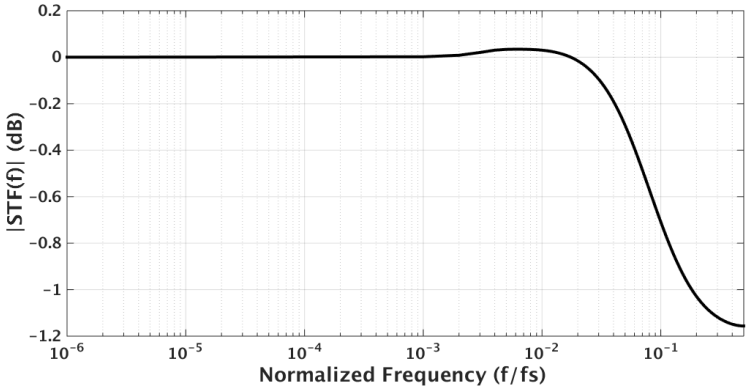

Fig. 17. The STF magnitude of the designed 4th-order modulator

The single-bit quantizer in this design is composed of a dynamic regenerative comparator followed by a SR latch [20]. No pre-amplification stages were used, which lead to a significant power saving. The simple reason is that, compared to the traditional CIFB modulator architecture, the selected CIFF architecture relaxes the voltage swing requirement at the quantizer input. In other words, the voltage amplitude at the comparator input node of the designed feedforward modulator is the sum of the input signal, the first active integrator's output swing and the attenuated output swing from the succeeding passive integrators, which is relatively larger than that of a modulator implemented by a CIFB structure. This can be clearly seen in Fig. 7. We then utilize a simple and power-efficient quantizer circuit without pre-amplifications [7]. The circuit schematic is shown in Fig. 18. When clock signal *clk* goes low, the nodes *x* and *y* are precharged to V_{DD}. While *clk* goes high, the precharged nodes start to discharge to ground by transistors M1a and M1b. The amount of discharge currents depend on the input signals. The cross-coupled transistors, M3a and M3b, form a positive feedback loop and amplify the difference in the inputs to a full-rail output. As the comparator is a dynamic circuit and is clocked by the non-overlapping clock phases, a slow clock causes leakage current flow through the branches. Therefore, high-V_{TH} and low-power (hvtlp type) transistors of the used 65 nm CMOS technology were utilized to suppress the leakage. The total power consumption of the comparator and latch is less than 10 nW.

Complete Modulator Circuit. The overall modulator circuit is shown in Fig. 19. It employs a fourth-order loop filter implemented by single-loop full feedforward architecture. It has four integrators including an active one in the first stage and three passive ones in the following stages. The summation at the quantizer input is performed by using a SC network. A simple dynamic comparator is utilized as single-bit quantizer, while the power consuming preamplifier is removed in total.

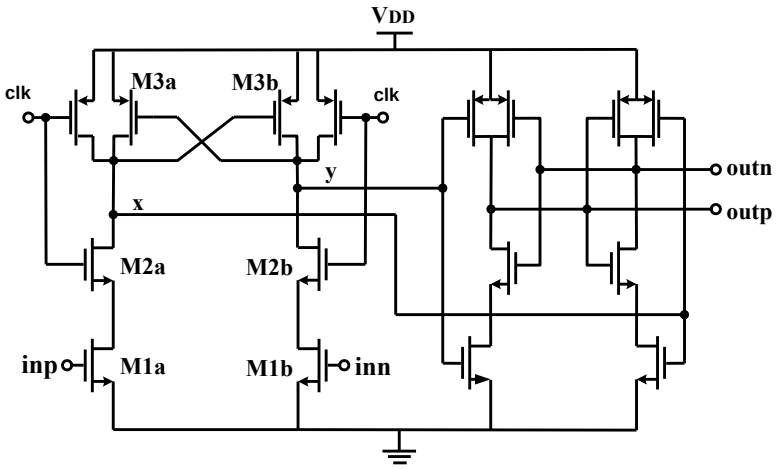

Fig. 18. Dynamic comparator and SR latch

A basic resonator feedback composed of two switches and a small capacitor C_b is employed to optimize the NTF's zero location near the edge of signal bandwidth. A 5dB SNR improvement can be obtained according to the simulation. The common-mode voltage is set to the middle of the power supply, i.e. 0.35 V. The reference voltage is set to 0.5 V, which is defined by V_{REFP} of 0.6 V and V_{REFN} of 0.1 V.

The capacitor value of the first integrator (i.e., C_{S1}) and the signal feedforward path (i.e., C_{f0}) are selected to fulfill the kT/C noise requirement of the modulator with a safe margin [10]. The other modulator sampling and feedforward capacitors (i.e., C_{Si} and C_{fi} for i = 2, 3, 4) are chosen to satisfy the modulator coefficients listed in Table 1. The first integrating capacitors (i.e., C_1) is chosen to realize the coefficient a_1 = 0.2, while the rest of the integrating capacitors (i.e., C_i for i = 2, 3, 4) are selected from the passive filter requirement, as discussed in section 3.2. It is worth to be pointed out that the first active stage suppresses the thermal noise or kT/C noise of the succeeding passive filters, thereby reducing the capacitor sizes drastically. Moreover, the resonator capacitor C_b is 0.25 pF in order to realize the resonator gain coefficient of 1/64. The capacitor values are summarized in Table 2.

4 Simulation Results

The proposed modulator was designed in a 65 nm CMOS technology and was simulated using a 256 kHz sampling clock frequency. Table 3 summarizes the simulation results. The modulator achieves 84 dB and 80.3 dB peak SNR and peak SNDR, respectively, from a 0.7 V supply. A -2.85 dBFS (i.e., 0.18 V peak amplitude), 109 Hz differential input signals were applied to the modulator input, while the reference

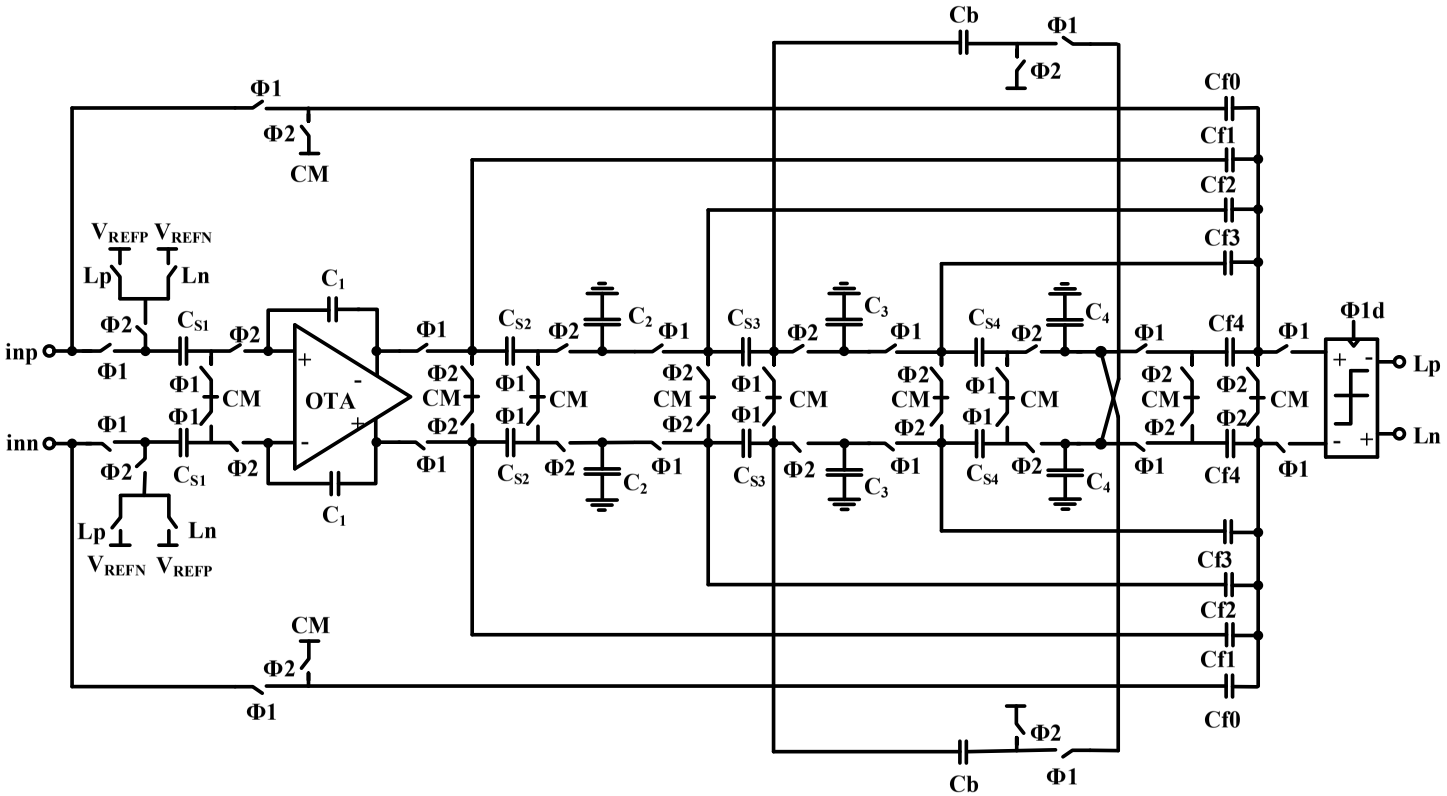

Fig. 19. Schematic of the proposed fourth-order active-passive modulator [7] (Courtesy of IEEE)

Table 2. Capacitor values in pF [7] (Courtesy of IEEE)

Sampling capacitors	Integrating capacitors	Feedforward Capacitors	Resonator coefficient
		$Cf_0 = 1$	$Cb = 0.25$
$C_{S1} = 1$	$C_1 = 5$	$Cf1 = 2$	
$C_{S2} = 0.25$	$C_2 = 16$	$Cf_2 = 3$	
$C_{S3} = 0.25$	$C_3 = 16$	$Cf_3 = 2$	
$C_{S4} = 0.25$	$C_4 = 16$	$Cf_4 = 5$	

voltage was set to 0.5 V (i.e., V_{REFP} of 0.6 V and V_{REFN} of 0.1 V), as shown in Fig. 19. The simulated output spectrum is shown in Fig. 20. Figure 21 shows the modulator peak SNDR with respect to the oversampling ratio (OSR). When the modulator is run at 1.0 MHz sampling frequency, the attained SNDR is 86 dB while dissipating 650 nW power. The input differential range is 1 V_{PP}.

Compared to the previous passive modulator in [3], the clock frequency is halved by using higher-order filter, beneficial for power reduction in the ADC and the following decimating filter. Significant SNR improvement was achieved by cascading four integrators and also alleviating the low swing at the quantizer input with input feedforward architecture. It is important to point out that the total capacitor area is estimated to be scaled down by 50%, as compared to the fully passive modulator presented in [3]. The total sum of all capacitor values in the passive ADC in [3] and the proposed fourth-order active-passive modulator is 280 pF and 138 pF, respectively.

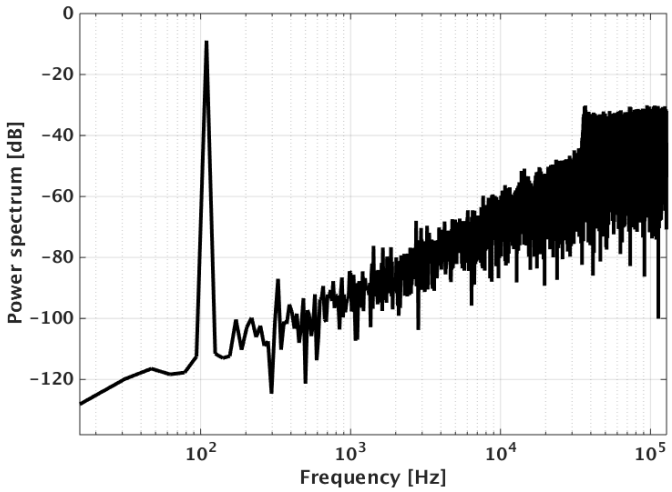

Fig. 20. Simulated modulator output spectrum with a -2.85 dBFS, 109 Hz input and 16384-points FFT [7] (Courtesy of IEEE)

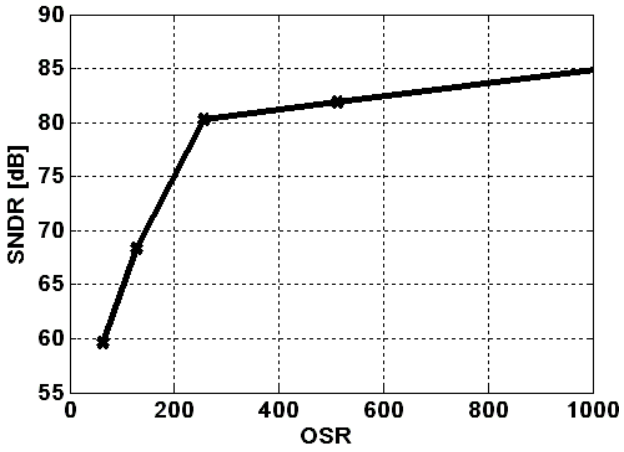

Fig. 21. Simulated SNDR versus oversampling ration OSR [7] (Courtesy of IEEE)

Table 3. Perfprmance results [7] (Courtesy of IEEE)

Technology	65 nm CMOS	
Supply Voltage	256 kHz	1.024 MHz
Clock Frequency	0.7 V	
Signal Bandwidth	500 Hz	
Input range	1.0 V differential	
Peak SNR	84 dB	92.8 dB
Peak SNDR	80.3 dB	86 dB
Power	400 nW	650 nW

5 Comparison of the Power Efficiency

The performance of the presented modulator in section 3 is compared with previously reported modulators using passive filter(s) in Table 4. Two commonly used FOMs (Walden and Schreier FOMs) are defined below:

$$FOM_W == \frac{Power}{2^{(SNDR-1.76)/6.02} \times 2 \times BW} \tag{15}$$

$$FOM_S = DR_{dB} + 10\log(\frac{BW}{Power}) \tag{16}$$

Table 4. Performance comparison with previously reported modulators using passive filter

Reference	Type	BW [Hz]	Sampling Rate[MHz]	SNDR [dB]	DR [dB]	Power [μW]	FOM_W[a] [pJ/step]	FOM_S[b]
[2] Chen	DT Passive	20k	10	67	78	250	3.41	157
[4] Chen	DT Passive	100k	104	74.1	80.5	830	1.0	159.7
[5]Yousry[e]	DT APDSM[c]	10M	640	56	54	5500	0.55	146.6
[6] Das	CT APDSM[d]	600k	256	N/A	86	5400	N/A	166.5
[3] Fazli	DT Passive	0.5k	0.5	65	65	0.43	0.3	144
[3] Fazli	DT APDSM	0.5k	0.25	70	70.5	1.27	0.49	156.5
[7] Fazli[e]	DT APDSM	0.5k	0.256	80.3	84	0.4	0.05	175

(a) FOM_W = Power/($2^{ENOB}\times 2\times BW$) known as the Walden FOM

(b) FOM_S = *DR*(dB)+10log (*BW*/*Power*) known as the Schreier FOM

(c) DT-APSDM = Discrete-Time Active-Passive Delta-Sigma Modulator

(d) CT-APSDM = Continuous-Time Active-Passive Delta-Sigma Modulator

(e) Simulation results were provided in [5, 7]

The FOM_W favors low-resolution ADCs, whereas the FOM_S favors high-DR ADCs. The passive modulator presented in [3] with 0.43 μW power consumption and medium resolution (68 dB SNR from a 0.7 V power supply) looks attractive when using FOM_W definition, as given by equation (15). When considering FOM_S, the hybrid second-order and fourth-order modulators present the FOM of 156.5 and 175, respectively, which demonstrate high power-efficiency among the modulators [2-6]. In particular, the fourth-order modulator in [7] employing a feedforward architecture presents an excellent energy-efficiency when both FOM_W and FOM_S are applied.

6 Summary

The ultimate purpose of this design was to improve the ADC resolution by solving some of the fundamental problems associated with the traditional passive modulators, discussed in section 2, such as extremely low voltage swing at the quantizer input and the comparator non-idealities including offset and noise. Furthermore, cascading three passive filters became possible by using feedforward modulator architecture.

Significant power reduction was obtained through (i) the reduced clock frequency by using a fourth-order and power-efficient loop filter, (ii) the removal of the power consuming preamplifier and (iii) the relaxed amplifier performance requirements in the full feedforward modulator structure.

The main advantage of the first active filter is that it can suppress the comparator nonidealities to a high extent. Additionally, due to the gain of this stage the thermal noise from the succeeding passive filters is also attenuated, resulting in significant capacitor area reduction.

Since in the feedforward architecture the loop filter mainly processes the quantization noise, the continual attenuation along with the passive integrator does not harm the signal components, another advantage of using passive stages in the feedforward structure. Therefore, three cascades of passive filters were exploited to create higher-order noise-shaping, which can decrease the OSR or sampling clock frequency leading to huge digital and analog power reduction. Furthermore, the input feedforward structure is suited well for low-power ΔΣ modulator design due to offering low integrators swing, which relaxes the slew rate requirement of the OTAs. Therefore, the slew rate and GBW of the OTA in the active stage were scaled down.

The impact of parasitics of the sampling and integrating capacitors on the performance of passive filter and the overall modulator was investigated and the simulation results were included.

Compared to the second-order passive modulator implemented in 65 nm technology [3] using distributed feedback architecture, the clock frequency in the proposed modulator reduced from 500 kHz to 256 kHz, which is beneficial for both analog performance scaling down and digital power reduction. The SNDR improved from 65 dB to 80 dB (2.5-bit resolution improvement), while the attained power of 400 nW is in the same order as the previous design (i.e., 430 nw). In other words, the power-efficiency (or FOM) of the overall modulator was enhanced from 296 fJ/step to 47 fJ/step, showing the effectiveness of combined feedforward structure and cascade of passive integrators. The attained FOM of 47 fJ/step makes this design a suitable candidate for low-voltage low-power ADC designs intended for medical applications.

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