

# Natural Interpretation of UML/MARTE Diagrams for System Requirements Specification

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in real-time temporal logic MTL (Metric Temporal Logic) extending LTL. Finally the research work, DDPSL (Drag and Drop PSL) [16], presents a template library defining PSL formal properties using logical and temporal operators. The research community of *runtime verification* [17] relies on lightweight formal verification techniques based on LTL/CTL. It check the correctness of the behavior of a system with the focus on generation of efficient observers for online monitoring. As opposed to this, our proposed framework targets the integration of observers in a complete work-flow. The focus here is on the presenting a natural way to model temporal behavior.

We also promote the use of graphical models over the use of temporal logic formula. Indeed, while temporal logic like LTL/CTL, are widely used in the later design stages in conjunction with model-checkers [18], they are not suitable to directly express high-level requirements at early stages. They are commonly rejected by requirements engineers [19] despite the various attempts to alleviate the syntax with higher-level constructs like in PSL (Property Specification Language) [20]. So we endorse to loose the expressiveness of LTL if we have a clear and formal graphical way of defining properties. Moreover, the domain of expressiveness of CCSL (used in our approach) is different from LTL and LTL-based languages (like PSL) [21]. Here we are interested to express properties on logical clocks for which LTL is not an obvious choice. Also LTL is not meant to express physical time properties, for which, this framework prefer the use of CCSL. Moreover, PSCs do not benefit from the popular embedded systems modeling and analysis profiles like MARTE. Rather than encoding formula with UML extensions, we propose to reuse UML/MARTE constructs to build a set of pre-defined property patterns pertinent for the domain addressed.

Another aspect of the related work is the advent of Formal Specification Level (FSL), still an informal level of representation. The focus of the FSL approach is to transform natural language descriptions directly into models bridging the design gap. On the other hand, our proposed framework targets the graphical representation of temporal properties replacing the need for textual specification of the system. *Natural language front-end* is a general trend to allow for a syntax-directed translation of concrete pattern instances to formulae of a temporal logic of choice, also used in [15]. Our framework approach is different from the FSL approach as we target the verification and validation of a subset of behavior rather than the complete system. Design engineers are usually well acquainted to UML diagrams and any graphical alternative to complex CCSL or LTL/CTL notations is more likely to get wide acceptance. Moreover, the use of MARTE profile allows to reuse the concepts of time and clocks to model timing requirements of embedded systems.

### III. UML/MARTE SEMANTICS

This paper proposes an approach to interpret the UML diagrams in a natural way. Hence this section introduces UML state of the art. UML itself lacks the notion of time which is essentially required in modeling temporal patterns. So selected features from the MARTE time model are explained which are used to facilitate semantically sound representation of time.

#### A. UML *State of the Art*

UML *state machine diagrams* [22] provide a standardized way to model functional behavior of state-based systems. They provide behavior to an instance of a class (or object). Each state machine diagram basically consists of states an object can occupy and the transitions which make the object change from one state to another according to a set of well defined rules. Transitions are marked by guard conditions and an optional action. Among the set of state machine elements defined, only a small subset is used by the presented approach to represent graphical properties by giving specific semantics to that chosen subset. The presented approach specifies  $S$  as a set of finite states consisting of simple states and final states while the other states (like initial pseudo-states and choice pseudo-states) are not used at all. From the standard set of state machine elements, only the top region is used while all other set of regions like in state hierarchy are not considered. Finally, the state machine is considered to have a finite set of valid transitions.

#### B. MARTE Time Model

The proposed approach uses concepts of clocks and time for which MARTE time model [3] is utilized. MARTE time model provides a sufficiently expressive structure to represent time requirements of embedded systems. In MARTE, time can be physical, considered as dense or discrete. But it can also be logical and related to user-defined clocks. Time may even be multiform, allowing different times to progress in a non-uniform fashion, and possibly independently to any (direct) reference to physical time. At the heart of the MARTE Time sub-profile, the stereotype *ClockType* extends the metaclass *Class* while the stereotype *Clock* extends metaclasses *InstanceSpecification* and *Property*. Clocks can appear in structural diagrams (like SysML block definition or UML composite structure) to represent a family of possible behaviors. This clock association gives an ability to the model elements identifying precisely instants or duration.

## IV. OBSERVATION PROFILE

The combined features of UML and MARTE provide a base for developing timed-models but they still lack the specialized features to model graphical temporal patterns. This section presents the first contribution of this paper in the form of a UML profile extension targeting temporal patterns. We introduce the *Observation profile* which is designed to target the expressiveness of graphical temporal properties. This profile resides on top of the UML/MARTE to provide a structure for building some predefined patterns. The focus of the presented work is not the minimalist approach but rather the expressiveness of the property from the system designer's point-of-view. So when a property specifies occurrence of something at some point in time, then it is an event and it seems natural to represent such properties as logical clocks. But when the properties specify duration or interval (not a particular point in time), then the obvious choice of representation is state relations.

In the proposed approach, extended state machine diagrams are mainly used to represent the behavior patterns of a system. These diagrams provide a more natural and syntactically

sound interpretation of graphical behavioral patterns of system states. State machines are used to model state-based relations represented graphically in the form of scenarios. Two basic scenarios are possible: negative and positive. These scenarios act as building blocks for more complex state patterns.

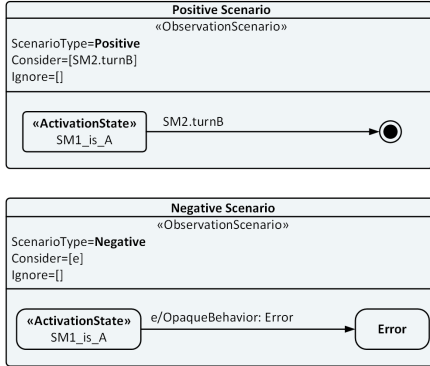


Fig. 1: Positive and Negative Scenarios

*Positive scenarios* model something that must happen under given conditions, as shown in Figure 1. Two types of stereotypes are used in this scenario. The *ObservationScenario* stereotype extends the UML state machine metaclass. It defines further three tagged values: ScenarioType, Consider and Ignore. *ScenarioType* is the basic type of the scenario. *Consider* contains the collection of all the events that are relevant to this scenario. It is just like the sensitivity list in SystemC, Verilog or VHDL. If the list of relevant events is large, then the list of events that are not relevant maybe modeled using the *Ignore*. Another stereotype applied to the scenario is the *ActivationState* stereotype. It extends the UML state metaclass and is used to identify the state that activates this particular scenario. It is active whenever the system is in a specific condition. The positive scenario expects an event to occur whenever the considered state is active. Failure occurs if the event does not occur. The scenario terminates normally if the desired event occurs. In Figure 1, the positive scenario represents the relation *State A starts State B*. Hence one state is ensuring to start another state at the same time, which is a very common behavior in systems.

*Negative scenarios* model something that must not happen under given circumstances. So when the state machine is active, it checks for a particular trigger event that leads the system to a violation/error state shown in Figure 1. This type of properties can use model-checking to detect if the system under observation ever reaches an error state. The negative property in the figure models the relation *State A excludes Event e*, which means the event e is not possible while the state is A. One other stereotype applied optionally to the states is the *Duration* stereotype used to model delay in some cases of temporal patterns (not shown here). It also extends the UML state metaclass. Figure 2 shows the proposed Observation profile as a collection of all these presented stereotypes.

## V. PROPOSED TEMPORAL PATTERNS

The major contribution of this proposed approach is to provide a set of reusable generic graphical temporal patterns. For identifying the temporal properties of systems, we started

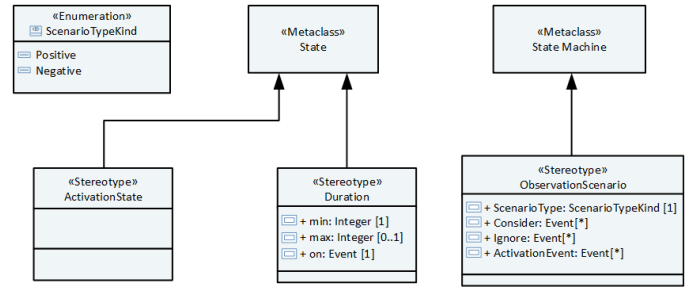


Fig. 2: Proposed Observation Profile

by considering several examples like the stream boiler case study [5], railway interlocking system [6] and the traffic light controller case study [7]. Working on these diverse examples to model behavioral properties in UML, we extracted several recurring temporal patterns. These patterns collected across various examples were refined with some inspiration taken from the Allen’s algebra targeting intervals [23]. This practice gave us a valuable collection of generic patterns divided into three major categories of behavioral relations that may exist in a system: state-state relations, state-event relations, and event-event relations. Researchers have already shown that constraints specified in CCSL are capable of modeling logical event-event temporal relations [24]. These CCSL constraints can be represented graphically using SysML/MARTE models [25]. Temporal patterns for the other two categories of relations are:

**State-State Relations:** precedes, triggers, contains, starts, finishes, implies, forbids, and excludes.

**State-Event Relations:** excludes, triggers, forbids, contains and terminates.

Next subsections discuss selected few of these temporal patterns. These patterns with their syntax and semantics are discussed in detail in an online report [26].

### A. State-State Relations

Presented approach including the two basic scenarios can be used to formally model relations between two different states of a system. Allen’s algebra [23] for intervals provides a base defining thirteen distinct, exhaustive and qualitative relations of two time intervals. From the comparative analysis of these relations, six primitive relations are extracted that can be applied to the state-based systems. Further two ‘negation’ relations are added (forbids, excludes), based on their usage and importance in the examples, to complete the set.

Semantically a state can be considered similar to an interval. We use the nomenclature of using capital letters (A,B,...) to denote states and small letters (a,b,...) for events/clocks. Dot notation like SM1.turnA is also used throughout the text to show the specific events. Given a strict partial ordering  $\mathbb{S} = \langle S, < \rangle$ , a state in  $\mathbb{S}$  is a pair  $[a_s, a_f]$  such that  $a_s, a_f \in \mathbb{S}$  and  $a_s < a_f$ . Where  $a_s$  is the start and  $a_f$  is the end of the state interval. An event or point e belongs to a state interval  $[a_s, a_f]$  if  $a_s \leq e \leq a_f$  (both ends included).

**Precedence** is an important state property where the relation ‘A precedes B’ means the state A comes before the state

B. It includes a delay/deadline clause to explicitly specify the duration between the termination of state A and the start of state B. Use of precedence relation with specific delay can also be equated to the triggers state-event relation (e triggers A after [m,n] on clk). The unit of the duration is dependent on the level of abstraction that is target of the graphical specification, i.e., it can be physical clock, loosely timed clock, or logical clock. Deadline defers the evaluation of state A until some number of ticks of clk (or any other event) occur. The number of ticks of clk considered are dependent on the two parameter natural numbers min and max evaluated as:

- [0, n] means ‘before n’ ticks of clk
- [m, 0] means ‘after m’ ticks of clk
- [m, m] means ‘exactly m’ ticks of clk

Mathematically, given a partial ordering  $\mathbb{S}$  having the states A ( $[a_s, a_f]$ ) and B ( $[b_s, b_f]$ ), a constant  $n$  and a clock  $clk$ , the equation

$$A \boxed{\leq} B \text{ by } [m, n] \text{ on } clk$$

means  $a_f \leq b_s$  and  $b_s$  occurs within the duration  $a_f + \Delta$ , where  $\Delta$  is between m and n ticks of event  $clk$ . The last tick of clk coincides with the start the state B (i.e,  $b_s$ ). Graphically, precedence is based on positive scenarios shown in Figure 3. The first state (State\_is\_A) is an activation state (shown by the stereotype) while the second state has the duration stereotype applied to specify the interval. The observation scenario gets active when the state machine SM1 gets in A state. It then checks for the state exit (turnNotA) and expects the other state machine SM2 to be in state B within the specified time duration. If this behavior occurs as desired, then the scenario goes dormant till the next state activation occurs.

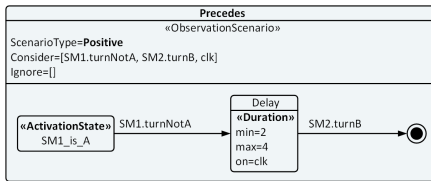


Fig. 3: A precedes B by [2, 4] on clk

**Forbiddance** is a negation property. Relation ‘A forbids B’ bars B to occur after state A occurs. It has another slightly different operator that works with events (e forbids A), discussed later on. Hence mathematically, given a partial ordering  $\mathbb{S}$  having the states A ( $[a_s, a_f]$ ) and B ( $[b_s, b_f]$ ), the equation  $A \boxed{\neg} B$  means  $b_s \neq a_f$ . Its graphical temporal pattern is shown in Figure 4. Scenario activates whenever SM1 is in state A and on exiting this state, the SM2 is expected to be not in state B (else violation occurs).

**Exclusion** between two states restricts them to occur at the same time. Mathematically, given a partial ordering  $\mathbb{S}$  having the states A ( $[a_s, a_f]$ ) and B ( $[b_s, b_f]$ ), the relation ‘A excludes B’ means that  $b_f < a_s$  or  $a_f < b_s$  for all instances of A and B. This relation can be decomposed into two basic state-event exclusion relations (shown without boxed symbols).

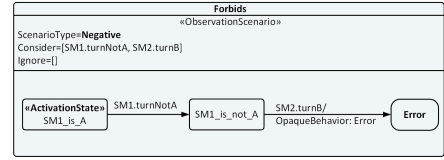


Fig. 4: A forbids B

$$A \# bs \text{ and } B \# as$$

Graphically, this temporal pattern is derived from the exclusion relation of state and event (discussed in the next sub-section). Two negative scenarios are used to model this behavior as shown in Figure 5. So during the particular state A for SM1, the event turnB is expected not to occur and vice versa for the other case.

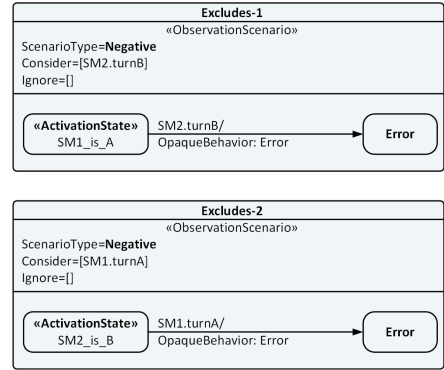


Fig. 5: A excludes B

## B. State-Event Relations

The relations between the system states and events can be modeled using the UML sequence diagrams or state machine diagrams. Here in this text we will only focus on the state machine based patterns. Based on the use, we discuss two state-event relations here.

The **excludes** relation *state A excludes event e* is a bijective relation. Mathematically, given a partial ordering  $\mathbb{S}$  having the state A ( $[a_s, a_f]$ ) and a clock  $e$ , it can be expressed as  $A \# e$  where  $e \notin [a_s, a_f]$ . It implies either  $e < a_s$  or  $a_f < e$ . Graphically it is modeled using a negative scenario, as shown in Figure 6. Here the SM1 while in state A, will cause error on event  $e$ .

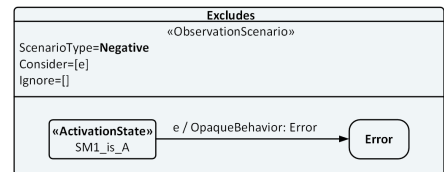


Fig. 6: A excludes e

The **terminates** relation is similar to finishes relation for states. The relation *event e terminates state A* can be expressed mathematically, given a partial ordering  $\mathbb{S}$  having the state A ( $[a_s, a_f]$ ), an event  $e$ , a constant  $n$  and a clock  $clk$ , as

$$e \Rightarrow A \text{ after } [m, n] \text{ on } clk$$

It means  $a_f$  occurs within the duration  $e + \Delta$ , where  $\Delta$  is between  $m$  and  $n$  ticks of event  $clk$ . Graphically, it is implemented using the positive scenario state machine, as shown in Figure 7.

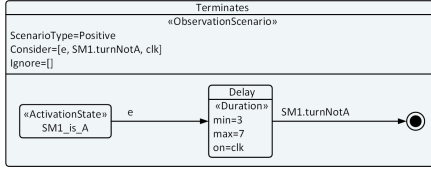


Fig. 7:  $e$  terminates A after [3,7] on  $clk$

## VI. APPLICATION OF TEMPORAL PATTERNS

Utility of temporal patterns is shown through a case study of traffic light controller taken from SystemVerilog Assertions Handbook [7]. It consists of a cross-road over North-South highway and the East-West farm road. There are sensors installed for the emergency vehicles and for the farm road traffic. Highway traffic is only interrupted if there is a vehicle detected by the farm road sensor. The architecture for the traffic light controller consists of two state machines, interface signals of the module and the timers. A few temporal verification properties of the design are discussed next.

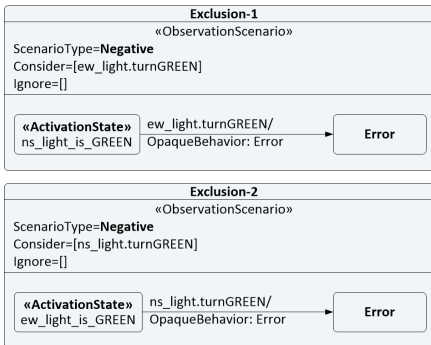


Fig. 8:  $ns\_light=GREEN$  excludes  $ew\_light=GREEN$

**Safety property, Never NS/EW lights both GREEN simultaneously.** This property is the exclusion of two states  $ns\_light.GREEN$  and  $ew\_light.GREEN$ . From our library of graphical temporal patterns, we consider two state-event excludes temporal patterns as shown in Figure 8. Here if  $ns\_light\_is\_GREEN$  is the activation state from SM1, then in the generic pattern we replace the event  $e$  with the start event of the opposite signal ( $turnGREEN$  of  $ew\_light$ ).

**State of lights at reset.** This constraint requires that whenever reset occurs, the  $ns\_light$  turns off. This property

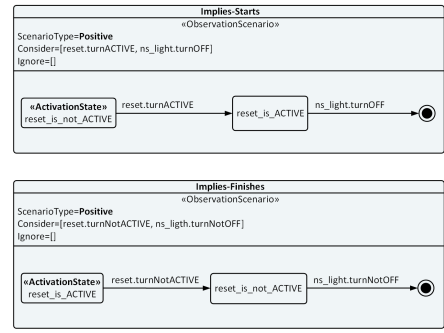


Fig. 9:  $reset=ACTIVE$  implies  $ns\_light=OFF$

shows that  $ns\_light.OFF$  is the consequence of reset. From our library of graphical properties, we use the implies operator for the relation, shown in Figure 9. The implies relation is like the excludes state-state relation as it is further composed of two state-state relations: *starts* and *finishes*. The starts relation guards the beginning of implies relation while the finishes guards the end of the implication relation. Both the relations are implemented using positive scenarios.

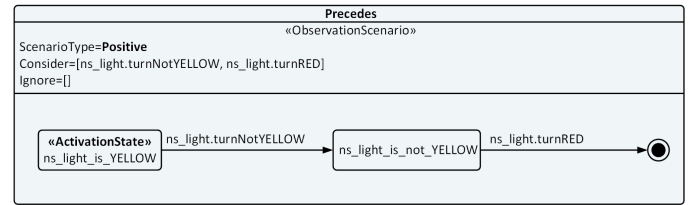


Fig. 10:  $ns\_light=YELLOW$  precedes  $ns\_light=RED$

**Safety, GREEN to RED is illegal. Need YELLOW.** This constraint is an example of the difference between the textual specification and the constraint implemented as assertion. Though the YELLOW state is specified in the text but it is never tested in the actual SystemVerilog assertion. Here the graphical approach is clear and precise in using the *precedes* relation for states (without defining any delay), shown in Figure 10. Here the name of the state ' $ns\_light\_is\_not\_YELLOW$ ' is not required (as it is not an activation state), and any desired name can be used. The property here ensures YELLOW comes before RED. To avoid cases like  $YELLOW \Rightarrow GREEN \Rightarrow RED$ , we can add another constraint  $ns\_light=GREEN$  precedes  $ns\_light=YELLOW$ . A little varying intent can also be implemented using the forbids relation  $ns\_light=GREEN$  forbids  $ns\_light=RED$  which seems to be the desired one for the text 'green to red is illegal'.

**Verification:** Graphical interpretation of properties are implemented in the form of *observers*. Verification by observers is a technique widely used in property checking [27]. They check the programs for the property to hold or to detect anomalies. In the presented framework, each temporal pattern is finally transformed into a unique observer code for a specific abstraction level (like register transfer level - RTL). It proposes to create a library of verification components for each graphical temporal pattern. An observer provides implementation to the semantically sound graphical patterns. An observer consists of a set of input parameters, one for each activation state and

event. A special violation output is there to flag any anomaly in the behavior. The way these patterns work is by relying on *adapters* as a glue logic. These adapters convert the signal or group of signals from the system to states and events. The property patterns implemented in the framework use these events and states. So adapters come in-between the module under verification and the observers. They receive inputs in the form of design module interface signals and state values. From this they generate the appropriate logical clock outputs and state identifiers to be consumed by the observers.

## VII. CONCLUSION AND FUTURE WORK

This paper presents a natural way to interpret UML diagrams annotated with features from MARTE to specify system requirements. It proposes a graphical approach to capture properties in a bid to replace temporal logic properties like in LTL. It also proposes a way to extend the existing capabilities of CCSL which can though represent state relations but is not practically meant for that task. The proposed approach identifies two major categories of temporal patterns, state-based and mixed state/event relations. Semantics of the states in both types of properties have been expressed as *state-start* and *state-end events*. An exhaustive set of state relations, based on Allen's work, have been proposed. Later these relations are implemented using a subset of state machine diagrams and sequence diagrams coupled with features from MARTE time model and Observation profile.

In the future, we wish to extend this work as a complete framework providing a comparative analysis of the presented operators with that of existing CCSL operators and code generation from the graphical properties. In regards to this continued effort, a tool plugin has been developed [28] for model transformation of such graphical patterns directly into CCSL and Verilog HDL based observers.

## ACKNOWLEDGMENT

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