



Hardware and Arithmetic for Hyperelliptic Curves Cryptography

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► To cite this version:

Arnaud Tisserand, Gabriel Gallin. Hardware and Arithmetic for Hyperelliptic Curves Cryptography. CominLabs Days 2016, Nov 2016, Rennes, France. , 2016. hal-01404755

HAL Id: hal-01404755

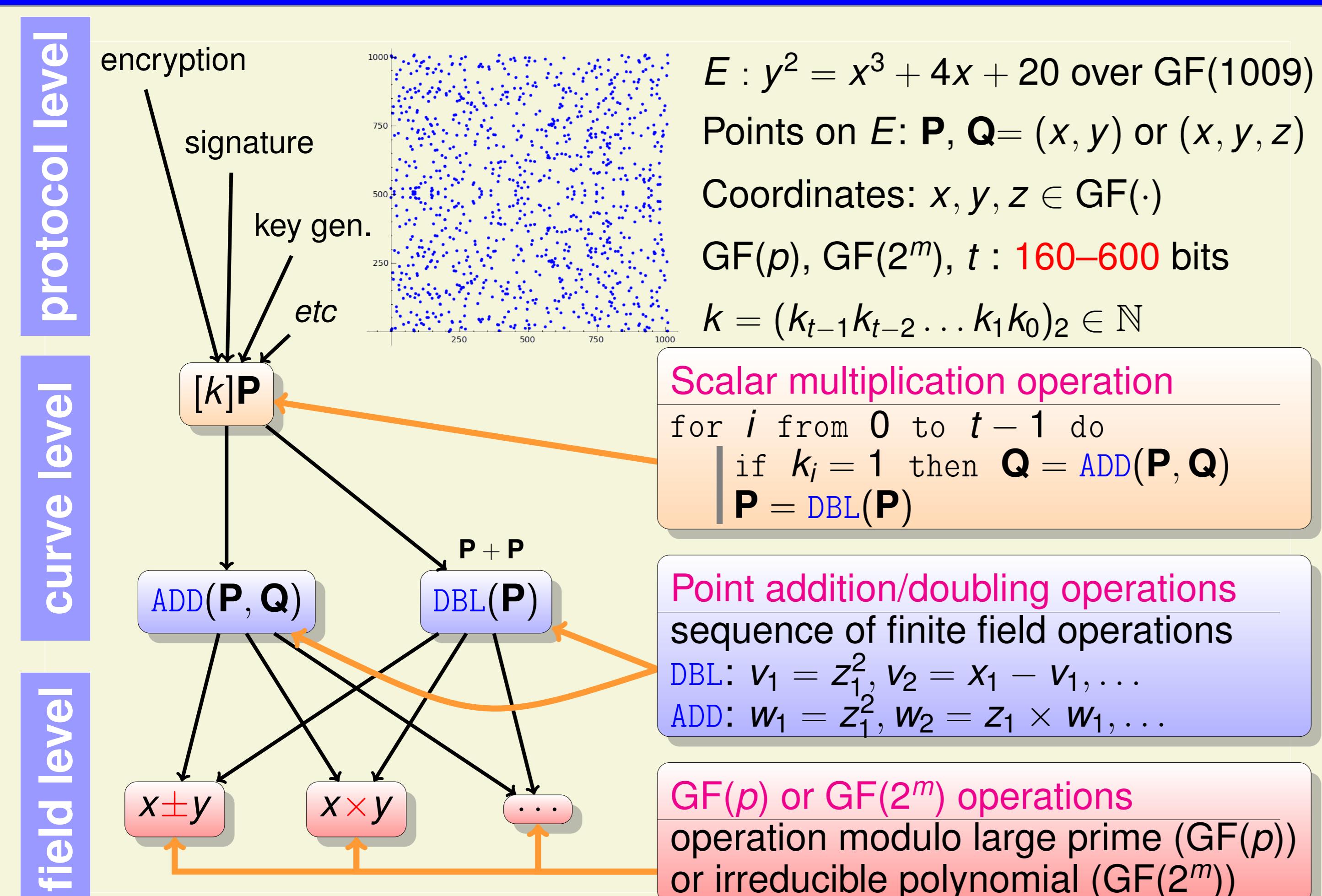
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Submitted on 29 Nov 2016

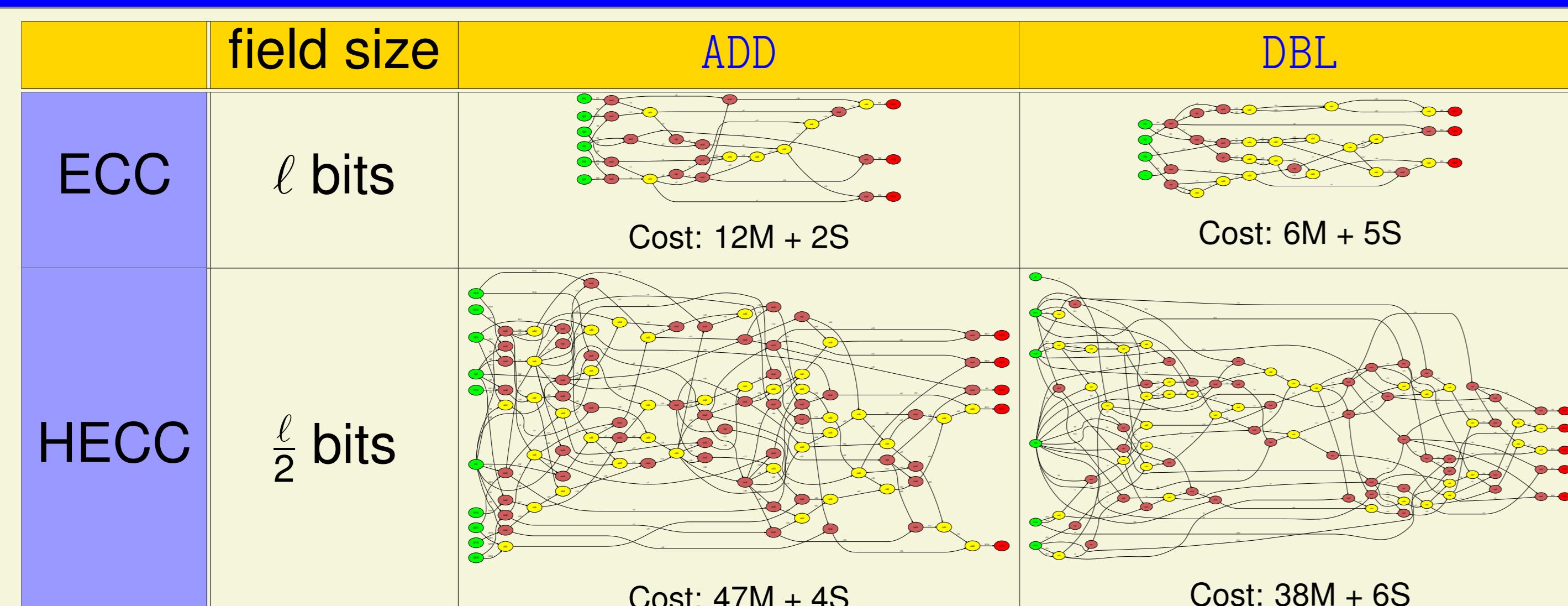
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1. Elliptic Curve Cryptography (ECC)

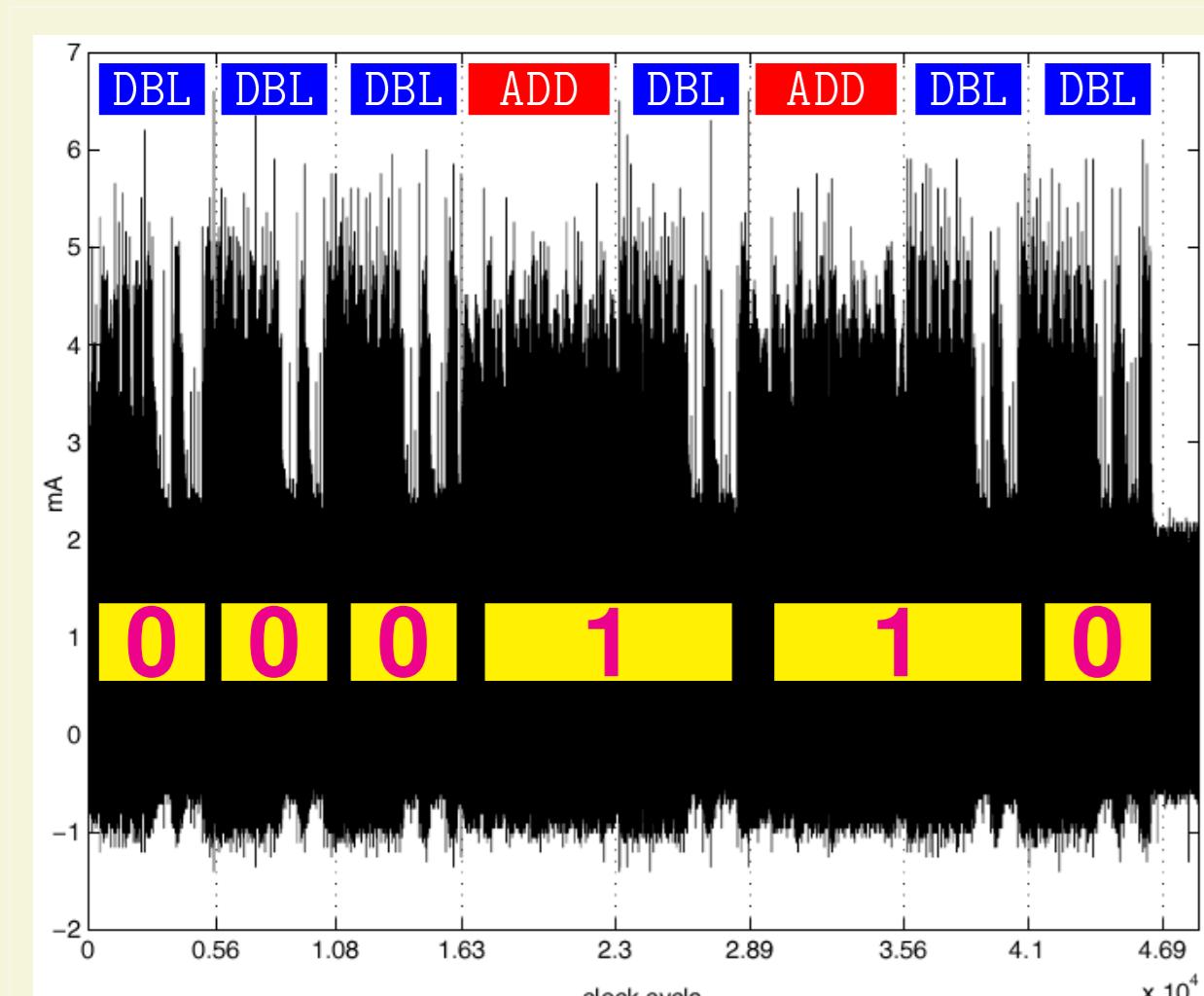


2. From ECC to HECC



Examples of computation expressions for projective coordinates

3. Side Channel Attacks (SCAs)



Side channels:

- Power consumption
- Electromagnetic radiation
- Computation timings

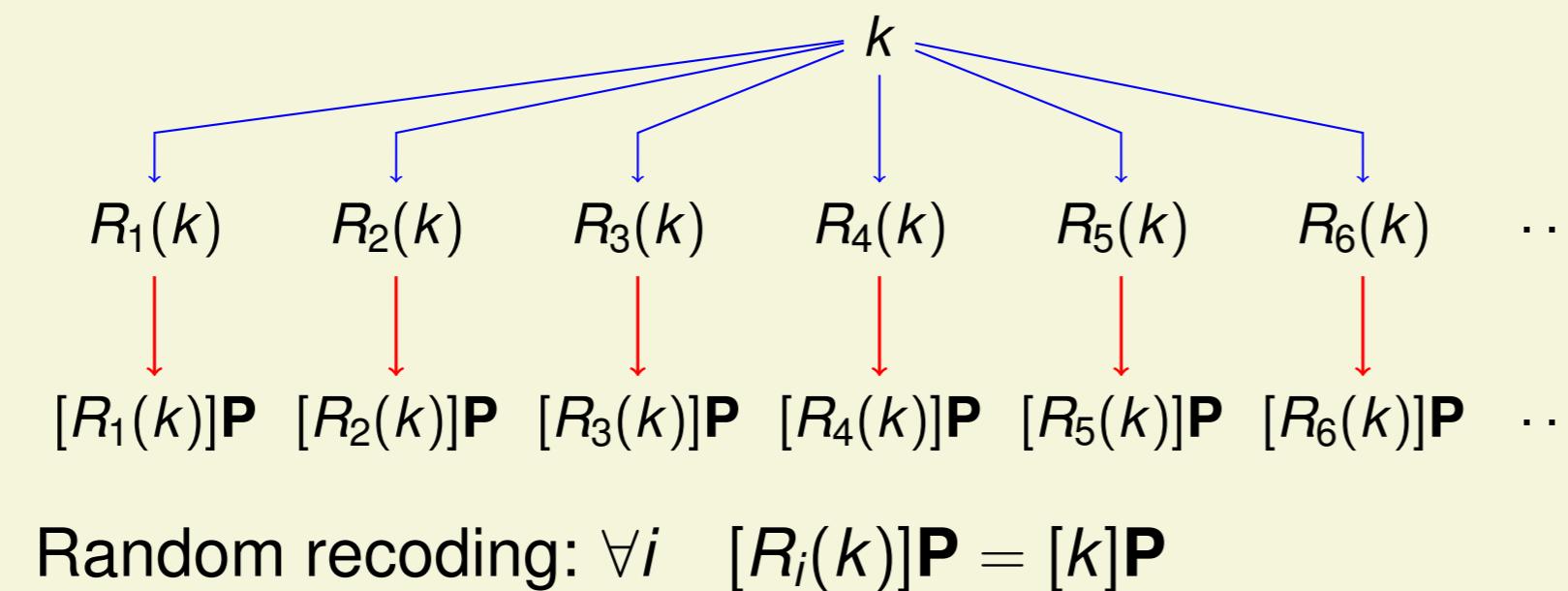
Attacks:

- Simple analysis
- Differential analysis (statistics)
- Templates and learning

4. Protections & Counter-Measures Against SCAs

- Uniform comp. durations
- Uniform power/EM profile
- Random behavior
- Circuit reconfiguration
- detection/correction codes
- Add noise (!)

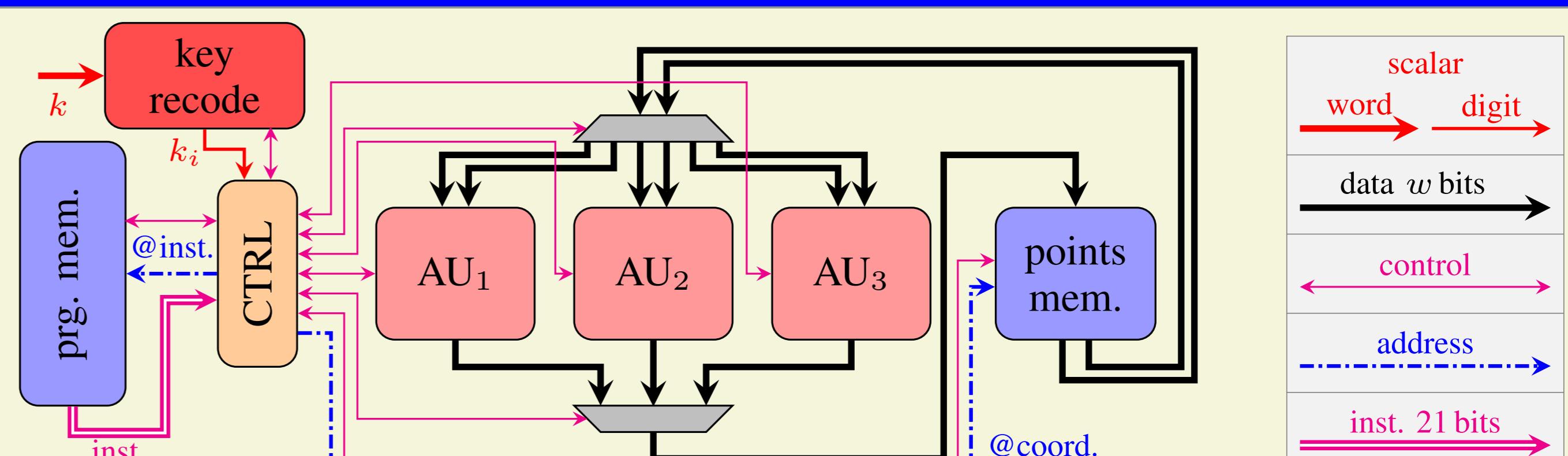
Example: use redundant number systems



5. HAH Project Objectives

- Efficient algorithms and representations for HECC
- HECC protections against SCAs (passive and active)
- Fast, low-power and secure hardware implementations (open source hardware code and programming tools)
- Intensive security evaluation using our SCA setup

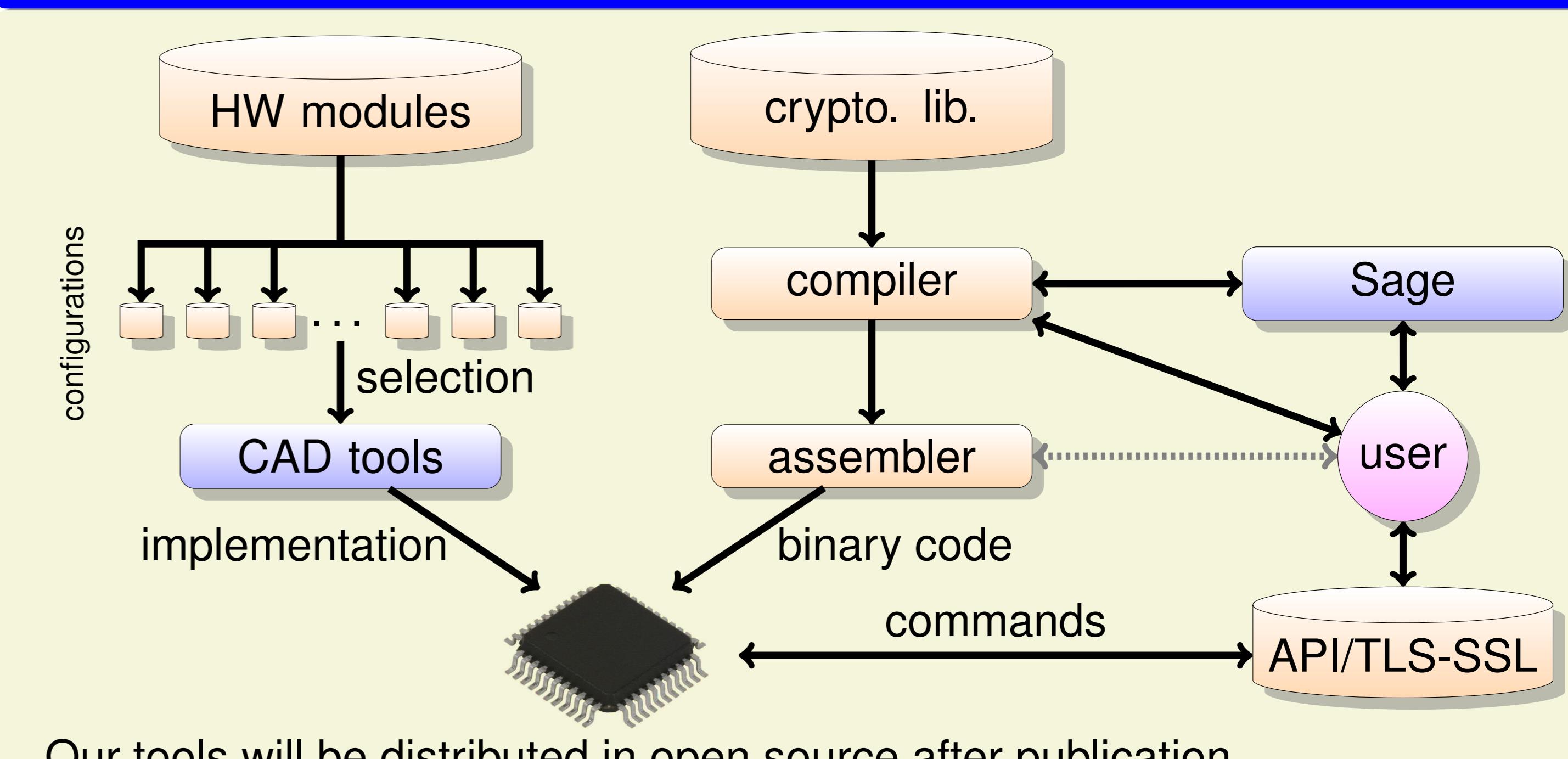
6. Developed Crypto-Processor(s)



- Arithmetic Units (AUs): \pm, \times, \div over $GF(p)/GF(2^m)$
- various configurations (area vs speed, internal protection)
- Various key recoding methods (and dedicated units)
- Configuration: field size, internal word size, #AUs, type(AUs)
- Circuit/architecture level protections

Remark: crypto-processor development started in PAVOIS ANR project

7. Programming Tools for Our Crypto-Processor(s)



8. Implementation Results on FPGA

XC6SLX75 FPGA, $GF(p)$, 256-bit ECC or 128-bit HECC, internal word size $w = 32$ bits

