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Formal Semantics of Behavior Specifications in the Architecture Analysis and Design Language Standard

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***Abstract*—In system design, an architecture specification or model serves, among other purposes, as a repository to share knowledge about the system being designed. Such a repository enables automatic generation of analytical models for different aspects relevant to system design (timing, reliability, security, etc.). The Architecture Analysis and Design Language (AADL) is a standard proposed by SAE to express architecture specifications and share knowledge between the different stakeholders about the system being designed. To support unambiguous reasoning, formal verification, high-fidelity simulation of architecture specifications in a model-based AADL design workflow, we have defined a formal semantics for the behavior specification of the AADL, the presentation of this semantics is the aim of this paper.**

I. Introduction

In system design, an architecture specification serves several important purposes. First, it breaks down a system model into manageable components to establish clear interfaces between them. In this way, complexity becomes manageable by hiding details that are not relevant at a given level of abstraction. Clear, formally defined, component interfaces allow us to avoid integration problems at the implementation phase. Connections between components, which specify how components affect each other, help propagate the effects of a change in one component to the linked components.

Second and most importantly, an architecture model is a repository to share knowledge about the system being designed. This knowledge can be represented as requirements, design artifacts, component implementations, held together by a structural backbone. Such a repository enables automatic generation of analytical models for different aspects relevant to system design, such as timing, reliability, security, performance, energy, etc. Since all the analyses are generated from the same source, the consistency of assumptions w.r.t. guarantees, of abstractions w.r.t. refinements, used for different analyses, becomes easier, and can be properly ensured in a design methodology based on formal verification and synthesis methods.

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Several standards for modeling embedded architectures have emerged in recent years: the SAE Architecture Analysis and Design Language (AADL)[1] [1], SysML[2], and UML MARTE [18]. Each of them represents different design approaches, materialises different concepts, serves different purposes. We focus on the AADL, and the scope and precision of concepts defined by this standard, to define a formal semantics for a significant subset of its behavioral specification annex language. Just as non-functional properties (timing, performance, energy, security properties), such descriptions can be attached to threads, processes, or any object of the standard (bus, sensor, actuator, port) to formally specify its behavior, as specified in the standard (e.g. a bus), or refine it (e.g. as an AFDX bus).

Since it began being discussed in the AADL committee, the formal semantics defined in this article evolved from a synchronous model of computation and communication [4] to a semantic framework for time and concurrency in the standard: asynchronous, synchronous or timed, to serve as a reference for model checking, code generation or simulation tools uses with the standard. This semantics is simple, relying on the structure of automata present in the standard already, yet provides tagged, trace semantics framework to establish formal relations between (synchronous, asynchronous, timed) usages or interpretations of behavior.

The remainder of this paper is organized as follows. Section II gives an overview of the Architecture Analysis and Design Language (AADL). Section III presents the *constrained automata*, that we use to specify the model of computation and communication of an AADL behavior specification. Section IV details the AADL behavior annex and its formalization using constrained automata. Section V discusses related work about formal specification of AADL models and finally Section VI concludes.

The extended version of this paper, [6], details

[1] http://www.aadl.info/
[2] http://www.omg.org/spec/SysML/1.4/

the implementation of the present model using the synchronous modeling environment Polychony on Polarsys[3] and applies it to the high-fidelity functional and real-time model of an adaptative cruise control system, Fig. 1.

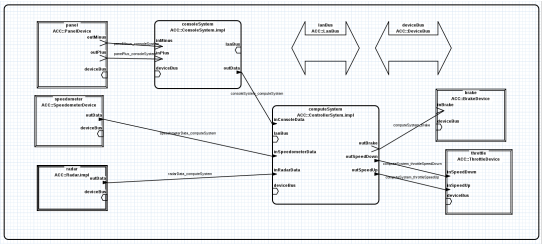

Figure 1. Overview of the Adaptive Cruise Control system modeled with AADL [6]. Double-lined rectangles represent devices, double-arrows buses and rectangles with rounded corners systems and subsystems.

II. The Architecture Analysis and Design Language

AADL [1] is a SAE International standard, dedicated to modeling embedded real-time system architectures. As an architecture description language, based on a component modeling approach, AADL describes the structure of systems as an assembly of software components allocated on execution platform components together with constraints and properties, including timing.

Architecture

In AADL, three distinct families of components are provided:

- software application components which include process, thread, thread group, subprogram, and data components,
- execution platform components that model the hardware part of a system including (possibly virtual) processor, memory, device, and (possibly virtual) bus components,
- composite components (systems).

The AADL components communicate via data, event, and event-data ports. Each component has a type, which represents the functional interface of the component and externally observable attributes. Each type may be associated with zero, one or more *implementation(s)* that describe the contents of the component, as well as the *connections* between components.

Properties

AADL properties provide various information about model elements of an AADL specification. For example, a property *Dispatch_Protocol* is used to provide the dispatch type of a thread. Property associations

[3]http://www.polarsys.org/projects/polarsys.pop

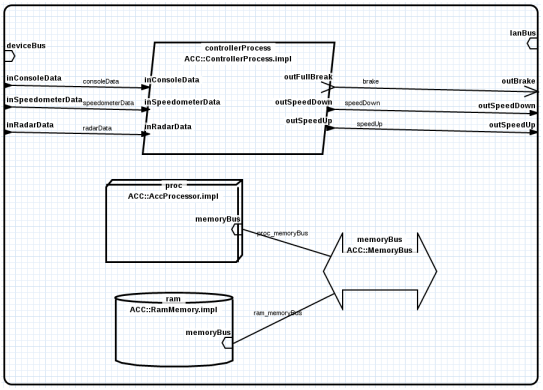

Figure 2. Control subsystem of the ACC system modeled with AADL specifying the main computational process and its associated ECU, bus and memory properties [6].

in component declarations assign a particular property value, e.g., *Periodic*, to a particular property, e.g., *Dispatch_Protocol*, for a particular component.

Timing execution model

Threads are dispatched depending on the thread type: periodically; by the arrival of data or events on ports; or from the arrival of a subprogram call (from another thread). Three event ports are predeclared: *dispatch*, *complete* and *error*.

A thread is activated to perform a computation at *start* time, and has to be finished before the *deadline*. The thread send a *complete* event at the end of its execution. The received inputs are frozen at a specified time (*Input_Time*), by default the *dispatch* time. This implies that the content of a dispatched port does not change between two consecutive *Input_Times*, even though the sender may send new values in its input FIFO. Such new values arriving after a given *Input_Time* will not be available through the port and thus will not be processed until the next *Input_Time*. As a result, the performed computation is not affected by a new input arrival until an explicit request for input (another *Input_Time*, such as the next dispatch time). Similarly, the output is made available to other components at a specified point of *Output_Time*, by default at *complete* (resp., *deadline*) time if the associated port connection is immediate (resp., delayed) communication.

III. Constrained Automata

We define the model of computation and communication of a behavior specification by the synchronous, timed or asynchronous traces of automata with variables [19]. These constrained automata are derived from *polychronous automata* defined within the polychronous model of computation and communication [13]. Automata define a behavior using transitions. A transition is composed of a source state,

a guard, an action, a target state. The guard and action of a transition are defined using logical formulas. The logical formula of the guard must be true for the transition to occur.

Vocabulary

These multi-sorted logical formulas are defined on the vocabulary W of AADL constants and of the states S, variables V, connections and ports P defined in the lexical scope of the denoted AADL object. An identifier w in W has a type $T = typeof(w)$ and is valuated on the corresponding domain $\mathbb{D}_T$, e.g., Booleans, integers or reals, $\mathbb{D} \supseteq \mathbb{B} \cup \mathbb{Z} \cup \mathbb{R}$. We write $\mathbb{D}_x$ for the value domain of a typed identifier x. The domain of a port identifier p of type T is defined by $\mathbb{D}_p = \mathbb{D}_T^{\perp} = \mathbb{D}_T \cup \{\perp\}$. The bottom sign $\perp$ denotes the absence of a value at the given step of execution. A port value is said absent if the port is not frozen and its value is neither read or written.

Formulas

The set of typed formulas F_W on the vocabulary W is an algebraic set of terms that denotes the conditions, actions and constraints of an AADL object of vocabulary W. It is defined by induction from:

- Constants 0 ($false$), to mean "never", and 1 ($true$), to mean "always". Always is discrete, relative to the vocabulary W.
- Atoms w of W, to mean the value of an identifier w.
- Unitary expressions:
  - $\hat{}p$ is the clock of p: a Boolean that denotes the presence of a value on a frozen port p, i.e., $p \neq \perp$;
  - $@p$ is the date of p: a real number that denotes the time of an event present on a port p;
  - v' denotes the next value of a variable v;
  - $\neg f$ denotes the complement of formula f, for all f in F_W.
- Binary expressions $f\ op\ g$:
  - for all Boolean formula f, g in F_W and Boolean operators $\vee$, $\wedge$, $\Rightarrow$, etc. (in particular, $f - g = f \wedge \neg g$);
  - for all numerical formula f, g in F_W and numerical operators $+$, $-$, $*$, $/$, $\%$, $=$, $<$, etc.

A formula f is the denotation of a well-typed AADL condition or action. It is hence assumed to be a well-typed, multi-sorted, logical expression. Ill-typed expressions do not define formula.

Model

A model m is a function $W \rightarrow \mathbb{D}_W$ from a vocabulary W to its domain of valuation $\mathbb{D}_W$ that is true for a formula f of F_W, written $m \models f$. A timed model $m^{@}$ is a function $W \rightarrow \mathbb{R} \times \mathbb{D}_W$ associating also each event with a date, that the formula must satisfy as well.

Automaton

The meaning of a behavior annex is defined by an incomplete automaton with variables $A = (S_A, s_0, V_A, P_A, T_A, C_A)$ defined by:

- S_A, the set of states of the automaton A, s_0 is the initial state.
- V_A, the set of local variables of the automaton A (${V_A}'$ designates the set of next values v' for all $v \in V_A$).
- P_A, the set of ports of the automaton A, both inputs I_A and outputs O_A, $P_A = I_A \cup O_A$.
- F_A is the set of Boolean formulas of A, defined on the vocabulary $W_A = S_A \cup V_A \cup P_A$.
- The transition function $T_A \in S_A \times F_A \rightarrow F_A \times S_A$ defines the transition system of A.
  - The source formula of a transition is its guard g, defined on V_A and I_A.
  - The target formula of a transition is its action f, defined from V_A and P_A.
- $C_A \in F_A$ is the constraint of A. It must always equal 0. It is a formula that denotes the invariants (properties, requirements) of the denoted AADL object in a form of a logical formula.

Since variables V are private to the automaton, a transition function T_A is equivalent to one in $X_A = Q_A \times F_P \rightarrow F_P \times Q_A$ over extended states $Q_A = S_A \times \mathbb{D}^{V_A}$ for all valuations $\mathbb{D}^{V_A} = \prod_{v \in V_A} \mathbb{D}_v$ of the variables V_A: for all transition $(s, g, f, d) \in T_A$, for all model $m \in (V_A + {V_A}') \rightarrow \mathbb{D}^{V_A}$, we have $((s, m(V_A)), m(g), m(f), (d, m({V_A}')) \in X_A$ and, for all $v' \in {V_A}'$ undefined in f, $m(v') = m(v)$.

The role of a constraint formula such as $\hat{}a \wedge \hat{}b = 0$ is to guarantee a property by all models of the incomplete automaton.

Properties

- The control clock 1_A of an automaton A is defined by the sum (union) of its port clocks $1_A = \sum_{p \in P_A} \hat{}p$.
- The trigger $tick_A(s) = \sum_{(s,g,f,d) \in T_A}(g)$ of a state s is defined by the upper bound of guard formulas g from s.
- The stuttering clock of a state s is defined by $\tau_A(s) = 1_A - ((s * C_A) + tick_A(s))$. It means that an automaton A is silent in state s if and only if its model m satisfies the constraint C_A in state s and no guard can be triggered from s with m.

Product

The synchronous product of two automata $A = (S_A, s_0, V_A, P_A, T_A, C_A)$ and $B = (S_B, t_0, V_B, P_B, T_B, C_B)$ is defined by

$A \mid B = (S_{AB}, (s_0, t_0), V_{AB}, P_{AB}, T_{AB}, C_{AB})$ with $S_{AB} = S_A \times S_B$, $V_{AB} = V_A \cup V_B$, $P_{AB} = P_A \cup P_B$, $C_{AB} = C_A \vee C_B$, $T_{AB} = \{((s_1, t_1), g_1 \wedge g_2, f_1 \wedge f_2, (s_2, t_2)) \mid (s_1, g_1, f_1, t_1) \in T_A \wedge (s_2, g_2, f_2, t_2) \in T_B\}$.

Product is commutative, associative, has neutral element $(\{s\}, s, \emptyset, \emptyset, \emptyset, 0)$ and is idempotent for deterministic automata.

Small step

The model m of a transition in an automaton A consists of a pre-condition $\text{pre}(m)$ defined on input ports $I \to \mathbb{D}_I^\perp$ and state variables $V \to \mathbb{D}_V$ and a post condition $\text{post}(m)$ defined on output ports $O \to \mathbb{D}_O^\perp$ and next values of variables $V' \to \mathbb{D}_V$.

A *small step* of an automaton A from state s to state t is defined by a model m of A that satisfies its constraint C_A, written $m \models \neg C_A$, and both the guard g and action f of a transition (s, g, f, t) of A, written $m \models g \wedge f$.

Big step

Let $n > 1$, $q_1 = (s_1, r_1)$ and $q_n = (s_n, r_n)$ two extended states of an automaton A with complete states $s_1, s_n \in S_A$ and variable valuations $r_1, r_n \in \mathbb{D}^{V_A} \simeq V_A \to \mathbb{D}_{V_A}$ (note that it may be the case that $q_n = q_1$). A *big step* of automaton A from s_1 to s_n is defined by a model $m \in P_A \to \mathbb{D}_{P_A}^\perp$ that, for all $1 \leq i < n$ satisfies:

- $\text{pre}\, r_{i+1}(v) = \text{post}\, r_i(v')$ for all $v \in V_A$
- $m_i = r_i \uplus m$
- $m_i \models \neg C_A$
- $(s_i, g_i, f_i, s_{i+1}) \in T_A$ and $m_i \models g_i \wedge f_i$
- $\text{pre}\, r_i(v) = \text{post}\, r_i(v')$ for all $v' \in V'_A$ not occurring in f_i and g_i
- s_i is an *execution state* if $1 < i < n$ (an *execution state* is a non observable, internal state—see Section IV).

We write $m, s_1 \models A, s_n$ to mean that m is the model of a big step of A from s_1 to s_n.

Synchronous and asynchronous trace

A *synchronous trace* $B \in P_A \to (\mathbb{D}_{P_A}^\perp)^*$ of an automaton A is a finite sequence of valuation over P_A obtained by concatenating the codomains of successive (big) steps. The length of B is denoted $|B|$. The set of synchronous traces of an automaton A from its initial state s_0 is defined as:

$$T(A, s_0) = \{B \in P_A \to (\mathbb{D}_{P_A}^\perp)^* \mid 0 \leq i < |B|, \\ m_i, s_i \models A, s_{i+1} \wedge \forall x \in dom(B), (B(x))_i = m_i(x)\}$$

An *asynchronous trace* $B^\# \in P_A \to (\mathbb{D}_{P_A})^*$ is the abstraction of a synchronous trace $B \in P_A \to (\mathbb{D}_{P_A}^\perp)^*$ obtained by the removal of all absence marks $\perp$. For a sequence s in $(\mathbb{D}^\perp)^*$, we denote by $s_{/\perp}$ the projection of s on $\mathbb{D}^*$. The set of asynchronous traces of an automaton A from its initial state s_0 is defined as:

$$T^\#(A, s_0) = \{B \in P_A \to (\mathbb{D}_{P_A})^* \mid \\ C \in T(A, s_0) \wedge \forall x \in dom(B), B(x) = C(x)_{/\perp}\}$$

Timed step and timed trace

A *timed step* of an automaton A from state s to state t is defined by a timed model $m^@$ defined on W_A that satisfies its constraint and the guard g and action f of a transition (s, g, f, t) of A. For all w in W_A, $m^@(w)$ refers to the value of w in $m^@$ and $m^@(@w)$ refers to the date of w in m.

A *timed trace* $B^@ \in P_A \to (\mathbb{R} \times \mathbb{D}_{P_A}^\perp)^*$ of an automaton A is the concatenation of the codomains of successive timed steps $(m_i^@)_{i \geq 0}$ of A such that for all $0 \leq i < j$, for all x in $dom(m_i^@)$, for all y in $dom(m_j^@)$, $m_i^@(@x) < m_j^@(@y)$. A timed trace $B^@$ is therefore the refinement of a synchronous trace $B \in P_A \to (\mathbb{D}_{P_A}^\perp)^*$ associating each event in B with a date.

IV. Behavior Annex Model

The behavior annex provides an extension to AADL to associate functional behavior specifications with AADL components. A behavior is expressed by transition systems with conditions and actions [2]. They can be refined to simulate and define the functional behavior of the AADL component using an imperative action language.

This section first presents how to formally express the meaning of a behavior annex using an automaton. Then, the constituents of the behavior annex are defined (transition system, action and expression language, etc.) and their formal semantics given.

A. Formalization using the constrained automata

The meaning of a behavior annex is defined by the axiomatic, denotational and operational interpretation of constrained, incomplete, automata with variables $A = (S_A, s_0, V_A, P_A, T_A, C_A)$ such as defined in Section III. The sets S_A, V_A, P_A represent the states (including the *initial state* s_0), variables and ports of A. The guard, action and constraints of its transitions T_A and constraints C_A are denoted by multi-sorted logical formula F_A.

F_A is defined over the vocabulary W_A available in the scope of a behavior annex: AADL value constants, port, state, and variable names. They are combined using AADL logical operators and numeric operators. Operators that are specific to the model of computation and communication of a given behavior annex are $\hat{}p$, a Boolean value to mean the presence of a value on port p under synchronous interpretation (i.e., $p \neq \perp$); and $@p$, a numeric value to mean the time of an event on p, under timed interpretation.

The transition system of an automaton A is defined by the function $T_A \in S_A \times F_A \to F_A \times S_A$ whose

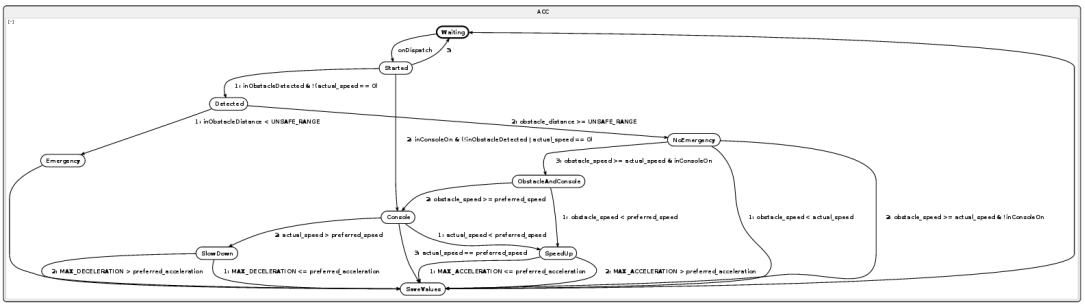

Figure 3. Overview of the ACC transition system with operation states, behavior conditions and variables [6]

quadruples (s, g, a, t) define the source state s, guard formula g, action formula a and target state t of a specified transition.

B. Automaton

The AADL behavior annex defines an extended automaton BA described by three sections: variables declarations, states declarations, and transitions declarations. This automaton BA of the behavior annex is not to be confused with the automaton A interpreted to give its meaning to a behavior annex. On the one hand, we have BA, an automaton which is part of the behavior annex, and on the other hand A, an automaton which is used to express the meaning of the whole behavior annex.

As shown in Figure 4, the automaton BA of a `behavior_annex` instance is defined on the vocabulary consisting of its private variables `behavior_variable`, of its states `behavior_state`, and ports of its parent component. Its transition system T_{BA} is the union of the transitions specified by a `behavior_transition`.

```
behavior_annex ::=
     [ variables { behavior_variable }+ ]
     [ states { behavior_state }+ ]
     [ transitions { behavior_transition }+ ]
```

Figure 4. Constituents of the behavior annex syntax for the transition system.

1) Variables section: The variables section of the transition system of a behavior annex declares identifiers that represent variables with the scope of the behavior annex subclause. Local variables can be used to keep track of intermediate results within the scope of the annex subclause. They may hold the values of out parameters on subprogram calls to be made available as parameter values to other calls, as output through enclosing out parameters and ports, or as value to be written to a data component in the AADL specification. They can also be used to hold input from incoming port queues or values read from data components in the AADL specification. They are not persistent across the various invocations of the same behavior annex subclause.

2) States section: The states section declares all the states of the automaton. Some states may be qualified as `initial` state (thread halted), `final` state (thread stopped), or `complete` state (thread awaiting for dispatch), or combinations thereof. A state without qualification is referred to as `execution` state. A behavior automaton starts from an initial state and terminates in a final state. A complete state acts as a suspend/resume state out of which threads and devices are dispatched. Complete states thus correspond (with initial and final states) to the observable states of the behavior, in which computations are "paused", inputs read and outputs produced.

```
behavior_transition ::=
  [ transition_identifier
    [ [ behavior_transition_priority ] ] : ]
      source_state_identifier
        { , source_state_identifier }*
          -[ behavior_condition ]->
            destination_state_identifier
              [ behavior_action_block ] ;
```

Figure 5. Elements of the behavior annex syntax for transitions.

3) Transitions section: The transitions section defines transitions from a source state to a destination state. Transitions in a behavior automaton represent an execution sequence within a thread. A transition out of a complete state is initiated by a dispatch once its condition is satisfied. Transitions can be guarded by dispatch or execute conditions, and can have actions. Figure 5 presents the syntax used in the behavior annex for transitions.

Dispatch conditions explicitly specify dispatch trigger conditions out of a complete state. A dispatch condition is a Boolean expression that specifies the logical combination of triggering events: arrival of an event or event data on an event port or an event data port, receipt of a call on a provided subprogram access, or timeout event.

Execute conditions specify transition conditions out of an execution state to another state. They effectively select between multiple transitions out of a given

state to different states. These conditions are logical expressions based on component inputs, subcomponent outputs, and values of data components, state variable values, and property constants. They can also result in catching a previously raised execution timeout exception.

If transitions have been assigned a priority number, then the priority determines the transition to be taken. The higher the priority number is, the higher the priority of the transition is. If more than one transition out of a state evaluates its condition to true and no priority is specified, then one transition is chosen non-deterministically. For multiple transitions with the same priority value the selection is also non-deterministic. Transitions with unspecified priority have the lowest one.

Each transition can have actions. Actions can be subprogram calls, retrieval of input and sending of output, assignments to variables, read/write to data components, and time consuming activities. An action is related to the transition and not to the states: if a transition is taken, the sequence of actions is performed and then the state specified as the destination of the transition becomes the new current state.

4) Transition semantics: States of a behavior annex transition system can be either observable from the outside (`initial`, `final` or `complete` states), that is states in which the execution of the component is paused or stopped and its outputs are available; or non observable execution states, that is internal states. We thus define two kinds of steps in the transition system BA: *small steps*, that is non-observable steps from or to an internal state; and *big steps*, that is observable steps from a *complete* state to another, through a number of small steps (see Section III).

The semantics of the AADL considers the observable states of the automaton. The set S_A of automaton A (used to interpret the behavior annex) thus only contains states corresponding to these observable states and set T_A big-step transitions from an observable state to another (by opposition with small-step transitions from or to an execution state).

A transition `behavior_transition` has source state $s =$ `source_state_identifier`. Its guard formula g is defined by the translation of the expression `behavior_condition` as a logical formula. Its target state $d =$ `destination_state_identifier` is that of the transition system defined by the semantic function $T(s, d)$ (defined Section IV-D) applied to its action block `behavior_action_block`.

A `transition_identifier`, if present, is represented by a label L that names the clock of the transition. It is a (virtual) event considered present and true iff the guard formula of that transition holds and the constraint of the automaton is enforced: the transition $(L : s, g, f, d)$ is equivalent to the transition (s, g, f, d) with the constraint $L \Leftrightarrow (s \wedge g)$.

A `behavior_transition_priority`, if present, enforces a deterministic logical order of evaluation among transitions. A pair of transitions $(s[m], g1, f1, s1)$ and $(s[n], g2, f2, s2)$ from a state s and such that $m > n$ (to mean that m has higher priority than n) is equivalent to the transitions $(s, g1, f1, s1)$ and $(s, g2 \wedge \neg g1, f2, s2)$: the guard formula of a prioritized transition is subtracted to all transition in the same state of lower or no priority.

C. Behavior Conditions

Behavior conditions that cause transitions may be either execute conditions or dispatch conditions (see Figure 6 for the syntax).

Execute conditions are Boolean-valued expressions, and may only be used in transitions leaving an execution (or initial) state. State machines may never 'stall' in execution states; there must always be an enabled, outgoing transition from an execution state. The `otherwise` condition occurs when no other execute condition off an execution state is true.

Dispatch conditions can only be associated with transitions from a `complete` state. A thread scheduler evaluates dispatch conditions to determine when threads are dispatched. A dispatch trigger condition can be the arrival of events or event data on ports (expressed as a disjunction of conjunctions) or timeout.

Periodic dispatches are always considered to be implicit unconditional dispatch triggers on complete states and handled by dispatch conditions without dispatch trigger condition.

Dispatch can also be triggered by event arrival at the predeclared `Stop` port. Timeout catch is a dispatch trigger condition that is raised after the specified amount of time since the last dispatch or the last completion is expired.

Semantics: A `dispatch_condition` is represented by a guarding formula g that is formed by referring to the clock $\hat{p}$ of the logical combination of ports specified as its `dispatch_trigger_condition`. An `execute_condition` is represented by a guarding formula that encodes its `logical_value_expression` using the current state of its persistent variables V. The `otherwise` clause is handled as the guard of least priority. It is hence defined by $(\hat{}s - tick_A(s))$, which differs from the stuttering clock of $s, \tau_A(s)$.

In the case of a time-triggered dispatch, when the dispatch trigger condition of an `on dispatch` clause is empty, the Boolean true is assumed, but only in the scope of the denoted object. It means that the dispatch condition is considered to be present as soon as time-

```
behavior_condition          ::=  execute_condition
                               |  dispatch_condition
execute_condition           ::= logical_value_expression
                               |  otherwise
dispatch_condition          ::= on dispatch   [ dispatch_trigger_condition ] [ frozen ( frozen_ports ) ]

dispatch_trigger_condition  ::= dispatch_trigger_expression | stop | timeout_catch
dispatch_trigger_expression ::=  dispatch_conjunction { or dispatch_conjunction }*
dispatch_conjunction        ::= port_identifier { and port_identifier }*
timeout_catch               ::= timeout  [ [ ( port_identifier { or port_identifier }*  ) ] behavior_time ]

behavior_action_block       ::=  { behavior_actions } [ timeout behavior_time ]
behavior_actions            ::= behavior_action | behavior_action_sequence | behavior_action_set
behavior_action_sequence    ::=   behavior_action { ; behavior_action }+
behavior_action_set         ::=   behavior_action { & behavior_action }+

behavior_action             ::=  basic_action
                               |  behavior_action_block
                               |  if ( logical_value_expression ) behavior_actions
                               {  elsif ( logical_value_expression ) behavior_actions }*
                               [  else behavior_actions ]   end if
                               |  for ( element_identifier in element_values ) { behavior_actions }
                               |  forall ( element_identifier in element_values ) { behavior_actions }
                               |  while ( logical_value_expression ) { behavior_actions }
                               |  do behavior_actions until ( logical_value_expression )

basic_action                ::=   assignment_action
                               |  communication_action
                               |  timed_action
```

Figure 6. Elements of the behavior annex syntax for conditions, actions and expressions

triggered and an event is to be handled (otherwise, it can be regarded as silent, i.e., absent).

A `timeout` clause, if present, is denoted by the dispatch of the virtual event port `timeout`, whose trigger is associated with a real time constraint of the parent component behavior action block. It can be associated with a port list to reset timer from before timing out by arrival of an event at listed port. The parent component is responsible for triggering this event by respecting the real time constraint behavior time, if specified, as well as with the specified frozen ports list, if present.

D. Action language

The action language of the behavior annex defines actions performed during transitions. Actions associated with transitions are action blocks that are built from basic actions and a minimal set of control structures: sequences, sets, conditionals and loops (see Figure 6 for the syntax). Action sequences are executed in order, while actions in actions sets can be executed in any order.

Basic actions can be assignment actions, communication actions or time consuming actions. Assignments consist of a value expression and a target reference (local variables, data components acting as persistent state variables, or outgoing features such as ports and parameters) for the value assignment, separated by the assignment symbol "`:=`".

Communication actions can be freezing the content of incoming ports, initiating a send on an event, data, or event data port, initiating a subprogram call or catching a previously raised execution timeout exception.

Time consuming actions, or timed actions, can be predefined computation actions. Computation actions specify computation time intervals. An execution timeout exception can be raised after any behavior action block. Raising such a timeout event may trigger a transition with a timeout catch execute condition.

Semantics: Let us recall that the transition system T representing a behavior transition is defined by $T = (s, g, true, s') \bigcup T'$. It has source state s and a guard formula g. Its target state d is that of the transition system T' defined by the semantic function call encoding the $behavior\_action\_block$ block as $\mathcal{T}(s', d)[behavior\_action\_block] = T'$. T' is constructed by recursively calling function $\mathcal{T}$ on the action block's sub-expressions.

The recursive function $\mathcal{T}(s, d)[behavior\_actions] = T$ associates the action block $behavior\_actions$ guarded by a behavior condition of formula g, of source and target states s and d, to a transition system T. It is defined by case analysis on $behavior\_actions$:

- a behavior action sequence is represented by concatenating the transition systems of its elements. For instance, $\mathcal{T}(s, d)[action_1 \ ; \ action_2]$ is translated by the union $T_1 \bigcup T_2$ of its transition systems $T_1 = \mathcal{T}(s, e)[action_1]$ and $T_2 = \mathcal{T}(e, d)[action_2]$, by introducing a new execution state e;
- a behavior action set is represented by composing the transition systems of its elements. For instance, $\mathcal{T}(s, d)[action_1 \ \& \ action_2]$ is translated

by the synchronous composition

$$T = (T_1|T_2)[(s_1, s_2)/s, (d_1, d_2)/d]$$

of its transition systems $T1 = \mathcal{T}(s_1, d_1)[action_1]$ and $T2 = \mathcal{T}(s_2, d_2)[action_2]$, substituting the composed states (s_1, s_2) and (d_1, d_2) by s and d.

A behavior action is translated by case analysis of its form:

- **if** (b) a_1 **else** a_2 **end if** is translated by a guard formula g corresponding to $logical\_expression$ and returning the union

  $$T = T_1 \bigcup T_2 \bigcup \{(s, g, true, s_1), (s, \neg g, true, s_2)\}$$

  of its transition systems $T_1 = \mathcal{T}(s_1, d)[a_1]$ and $T_2 = \mathcal{T}(s_2, d)[a_2]$ where the guard formula g is the translation of the logical value expression, b;
- **while** (b) { a } is translated by the union $T_1 \bigcup T_2$ of its transition systems $T_1 = \mathcal{T}(s_1, s_2)[a]$ and $T_2 = \{(s, h, true, s_1), (s, \neg h, true, d), (s_2, h, true, s_1), (s_2, \neg h, true, d)\}$ where the guard formula h is the translation of the logical value expression, b;
- **do** a **until** (b) is translated by the union $T_1 \bigcup T_2$ of its transition systems $T_1 = [a]$ and $T_2 = (s_1, h, true, s), (s_1, \neg h, true, d)$ where the guard formula h is the translation of the logical value expression, b;
- **forall** $(j$ **in** $e)$ { a } can be translated by the action set $a_1 \& \ldots \& a_n$ where a_i results from the substitution of j by the i^{th} element value of e in a.
- **for** $(j$ **in** $e)$ { a } can be translated by the action sequence $a_1; \ldots; a_n$ where a_i results from the substitution of j by the i^{th} element value of e in a.

A basic action is translated by case analysis of its grammar's sub-clauses:

- an assignment action to a variable v:=e is represented by updating v with e as $\mathcal{T}(s, d)[v := e] = \{(s, true, v' = e, d)\}$ where v' represents the next value of v;
- an output port action $port!(value)$ is represented by an action formula that binds $value$ to $port$ by $\mathcal{T}(s, d)[port!value] = \{(s, true, port = value, d)\}$;
- an input port action $port?(target)$ is represented by an action formula that updates $target$ to $port$ by $\mathcal{T}[port?target] = \{(s, true, target' = port, d)\}$;
- a timed action of the form **computation** $(t_1[..t_2])$ is a timing constraint imposed on the execution time of the action block. It can either be represented by a timing property of the parent thread object or simulated by a protocol interacting with the scheduler using two virtual ports ps (start) and pf (finish) to specify a delay of time between exclusive occurrences of ps and pf, and to translate the timing specification by $\mathcal{T}(s, d)(t_1[..t_2])] = \{(s, true, ps, c), (c, pf, true, d)\}$ using a complete state c and the timed constraint $@ps + t_1 \leq @pf + t_2$.

E. Expression language

The expression language is used to define expressions, the results of which are used either as logical conditions of transitions or conditional statements, or as values for assignment actions. Expressions consist of logical expressions, relational expressions, and arithmetic expressions. Values of expressions can be variables, constants or the result of another expression. Variable expression values are evaluated from incoming ports and parameters, local variables, referenced data subcomponents, as well as port count, port fresh, and port dequeue. Constant expression values are Boolean, numeric or string literals, property constants or property values.

V. Related work

Many related works have contributed to the formal specification, analysis and verification of AADL models and its annexes, hence implicitly or explicitly proposing a formal semantics of the AADL in the model of computation and communication of the verification framework considered.

The analysis language REAL [10] allows to define structural properties on AADL models that are checked inductively visiting the object of a model under verification. [9] presents an extension of this language called LUTE which further uses PSL (Property Specification Language) to check behavioral properties of models as well as a contract framework called AGREE for assume-guarantee reasoning between composed AADL model elements.

The COMPASS project has also proposed a framework for formal verification and validation of AADL models and its error annex [8]. It puts the emphasis on capturing multiple aspects of nominal and faulty, timed and hybrid behaviors of models. Formal verification is supported by the nuSMV tool. Similarly, the FIACRE framework [3] uses executable specifications and the TINA model checker to check structural and behavioral properties of AADL models.

RAMSES, on the other hand [7], presents the implementation of the AADL behavior annex. Its implementation OSATE proceeds by model refinement and can be plugged in with Eclipse-compliant backend tools for analysis or verification. For instance, the RAMSES tools uses OSATE to generate C code for OSs complying the ARINC-653 standard.

Synchronous modeling is central in [17], which presents a formal real-time rewriting logic semantics for a behavioral subset of the AADL. This semantics can be directly executed in Real-Time Maude and provides a synchronous AADL simulator (as well as LTL model-checking). It is implemented by the tool AADL2MAUDE using OSATE.

Similarly, Yang et al. [20] define a formal semantics for an implicitly synchronous subset of the AADL, which includes periodic threads and data port communications. Its operational semantics is formalised as a timed transition system. This framework is used to prove semantics preservation through model transformations from AADL models to the target verification formalism of timed abstract state machine (TASM).

Our proposal carries along the same goal and fundamental framework of the related work: to annex the core AADL with formal semantic frameworks to express executable behaviors and temporal properties, by taking advantage of model reduction possibilities offered thanks to a synchronous hypothesis, of close correspondence with the actual semantics of the AADL.

Yet, we endeavour in an effort of structuring and using them together within the framework of a more expressive multi-rate or multi-clocked, synchronous, model of computation and communication: that of polychrony. Polychrony would allow us to gain abstraction from the direct specification of executable, synchronous, specification in the AADL, yet offer services to automate the synthesis of such, locally synchronous, executable specification, together with global asynchrony, when or where ever needed.

CCSL, the clock constraint specification language of the UML profile MARTE [16], relates very much to the effort carried out in the present document. CCSL is an annotation framework to making explicit timing annotation to MARTE objects in an effort to disambiguate its semantic and possible variations.

CCSL actually provides a clock calculus of greater expressivity than polychrony, allowing for the expression of unbounded, asynchronous, causal properties between clocks (e.g. inf and sup).

While CCSL essentially is isolated as an annex of the MARTE standard for specifying annotations, our approach is instead to build upon the semantics of the existing behavior annex and specify it within a polychronous model of computation and communication.

Finally, the Behavior Language for Embedded Systems with Software (BLESS) [11], [12] was derived from the behavior annex by adding non-executable assertions to behavior to become a proof outline. With human guidance, a proof engine transforms proof outlines into deductive proofs that every execution conforms to a formal behavior specification. Although the formal semantics defined for BLESS are expressed much differently than the semantics for behavior annex defined here, they are not incompatible. We are endeavoring to merge the semantics so that deductively proved BLESS behaviors can also be analyzed with polychronous tools such as Polychrony.

Our previous work demonstrated that all concepts and artefacts of the AADL could, as specified in its normative documents, be given a formal specification in the polychronous model of computation and communication [15], [23], [14], [21], [22], [5], implemented by mean of its import and simulation in the Eclipse project POP's toolset available from the Polarsys Industry Working Group[4].

VI. Conclusion

In this paper, we propose a formal semantics for a significant subset of the behavioral specification annex of the Architecture Analysis and Design Language (AADL). This annex allows one to attach a behavior specification to any components of a system modeled using the AADL, and can be then analyzed for different purposes which could be, for example, the verification of logical, timing or scheduling requirements.

The addressed subset includes the transition system (state variables, states and transitions), the conditions that can be attached to transitions, the action language allowing to describe actions to be computed when a transition is fired and the expression language, used for logical conditions and assignment actions.

The semantics we presented for this subset relies on constrained automata (automata with variables derived from polychronous automata) and supports unambiguous reasoning, formal verification and simulation of the modeled system.

In future work, we will provide semantics for the remaining subset of the behavior specification annex of the AADL (mainly the synchronization protocols allowing to send and receive execution request in a client-server configuration). We will also implement the semantics of the behavior specification annex through a model transformation from the annex to the Signal language, in which the constrained automata are already implemented.

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