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TCAD Simulation of Amorphous Indium-Gallium-Zinc Oxide Thin-Film Transistors

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Abstract. Indium-gallium-zinc oxide (IGZO) thin-film transistors (TFTs) are simulated using TCAD software. Nonlinearities observed in fabricated devices are obtained through simulation and corresponding physical characteristics are further investigated. For small channel length (below 1 μm) TFTs' simulations show short channel effects, namely drain-induced barrier lowering (DIBL), and effectively source-channel barrier is shown to decrease with drain bias. Simulations with increasing shallow donor-like states result in transfer characteristics presenting hump-like behavior as typically observed after gate bias stress. Additionally, dual-gate architecture is simulated, exhibiting threshold voltage modulation by the second gate biasing.

Keywords: IGZO, TCAD simulation, DOS, TFT, CPS.

1 Introduction

Oxide TFTs are nowadays starting to play an important role in display industry, with leading companies as LG using them in the backplane of recent products, such as curved organic light emitting device (OLED) TV sets. Still, significant advances in the current state-of-the-art of oxide TFT technology are required before high performance fully transparent, flexible, low-cost and low-power dissipation electronics reach the maturity level required for commercialization. The implementation of Technology Computer-Aided Design (TCAD) [1][2] tools for simulation of devices at a physical level can lead to understanding on how to further improve fabrication processes, material properties and device architectures. The ultimate goal is to enhance the performance of amorphous oxide TFTs, mimicking the routes followed for single-crystalline CMOS, a-Si and poly-Si technologies. Embedding physically-extracted parameters from the fabricated devices into the models for simulation, accurate models can be built and prediction on how changes in materials and processes affect physical response of the oxide TFTs can be achieved. This can allow viable process and device development and, simultaneously, understanding, the otherwise difficult or even impossible to extract physical

characteristics behind device operation. Some specific goals to be addressed are referred next.

As performance of amorphous oxide semiconductors (AOS) is controlled by the density of states (DOS) in a given material, and TCAD simulation is based in the DOS [3], it can provide understanding of the specific nature of states causing performance differences among different AOS. This can be used for instance to achieve a suitable and sustainable indium-free replacement for IGZO. Modeled IGZO TFTs based on DOS extracted from different techniques have shown to agree very well with measured characteristics, without employing any fitting parameter [4] [5]. Instabilities in oxide TFTs can be further investigated with TCAD, by implementing charge-trapping and defect creation in the simulations, allowing to understand the specific physical causes of degradation in TFTs, typically associated with Gate/Drain Bias Stress, illumination and temperature. Correlations between the defect-creation and the device performance degradation have been reported [6], with localization of defect creation being also investigated by means of simulations [7]. Some effects that limit device performance are related to device architecture, as parasitic capacitances that limit the maximum operation frequency, and short channel effects (SCE), which limit the scalability of the technology. As architectures can be arbitrarily defined in TCAD simulation optimization and understanding of physical phenomena in different geometries appears as a great advantage. Moreover, as recently more and more TFT architectures are proposed (e.g. dual-gate, floating-capping-metal, bulk-accumulation [8] and dual-active layer TFTs), TCAD can accelerate the optimization of those configurations, reducing fabrication runs and elucidating the physics behind the electrical behavior of each architecture [9].

In this work the short channel effect Drain Induced Barrier Lowering (DIBL) is shown with TCAD simulation in μm -scale IGZO TFTs. To the best of the authors' knowledge it's the first time that the barrier level for different drain bias is displayed for μm -scale oxide TFTs.

2 Integration in Cyber Physical Systems

Amorphous oxide electronics allow for production in a wide range of substrates, notably, inexpensive flexible and/or transparent substrates, as they can be processed at low temperatures (while still maintaining good performance) and have large area uniformity due to their amorphous nature. This way, they can be integrated into a wider range of systems, rather than their silicon technology counterparts. This technology thus shows to have great applicability in Cyber Physical Systems (CPS). In the CPS 5Cs architecture, amorphous oxides can be integrated in the Connection and the Conversion layers. In the Connection level they present the already discussed advantages of being applicable in wide range of substrates, as flexible and transparent ones. Several applications have already been reported as gas sensors [10], touch-panels [11] and even biological sensors [12]. Integrated with the connection level, the technology can also be in the conversion level as they have performance that allow for the processing of the information received at the Connection level. In fact, one of the current trends of oxide TFT technology is precisely focused on full integration and

in increasingly more complex circuits, including signal processing, amplification and, ultimately, analog-to-digital conversion [13].

3 TCAD Simulation

In this section some preliminary simulations are presented, addressing specific scenarios in which IGZO TFT devices, as produced in our group, show the need for improvement. Sputtered staggered bottom-gate TFTs on glass have been produced. A 60 nm thick Molybdenum (Mo) gate electrode was sputtered. The dielectric layer is a sputtered 100 nm thick 7 layer multicomponent oxide (alternating layers of SiO_2 and Ta_2O_5). The active layer is a 40 nm thick amorphous IGZO (with 2:1:1 composition in In:Ga:Zn atomic ratio), also sputtered. Finally, 60 nm thick Mo source and drain electrodes have been sputtered. All layers were patterned by photolithography and lift-off with exception of the dielectric layer, in which, photolithography and dry-etching have been used. A schematic of the fabricated devices can be seen in Fig. 1. After all layer fabrication devices were annealed at 180°C for 10 minutes in air in a rapid thermal annealing system. This fabrication process is compatible with commercial polymeric films.

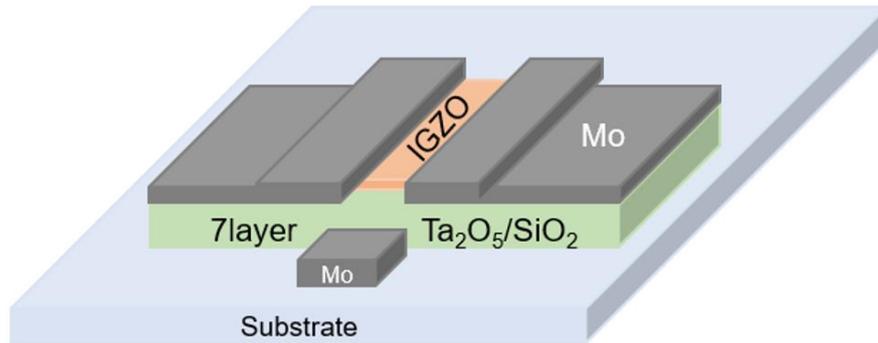


Fig. 1. Schematic of the sputtered IGZO TFTs.

For simulation purposes the TCAD Silvaco's 2D ATLASTM was used. A similar configuration than that of fabricated devices was employed. An electron mobility of $16\text{ cm}^2\text{ (V s)}^{-1}$ and electron concentration of 10^{16} cm^{-3} in the a-IGZO was assumed. Both fabricated and simulated TFTs have a channel length of $20\text{ }\mu\text{m}$ unless otherwise is specified. Channel width of the characterized TFTs is $20\text{ }\mu\text{m}$ and for simulated devices the obtained drain current in 2D simulation is factored in order to correspond to a $20\text{ }\mu\text{m}$ width channel TFT.

3.1 Short Channel Effects

Sputtered IGZO TFTs with channel length (L) below $5\ \mu\text{m}$ have exhibited SCEs, which are well known in silicon technology, where devices are of nm-scale. As low L ($5\ \mu\text{m}$ and below) IGZO TFTs have been reported with [14] and without [15] SCEs, TCAD simulation was used to investigate this physical limitation further, as the mechanisms for enabling or not the SCE are not clear yet. Preliminary simulations for similar TFTs showed that the short channel effects occur for $L = 0.5\ \mu\text{m}$. As shown in Fig. 2, turn-on voltage (V_{on}) shifts negatively with increasing drain bias in the simulated transfer characteristics. This effect is explained as Drain Induced Barrier Lowering (DIBL), as for low L drain bias can reduce the Source-Semiconductor Schottky junction barrier.

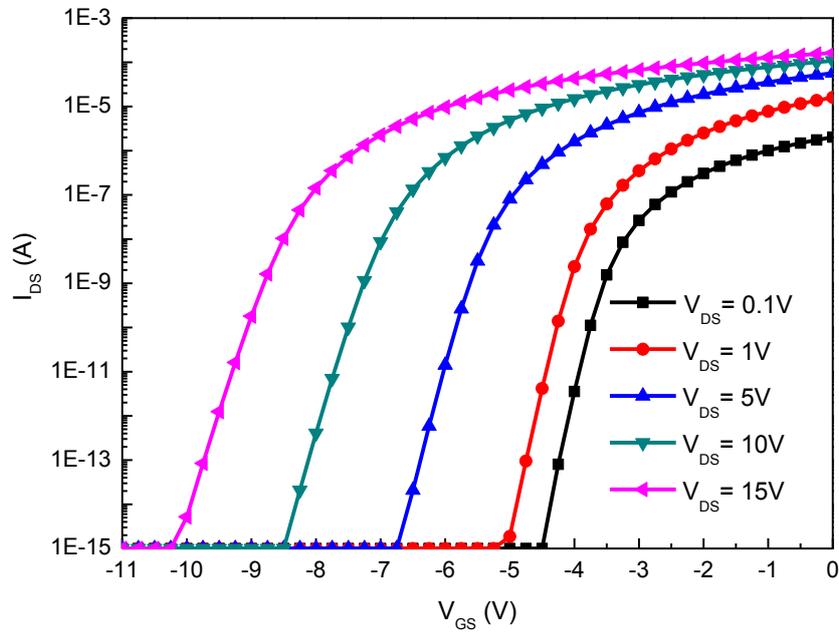


Fig. 2. V_{on} shift with increasing drain bias for simulated $L = 0.5\ \mu\text{m}$.

By extracting the conduction band energy level across the channel the decreasing of the barrier between source and semiconductor with increasing drain bias is clear, as shown in Fig. 3.

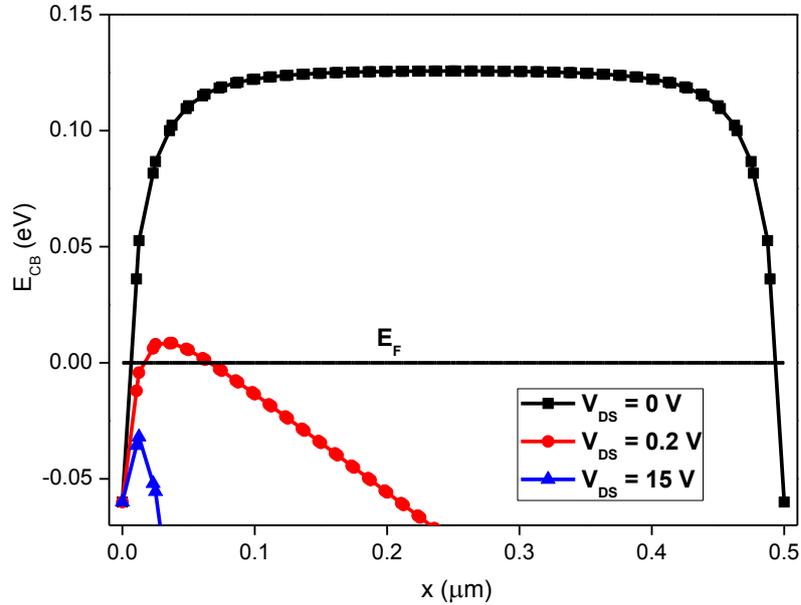


Fig. 3. Conduction band energy of IGZO in respect to the fermi level (E_F) for a $L=0.5 \mu\text{m}$ IGZO TFT, showing source-semiconductor barrier lowering (at $x=0\mu\text{m}$) for increasing drain bias.

3.2 Hump in Transfer Characteristics.

Performance degradation by irradiation, temperature and/or bias stress is one the main challenges for the application of oxide electronics. Fabricated devices showed hump like behavior in transfer characteristics after gate bias stress. This hump has been reported on several scenarios, and many different explanations have been reported so far. Some authors report it as a result of an effect of shallow donor-like states creation in the semiconductor [6]. Fig. 4 shows a simulation with increasing peak value of this shallow donor state, assuming 0.1eV of peak variance and a state energy 0.2 eV below conduction band, since energy states at this level have been reported [16]. The concentration increase in these states leads to the creation of an increasingly more visible hump, suggesting that it might be the (or at least, one of the) creation mechanisms for the hump.

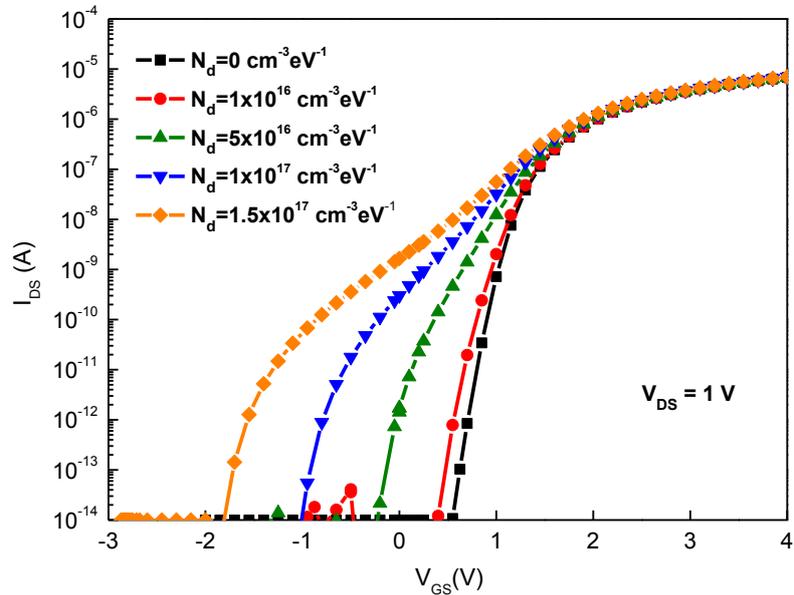


Fig. 4. Increasing of hump-like behavior in transfer characteristics of IGZO TFTs with increasing concentration of shallow donor-like states.

3.3 Dual-Gate TFT

Typically, fabricated IGZO TFT in our research group at CENIMAT/I3N at FCT NOVA show a depletion mode operation, which complicates its application in circuits. Some architectures for threshold voltage modulation have been already reported, as applying a second-gate on the back-interface of the semiconductor. Fig. 5 shows simulated transfer characteristics for dual-gated IGZO TFTs, with different fixed bias on the second gate. The added top gate and top gate oxide for dual-gate simulation are identical to the bottom gate and bottom gate oxide. As expected the V_{on} is modulated, which can be used to achieve enhancement mode devices.

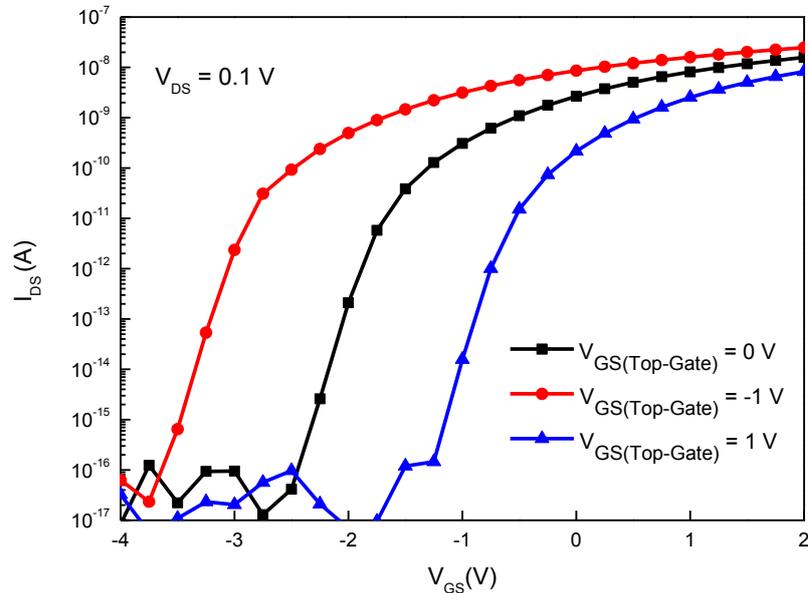


Fig. 5. Modulation of V_{on} in dual-gate IGZO TFT by second gate bias.

4 Conclusions and Future Work

TCAD simulations have demonstrated to be a powerful tool to improve understanding on amorphous oxide TFTs and reduce fabricated batches and costs. Short channel effects have been shown in simulations of IGZO TFTs, and these are in agreement to what was verified in fabricated devices by sputtering. Transfer characteristics shifted with drain bias, explained as DIBL, and the barrier has been effectively seen to reduce with drain bias observing the simulated conduction band energy in the IGZO. Further investigation on the SCEs, such as understanding the role of the schottky barrier, might elucidate on how to suppress these effects. As for the hump behavior, simulation showed that it may be somehow related to shallow donor-like state creation. Further investigation on how specific DOS affect the device characteristics will lead to understanding the mechanisms of degradation in the oxide TFTs. Finally, simulation of a double-gate TFT was employed, and the V_{on} modulation by the second gate bias was observed. This modulation can be used to achieve enhancement mode TFTs as preferred for application in circuit.

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