

Editor-in-Chief

A. Joe Turner, Seneca, SC, USA

Editorial Board

Foundations of Computer Science

Mike Hinchey, Lero, Limerick, Ireland

Software: Theory and Practice

Michael Goedicke, University of Duisburg-Essen, Germany

Education

Arthur Tatnall, Victoria University, Melbourne, Australia

Information Technology Applications

Ronald Waxman, EDA Standards Consulting, Beachwood, OH, USA

Communication Systems

Guy Leduc, Université de Liège, Belgium

System Modeling and Optimization

Jacques Henry, Université de Bordeaux, France

Information Systems

Jan Pries-Heje, Roskilde University, Denmark

ICT and Society

Jackie Phahlamohlaka, CSIR, Pretoria, South Africa

Computer Systems Technology

Paolo Prinetto, Politecnico di Torino, Italy

Security and Privacy Protection in Information Processing Systems

Kai Rannenber, Goethe University Frankfurt, Germany

Artificial Intelligence

Tharam Dillon, Curtin University, Bentley, Australia

Human-Computer Interaction

Annelise Mark Pejtersen, Center of Cognitive Systems Engineering, Denmark

Entertainment Computing

Ryohei Nakatsu, National University of Singapore

IFIP – The International Federation for Information Processing

IFIP was founded in 1960 under the auspices of UNESCO, following the First World Computer Congress held in Paris the previous year. An umbrella organization for societies working in information processing, IFIP's aim is two-fold: to support information processing within its member countries and to encourage technology transfer to developing nations. As its mission statement clearly states,

IFIP's mission is to be the leading, truly international, apolitical organization which encourages and assists in the development, exploitation and application of information technology for the benefit of all people.

IFIP is a non-profitmaking organization, run almost solely by 2500 volunteers. It operates through a number of technical committees, which organize events and publications. IFIP's events range from an international congress to local seminars, but the most important are:

- The IFIP World Computer Congress, held every second year;
- Open conferences;
- Working conferences.

The flagship event is the IFIP World Computer Congress, at which both invited and contributed papers are presented. Contributed papers are rigorously refereed and the rejection rate is high.

As with the Congress, participation in the open conferences is open to all and papers may be invited or submitted. Again, submitted papers are stringently refereed.

The working conferences are structured differently. They are usually run by a working group and attendance is small and by invitation only. Their purpose is to create an atmosphere conducive to innovation and development. Refereeing is also rigorous and papers are subjected to extensive group discussion.

Publications arising from IFIP events vary. The papers presented at the IFIP World Computer Congress and at open conferences are published as conference proceedings, while the results of the working conferences are often published as collections of selected and edited papers.

Any national society whose primary activity is about information processing may apply to become a full member of IFIP, although full membership is restricted to one society per country. Full members are entitled to vote at the annual General Assembly, National societies preferring a less committed involvement may apply for associate or corresponding membership. Associate members enjoy the same benefits as full members, but without voting rights. Corresponding members are not represented in IFIP bodies. Affiliated membership is open to non-national societies, and individual and honorary membership schemes are also offered.

Andreas Burg Ayşe Coşkun
Matthew Guthaus Srinivas Katkoori
Ricardo Reis (Eds.)

VLSI-SoC: From Algorithms to Circuits and System-on-Chip Design

20th IFIP WG 10.5/IEEE International Conference
on Very Large Scale Integration, VLSI-SoC 2012
Santa Cruz, CA, USA, October 7-10, 2012
Revised Selected Papers

Volume Editors

Andreas Burg
EPFL, Lausanne, Switzerland
E-mail: andreas.burg@epfl.ch

Ayşe Coşkun
Boston University, MA, USA
E-mail: acoskun@bu.edu

Matthew Guthaus
University of California, Santa Cruz, CA, USA
E-mail: mrg@soe.ucsc.edu

Srinivas Katkoori
University of South Florida, Tampa, FL, USA
E-mail: katkoori@cse.usf.edu

Ricardo Reis
Universidade Federal do Rio Grande do Sul
Porto Alegre, Brazil
E-mail: reis@inf.ufrgs.br

ISSN 1868-4238

e-ISSN 1868-422X

ISBN 978-3-642-45072-3

e-ISBN 978-3-642-45073-0

DOI 10.1007/978-3-642-45073-0

Springer Heidelberg New York Dordrecht London

Library of Congress Control Number: 2013953903

CR Subject Classification (1998): C.5.4, B.7, C.3, C.1, C.0, B.8, B.6, B.7

© IFIP International Federation for Information Processing 2013

This work is subject to copyright. All rights are reserved by the Publisher, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, reuse of illustrations, recitation, broadcasting, reproduction on microfilms or in any other physical way, and transmission or information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed. Exempted from this legal reservation are brief excerpts in connection with reviews or scholarly analysis or material supplied specifically for the purpose of being entered and executed on a computer system, for exclusive use by the purchaser of the work. Duplication of this publication or parts thereof is permitted only under the provisions of the Copyright Law of the Publisher's location, in its current version, and permission for use must always be obtained from Springer. Permissions for use may be obtained through RightsLink at the Copyright Clearance Center. Violations are liable to prosecution under the respective Copyright Law.

The use of general descriptive names, registered names, trademarks, service marks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

While the advice and information in this book are believed to be true and accurate at the date of publication, neither the authors nor the editors nor the publisher can accept any legal responsibility for any errors or omissions that may be made. The publisher makes no warranty, express or implied, with respect to the material contained herein.

Typesetting: Camera-ready by author, data conversion by Scientific Publishing Services, Chennai, India

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

Preface

This book contains extended and revised versions of the best papers that were presented during the 20th edition of the IFIP/IEEE WG10.5 International Conference on Very Large Scale Integration, a global System-on-a-Chip Design & CAD conference. The 20th conference was held at the Dream Inn Hotel, Santa Cruz, California, USA (October 7–10, 2012). Previous conferences have taken place in Edinburgh, Trondheim, Vancouver, Munich, Grenoble, Tokyo, Gramado, Lisbon, Montpellier, Darmstadt, Perth, Nice, Atlanta, Rhodes, Florianópolis, Madrid, and Hong Kong.

The purpose of this conference sponsored by IFIP TC 10 Working Group 10.5, the IEEE Council on Electronic Design Automation (CEDA), and by IEEE Circuits and Systems Society, with the In-Cooperation of ACM SIGDA, is to provide a forum for the exchange of ideas and presentation of industrial and academic research results in the field of microelectronics design. The current trend toward increasing chip integration and technology process advancements has brought about stimulating new challenges both at the physical and system design levels, as well as in the test of these systems. VLSI-SOC conferences aim to address these exciting new issues.

The 2012 edition of VLSI-SoC maintained the traditional structure of the conference, which has been successful at the previous VLSI-SOC conferences. The quality of submissions (110 regular papers and nine special session papers from 15 countries) made the selection process difficult. Finally 33 papers were accepted for oral presentation and 17 posters were accepted for presentation. Out of the 33 regular oral papers presented at the conference, 12 papers were chosen by a selection committee to have an extended and revised version included in this book. The selection of these papers has considered the evaluation scores during the review process and the review forms provided by members of the Technical Program Committee and session chairs as a result of the presentation. The chapters of this book have authors from Belgium, Brazil, China, Italy, Sweden, Switzerland and the USA. The Technical Program Committee comprised 97 members.

VLSI-SoC 2012 was the culmination of the work of many dedicated volunteers: paper authors, reviewers, session chairs, invited speakers and various committee chairs, especially the local arrangements organizers. We thank them all for their contribution.

This book is intended for the VLSI community, mainly those persons who did not have the chance to attend the conference. We hope you will enjoy

reading this book and that you will find it useful in your professional life and for the development of the VLSI community as a whole.

October 2013

Andreas Burg
Ayşe Coşkun
Matthew Guthaus
Srinivas Katkoori
Ricardo Reis

Organization

The IFIP/IEEE International Conference on Very Large Scale Integration-System-on-Chip (VLSI-SoC) 2012 took place during October 7–10, 2012, in the Dream In Hotel, Santa Cruz, California, USA. VLSI-SoC 2012 was the 20th in a series of international conferences, sponsored by IFIP TC 10 Working Group 10.5 (VLSI), IEEE CEDA, and ACM SIGDA.

General Chair

Matthew Guthaus UC Santa Cruz, USA

Program Chairs

Ayse Coskun Boston University, USA
Andreas Burg EPFL, Switzerland

Special Sessions Chair

Wentai Liu UC Santa Cruz, USA

Local Arrangements Chair

Jose Renau UC Santa Cruz, USA

Publication Chairs

Srinivas Katkoori Univ of South Florida, USA
Ricardo Reis UFRGS, Brazil

Publicity Chair

Ricardo Reis UFRGS, Brazil

Registration Chair

Rajsaktish Sankaranarayanan UC Santa Cruz, USA

Finance Chair

Baris Taskin Drexel, USA

PhD Forum Chair

Ken Pedrotti UC Santa Cruz, USA

Web Chair

Walter Condley UC Santa Cruz, USA

Steering Committee

Chi-Ying Tsui	HKUST, Hong Kong, SAR China
Manfred Glesner	TU Darmstadt, Germany
Luis Miguel Silveira	INESC ID, Portugal
Salvador Mir	TIMA, France
Ricardo Reis	UFRGS, Brazil
Michel Robert	University of Montpellier, France

Table of Contents

FPGA-Based High-Speed Authenticated Encryption System	1
<i>Michael Muehlberghuber, Christoph Keller, Frank K. Gürkaynak, and Norbert Felber</i>	
A Smart Memory Accelerated Computed Tomography Parallel Backprojection	21
<i>Qiuling Zhu, Larry Pileggi, and Franz Franchetti</i>	
Trinocular Stereo Vision Using a Multi Level Hierarchical Classification Structure	45
<i>Andy Motten, Luc Claesen, and Yun Pan</i>	
Spatially-Varying Image Warping: Evaluations and VLSI Implementations	64
<i>Pierre Greisen, Michael Schaffner, Danny Luu, Val Mikos, Simon Heinzle, Frank K. Gürkaynak, and Aljoscha Smolic</i>	
An Ultra-Low-Power Application-Specific Processor with Sub- V_T Memories for Compressed Sensing	88
<i>Jeremy Constantin, Ahmed Dogan, Oskar Andersson, Pascal Meinerzhagen, Joachim Rodrigues, David Atienza, and Andreas Burg</i>	
Configurable Low-Latency Interconnect for Multi-core Clusters	107
<i>Giulia Beanato, Igor Loi, Giovanni De Micheli, Yusuf Leblebici, and Luca Benini</i>	
A Hexagonal Processor and Interconnect Topology for Many-Core Architecture with Dense On-Chip Networks	125
<i>Zhibin Xiao and Bevan Baas</i>	
Fault-Tolerant Techniques to Manage Yield and Power Constraints in Network-on-Chip Interconnections	144
<i>Anelise Kologeski, Caroline Concatto, Fernanda Lima Kastensmidt, and Luigi Carro</i>	
On the Automatic Generation of Software-Based Self-Test Programs for Functional Test and Diagnosis of VLIW Processors	162
<i>Davide Sabena, Luca Sterpone, and Matteo Sonza Reorda</i>	

SEU-Aware Low-Power Memories Using a Multiple Supply Voltage Array Architecture	181
<i>Seokjoong Kim and Matthew R. Guthaus</i>	
CMOS Implementation of Threshold Gates with Hysteresis	196
<i>Farhad A. Parsan and Scott C. Smith</i>	
Simulation and Experimental Characterization of a Unified Memory Device with Two Floating-Gates	217
<i>Neil Di Spigna, Daniel Schinke, Srikant Jayanti, Veena Misra, and Paul Franzon</i>	
Author Index	235