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**Abstract.** A simple method to tune the output pole of a passive mixer is proposed which leads to up to 33 dB improvement in an IEEE 802.15.4 standard compatible receiver's IF section $IIP_3$. This method is used in the design of an ultra-low power receiver front-end which consumes just 2.2 mW from a 1-V supply while achieving a SSB NF of approximately 9 dB. The energy-aware architecture allows for a 70 % reduction in the nominal power consumption (down to 0.7 mW) under strong signal conditions while improving the receiver's $IIP_3$ and not affecting the receiver's input matching. The receiver is designed in a 0.18-µm RFCMOS technology.

**Keywords: RF Front End, CMOS RF Integrated Circuits, Low Power, System on Chip.**

## 1 Introduction

The demand for low power, low data-rate, short-range communications for applications such as wireless sensor networks (WSN) for home and factory automation, and wireless personal area networks (WPAN) devices such as wireless mice and keyboards, has led to significant research in the field of low power RF CMOS IC design [1]-[9]. In 2003, the IEEE introduced the IEEE 802.15.4 standard [10] in order to accommodate such applications. The standard features relaxed noise and linearity requirements making ultra-low power design possible.

Typically, low-IF and direct-conversion receiver architectures are used in such applications where the receiver front-end would commonly be configured as shown in Fig. 1. The architecture consists of an off-chip band-select filter, an LNA, IQ mixers, and channel-select filters. In direct-conversion systems, low-pass channel filters are used [5], while complex band-pass channel filters are used in low-IF systems [1], [6]. In the 2.4 GHz Industrial, Scientific and Medical (ISM) Band, the receiver designs which consume the lowest power are presented in [2], and [3], and use 1.4 mW and

0.75 mW respectively. However, both designs involve significant tradeoffs which do not necessarily permit their use for the IEEE 802.15.4 standard [7] (neither work was designed to be compatible with the IEEE 802.15.4 standard). For instance, in [2], the $IIP_3$ is only -37 dBm which is insufficient to meet the standard's requirements. Furthermore, the NF was tested at an IF of 10 MHz and the authors did not discuss the possibility of lowering the IF. In [3], no input matching is used [11], which can lead to interface problems with external components, and no LNA is used, which can result in unwanted transmission of the local oscillator (LO) signal. Among works specifically designed to meet the IEEE 802.15.4 standard, the lowest power consumption is used in [4], at 4.05 mW.

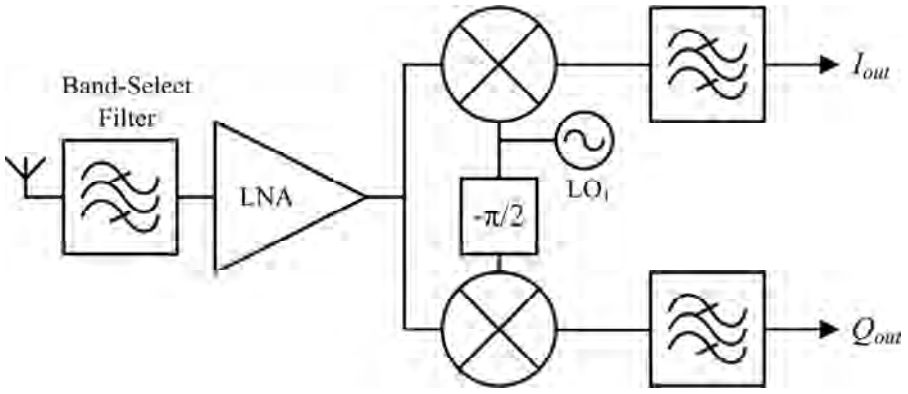


**Fig. 1.** A typical front-end for a low-IF or direct-conversion receiver.

In this work, we present a passive mixer architecture which when used, allows for an ultra-low power IF section. This architecture was originally presented in [12] (simulated results only), and has been used to design a receiver front-end which consumes just 2.2 mW from a 1-V supply. We also build upon our previous research on energy-aware design [7], designing the receiver's power consumption to be controllable down to 0.7 mW. The proposed energy-aware design technique also makes the receiver's input matching virtually independent of the LNA power consumption. For the remainder of this paper, the front-end refers to the part of the receiver up to the channel filtering, and the IF section refers to the IF channel filter, where it is understood that there is no IF in a direct-conversion system, and the signal is directly translated to baseband.

## 2 Passive Mixer Architectures

For short-range, low-data-rate communications, CMOS based designs generally favor the use of passive down-conversion mixers as opposed to active mixers. On the positive side, passive mixers do not consume power, and offer very low flicker noise and high linearity. However, passive mixers essentially present a resistance in series with the signal path which can be noisy, and may also require a higher LO drive than

their active counterparts. Active mixers work on the principle of current-commutation and offer the advantages of high output impedance, and better port to port isolation. Unfortunately, they tend to degrade linearity, and add considerable flicker noise. The disadvantages of active mixing as applied to short-range, low-data-rate systems outweigh the benefits.

To get an idea of how well different receivers perform using active and passive mixers, we can look at their overall sensitivity. The sensitivity can be broken down into two types, noise figure (NF) limited sensitivity, and third-order intercept ($IIP_3$) limited sensitivity. Since the overall performance of a receiver can be broken down into several nearly independent performance parameters (NF, $IIP_3$, phase noise, DC-offset, etc), other limiting factors on sensitivity are possible. Here we will only look at the NF, and the $IIP_3$ as they generally are the more dominant parameters which limit overall sensitivity [1]-[7]. *NF* limited sensitivity is easily calculated as,

$$\mathrm{Sen_{NF}} = \mathrm{NF} + 10\log(kT\Delta f) + \mathrm{SNR_{req}} \qquad (\mathbf{1})$$

while $IIP_3$ limited sensitivity is calculated as,

$$\mathrm{Sen_{IIP3}} = -3 + 3\mathrm{P_{blk}} + \mathrm{SNR_{req}} - 2\mathrm{IIP_3} \qquad (\mathbf{2})$$

where $k$ is Boltzmann's constant, T is the temperature in Kelvin (normally taken as 290 K), $\Delta f$ is the bandwidth (2 MHz in this case), $\mathrm{SNR_{req}}$ is the required SNR, and $\mathrm{P_{blk}}$ is the power of the interfering signals. The addition of -3 in (2) accounts for the fact that $IIP_3$ should be measured with the desired signal 3 dB above the sensitivity level. The IEEE 802.15.4 standard specifies +0 dBc and +30 dBc interferers at the adjacent and alternate channels while the input signal is 3 dB above the sensitivity level (-85 dBm). Therefore, for the calculation of $\mathrm{Sen_{IIP3}}$, $\mathrm{P_{blk}}$ is set to -52 dBm. Based on [13], we estimate the required SNR to be approximately 14 dB. Based on (1) and (2), the required NF and $IIP_3$ can be calculated as 12 dB and -30 dBm respectively. Table 1 compares the sensitivities of several recently published low-power designs. As this work primarily deals with lowering the IF section power consumption, we also include the required IF section power consumption in Table 1.

**Table 1.** Overall Sensitivity Versus Mixer Type for Recent low-Power Front Ends

| Reference | [1] | [2] | [3] | [4] | [5] | [6] | [7][B] |
|---|---|---|---|---|---|---|---|
| $Sen_{NF}$ (dBm) | -91.3 | -92 | -91.9 | -91 | -89.7 | -87 | -90.7 |
| $Sen_{IIP3}$ (dBm) | -110 | -68 | -127 | -118 | -126 | -112 | -88 |
| Mixer Type[A] | PC | A | PV | PV | PC | A | PC |
| Tech. (nm) | 180 | 180 | 130 | 90 | 180 | 180 | 180 |
| Power (mW) | 10 | 1.4 | 0.75 | 4.05 | 6.3 | 10.8 | 5.4 |
| IF Power (mW) | 5.76[C] | 0.5 | 0.75 | 1.15 | 4.5 | - | 0.36 |

[A] A: Active, PV: Passive Voltage-mode, PC: Passive Current-mode

[B] Second gain mode

[C] Estimated only.

From Table 1, for the designs using active mixers, the $IIP_3$ limited sensitivity in [2] is poor, while [6] consumes the most power and achieves the poorest $Sen_{NF}$. Although these findings are not conclusive, a trend is observable. It is well understood that the overall NF of the system is limited by the NF of the first LNA. This leads to rather high LNA power consumption in order to keep the NF low. However, the average front-end in Table 1 allocates 48 % of the power consumption to the IF section which indicates that the IF section still takes a significant portion of the overall power consumption. This work explores a mixer architecture which allows for an ultra-low power IF section.

### 2.1 Current-Mode and Voltage-Mode Passive Mixers

In Table 1, we have identified two classes of passive mixers. For passive mixers where the input impedance of the IF section is small compared to the passive mixer core's output impedance, we term the passive mixer a current-mode passive mixer. For passive mixers where the input impedance of the IF section is large compared to the passive mixer core's output impedance, we term the passive mixer a voltage-mode passive mixer. A basic diagram of current-mode and voltage-mode passive mixers is shown in Fig. 2. The passive mixer core is represented by a variable resistor whose resistance is controlled by a local oscillator (LO) voltage. The current-mode passive mixer core is normally followed by a transimpedance amplifier (TIA) [14], which can easily be modified into a channel-select filter (CSF) [1], [15]. In Fig. 2, the TIA is modified to form a simple low-pass filter.

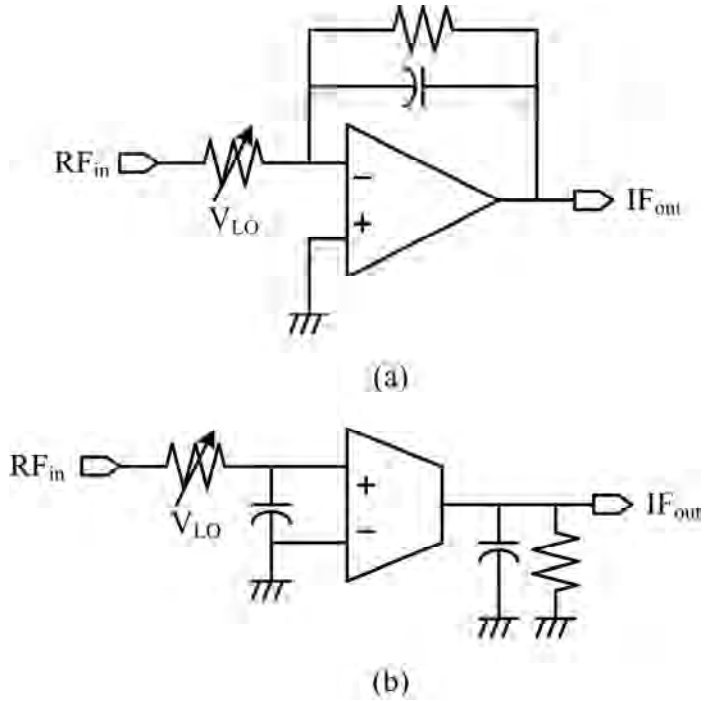


**Fig. 2.** A simplified illustration of connection between (a) a current-mode passive mixer and an op-amp based filter, and (b) a voltage-mode passive mixer and a $g_m$-C based filter.

### 2.2 IF Section Pre-Filtering

Both the current-mode and the voltage-mode passive mixers offer the possibility of pre-filtering the signal before the IF section. What we mean by this is that a single stage of filtering is realized before the signal is passed through any active components in the IF section. For the voltage-mode passive mixer in Fig. 2 (b), this is obvious as the mixer core's variable resistance forms an RC pole with the input capacitance of the IF section. This RC low-pass filter precedes any active amplification (in the IF section).

For the current-mode passive mixer this is also true. We illustrate this in Fig. 3. Assume the op-amp has a frequency-dependent gain as shown in Fig. 3 on the left y-axes. In Fig. 3 (a), we show the case where the TIA is formed by removing the capacitor in Fig. 2 (a). In Fig. 3 (b), we show the case where the TIA has been turned into a CSF using the circuit shown in Fig. 2 (a). Assuming the input to the overall filter is some represented by some broadband signal, the outputs to the op-amps would appear as they do in Fig. 3. The output in Fig. 3 (b) roughly corresponds to a broadband signal that has been filtered by a first order filter with a 1-MHz corner frequency while that in Fig. 3 (a) corresponds to a broadband signal that has been amplified. By extension, the inputs to the op-amps (not the inputs to the overall

filters) must by equal to the outputs after subtracting the op-amp gain. The op-amp inputs are also shown in Fig. 3 and three discrete tones, *A*, *B*, and *C* are also shown. Clearly, the op-amp input level is reduced above the corner frequency for the op-amp based CSF. The reduced out-of-band input level leads to better out-of-band $IIP_3$.

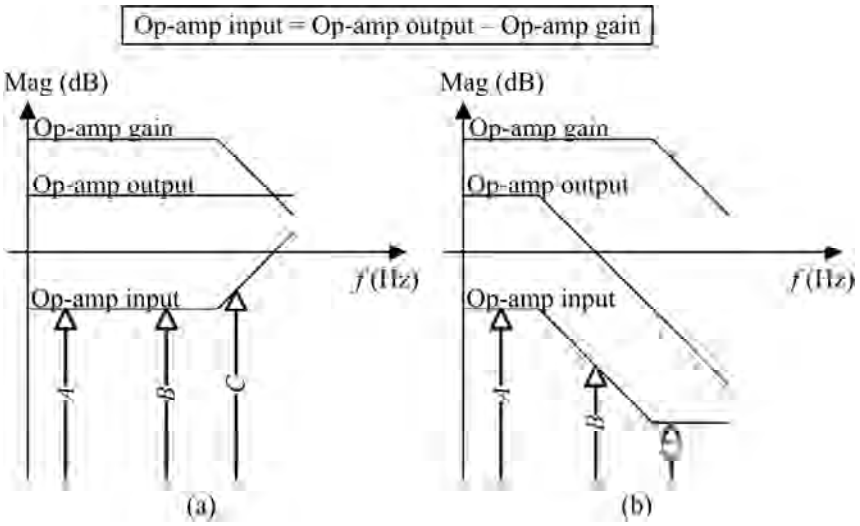


**Fig. 3.** Illustration of the pre-filtering effect of an op-amp based CSF. (a) The case with an op-amp based TIA, and (b) the case with an op-amp based CS

The effect of this pre-filtering on the IF section (when compared to the case without pre-filtering) for both voltage- and current-mode passive mixers is a tremendous reduction in the required IF section $IIP_3$. We can estimate the required $IIP_3$ in dBm of the IF section as,

$$IIP_{3,IF} = \tfrac{1}{2}[2P_{blk1} + P_{blk2} - (P_{sen} - 3) + SNR_{req}] + G_{RF} \quad (\mathbf{3})$$

where $P_{blk1}$ and $P_{blk2}$ are the power of the two interfering tones, $P_{sen}$ is the required sensitivity level, and $G_{RF}$ is the gain of the RF section. The addition of 3 comes from the requirement of the desired signal being 3 dB above the sensitivity level [10]. The derivation of (3) is rather straightforward, and is found by calculating the input level which causes the 3$^{rd}$-order intermodulation component to exceed the allowable noise floor. The channel interference profile which the receiver must be able to tolerate is rather simple [6] and is shown in Fig. 4 (a) at the IF (after down-conversion) for a direct-conversion system. Based on the interference profile, we can estimate the required IF section $IIP_3$ under two worst-case scenarios.

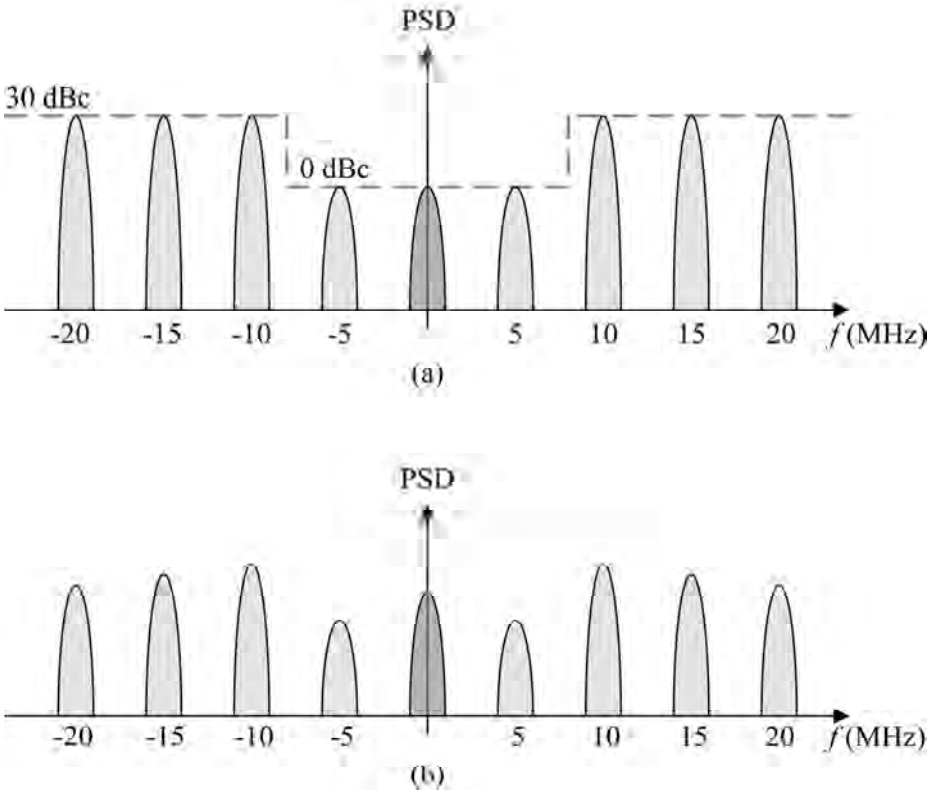


**Fig. 4.** Illustration of the effect of a single pole low-pass filter on IEEE 802.15.4 standard interference (a) before and (b) after filtering. The striped signals are interferers while the shaded signal is the desired signal.

The first scenario is when two blockers, in the adjacent and alternate channels respectively, intermodulate to create in-band distortion. Hence $P_{blk1}$ is equal to -82 dBm, and $P_{blk2}$ is equal to -52 dBm. If the gain of the RF section is 30 dB, then the required IF section $IIP_3$ in the first case is equal to -30 dBm. The second scenario involves two interferers in the alternate channel and at 20-MHz offset respectively. Both $P_{blk1}$ and $P_{blk2}$ are equal to -52 dBm. For the same RF section gain, the required $IIP_3$ of the IF section is 0 dBm. The overall receiver $IIP_3$ requirement is easily calculated by simply subtracting $G_{RF}$ (30 dB) from the above results.

At a zero IF, the IEEE 802.15.4 standard signal bandwidth is 1 MHz [1]. The effect of a 1-MHz pre-IF section filter on the IEEE 802.15.4 standard interferers is shown in Fig. 4 for a direct conversion system. The adjacent channel is filtered by 20log(5MHz/1MHz) = 14 dB, while the alternate channel is filtered by 20log(10MHz/1MHz) = 20 dB. For the first scenario mentioned above, the effect on the required IF section $IIP_3$ is equal therefore equal to a reduction of 14 dB + ½ * 20 dB = 24 dB. For the second scenario, the required IF section $IIP_3$ is reduced by 20 dB + ½ * 13 dB = 33 dB. This is evident from (3). With such a reduction in IF section required $IIP_3$, one has the option of either increasing the LNA/Mixer gain, reducing

the IF section $IIP_3$, or doing some combination of both. Both alternatives can lead to very low IF section power consumption.

### 2.3 Voltage-Mode versus Current-Mode Passive Mixers

We have illustrated how both voltage-mode and current-mode passive mixers offer the advantage of effectively pre-filtering the signal before active amplification. In this application, power consumption is critical. The filtering ability of op-amp based CSFs is determined by the unity-gain bandwidth (UGB) of the loop-gain of the feedback system. As the loop-gain falls below unity, the overall gain of the feedback system deviates from its ideal closed-loop gain, and the feed-forward path tends to dominate the transfer function [16]. As the filter only behaves correctly up to the UGB of the loop gain, it is desirable to have a high UGB op-amp. The UGB of an op-amp is limited by its power consumption under a given load condition. This is because for stability purposes, the UGB is generally limited by the non-dominant pole frequency. For instance, in a simple Miller compensated op-amp, for a 45 degree phase margin, the UGB is equal to the non-dominant pole frequency, and the non-dominant pole frequency is approximately equal to $g_{m2}/C_L$, where $g_{m2}$ is the transconductance of the second stage, and $C_L$ is the load capacitance. Increasing $g_{m2}$ requires increasing the power consumption.

A major advantage of op-amp based active-RC filters is their excellent linearity resulting from their use of feedback. It can be shown that the $IIP_3$ and $IIP_2$ of a feedback system improves with the loop gain as [17], [18],

$$V_{IIP3,after} = V_{IIP3,before}(1 + LG)^{1.5}\,, \tag{4}$$

$$V_{IIP2,after} = V_{IIP2,before}(1 + LG)^{3}\,, \tag{5}$$

where LG is the loop gain, $V_{IIPn,\mathit{before}}$ is the $IIP_n$ in volts before closing the feedback loop, and $V_{IIPn,\mathit{after}}$ is the $IIP_n$ in volts after closing the feedback loop.

$G_m$-C type filters can generally be designed to operate at higher frequencies than their active-RC counterparts. The simplest possible transconductor in CMOS technology is a single MOSFET, and for differential circuits, a transconductor can take the form of a differential pair. Such a simple design inevitably achieves good noise performance due to the low component count (fewer noise generators). This naturally relaxes the power consumption requirements of the transconductor. Compared to an op-amp based active-RC filter, however, a $G_m$-C filter using simple differential pair suffers from significantly poorer linearity. Therefore, in most $G_m$-C filters, some form of transconductor linearization is needed [19].

## 3 The Proposed Architecture

In this work, rather than trying to linearize the transconductors, we use the idea of pre-filtering the signal using the passive-mixer's output pole. As this RC pole forms a first-order low-pass filter, the mixer favors a direct-conversion receiver architecture. A third-order Butterworth response provides sufficient filtering of the interference for the IEEE 802.15.4 standard [1], and since the real pole is formed at the passive mixer output, only a second-order active filter is necessary to form the desired response.

The benefits of using the proposed mixer architecture can be summarized as follows: low-power $G_m$-C filters can be used, transconductor linearization is unnecessary, and only two active filter stages are necessary (as opposed to three in the current-mode passive mixer implementation). Unfortunately, the real pole formed by the switch resistance and the output capacitance of the voltage-mode passive mixer is generally not used for filtering because of the considerable variation in the switch resistance. The switch resistance can vary due to uncertainty in the LO voltage ($V_{LO}$), the switch threshold voltage, the switch size, and even the output impedance of the previous stage (the LNA output resistance affects the passive mixer output resistance [7]). Therefore, in order to ensure that the CSF behaves properly, the output pole of the voltage-mode passive mixer must be tuned. The proposed receiver architecture including the passive mixer tuning circuit is shown in Fig. 5. The tuning technique will be discussed in the section describing the passive mixer.

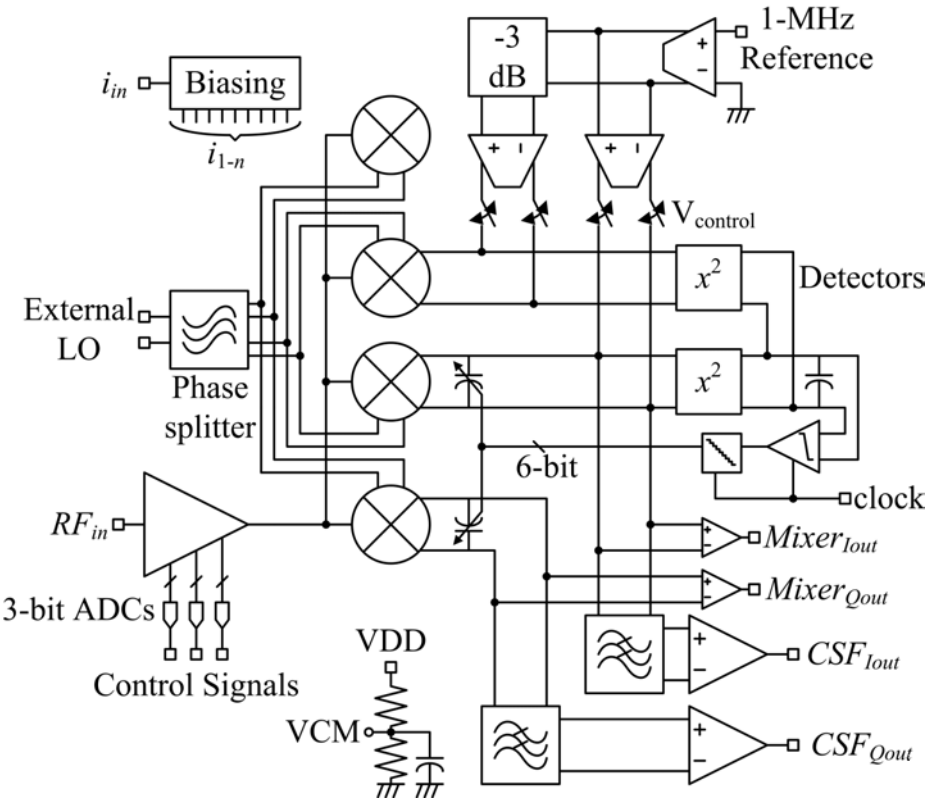


**Fig. 5.** A complete schematic of the proposed receiver front-end including the LNA, passive mixers, CSF, output buffers, LO phase splitter, and passive mixer tuning circuitry.

### 3.1 The Low-Noise Amplifier

The low-noise amplifier was implemented as a single-ended, single stage common-source amplifier. The schematic is shown in Fig. 6. The core of the amplifier is a simple common-source cascode configuration which offers good reverse isolation, and high output impedance. The transconductance of the core is controllable via $V_{C1}$ to $V_{C3}$ in 6 dB steps, and this also controls the power consumption of the LNA in the same proportion. The input and output frequency selective networks were made tunable (using digitally controlled capacitor banks) in order to avoid any frequency offset which may result from inadequate passive device modeling. The quality factor of the input and output frequency selective networks are 1.77 and 6.01 respectively. These networks were only tuned once before performing all of the main measurements and were not re-tuned for different power states.

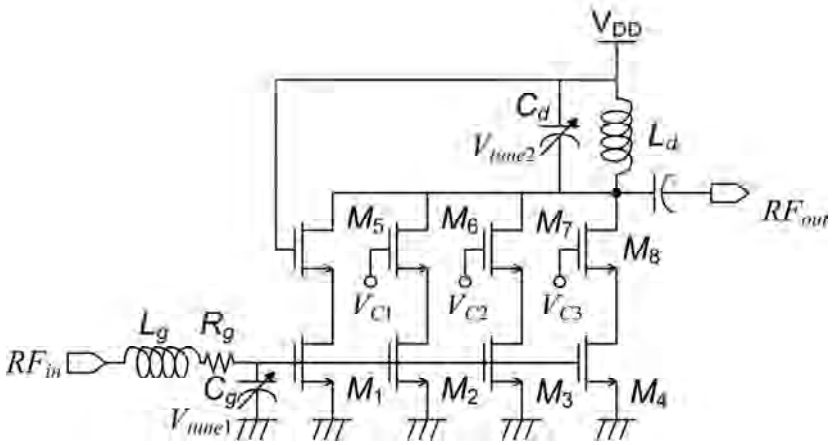


**Fig. 6. Schematic of the proposed LNA. $V_{C1}$ to $V_{C3}$ control the gain/power consumption state of** the amplifier, while $V_{tune1}$ and $V_{tune2}$ tune its frequency response.

Transistors $M_1$-$M_4$ are biased in the weak-inversion region [20], which has been shown to offer improved performance in the low GHz frequency range as compared to strong-inversion biasing. One way of accessing a transistor's overall performance is by looking at its maximum unilateral transducer gain, $G_{TUmax}$ [21]. However, in practice, the quality factor of on-chip inductors limits the amount of voltage gain that can be achieved in a step-up matching network, and this is not reflected in the $G_{TUmax}$ of a transistor. In order to correct for this, we have simulated $G_{TUmax}$ for a transistor in a 0.18-µm RFCMOS process design kit (PDK) with 500-ohm shunt resistors added to the gate and drain nodes of the transistor (Fig. 7). The device drain current was set to 1 mA while the device width was swept. The threshold voltage was 0.48 V. From Fig. 7, $G_{TUmax}$ is higher in the strong-inversion region at very high frequencies, but at very low frequencies, $G_{TUmax}$ is optimum in the weak-inversion region. In this case, at 2.4 GHz, a gate-overdrive voltage of 35 mV appears to be optimum.

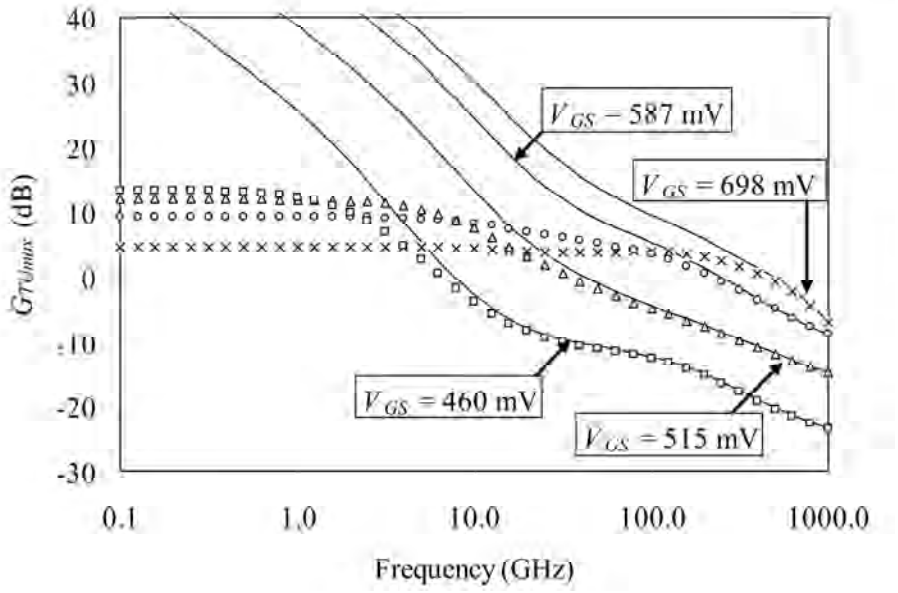


**Fig. 7.** Simulated transistor $G_{TUmax}$ with (scatter plots) and without (solid line) 500-ohm resistors added in shunt to the gate and drain terminals. $G_{TUmax}$ is higher in the strong-inversion region at very high frequencies, but higher in the weak-inversion region at very low frequencies. The drain current was fixed to 1 mA for all cases while the device width was swept.

In practice, it is difficult to power match a device directly to 50 ohm at 2.4 GHz due to the low quality factor of on-chip passive elements. Designers normally opt to create a virtual input resistance to match to, and inductive degeneration is a popular choice due to its ability to provide nearly simultaneous noise and impedance matching [22], while improving the linearity due to the use of feedback. However, it should be remembered that this impedance matching does not power match the device, and hence does not maximize the power output of the device. In cases where impedance matching is necessary, but a very low *NF* is not critical, impedance matching can be achieved by simply directly adding a resistor in series with the gate [20] and resonating out the gate-source capacitance as is done in Fig. 6. In our case, inductive degeneration is not a viable option since the LNA power control would affect the input resistance differently at different power levels. In our design, the input impedance is virtually independent of the power state since $M_1$-$M_4$ remain connected to the input node and in the on-state for all four power states.

Fig. 8 shows the measured *S*-parameters of the LNA for all power states. The input impedance of the mixer was simulated to be 2 kΩ, and this is chosen as the termination resistance of the LNA output port for measurement. The voltage gain of the LNA is found by adding 16 dB to $S_{21}$ to account for the step up in impedance from the 50-Ω input to the 2-kΩ output. From the figure, the input reflection coefficient is nearly independent of the power state, while the $S_{21}$ shows a 6 dB gain step. The S-

parameters were measured by using a 50-Ω vector network analyzer (VNA) and then mathematically converting the output port to 2 kΩ [23]. When probing the LNA output, the mixer was turned off to prevent it from loading the LNA. The measured LNA *NF* is shown in Fig. 9. At the highest gain/power state, the measured *NF* is 4.8 dB at the center frequency. This is acceptable given the overall required *NF* of 12 dB. It is of note that for the proposed matching scheme, the minimum achievable *NF* is more than 3 dB.

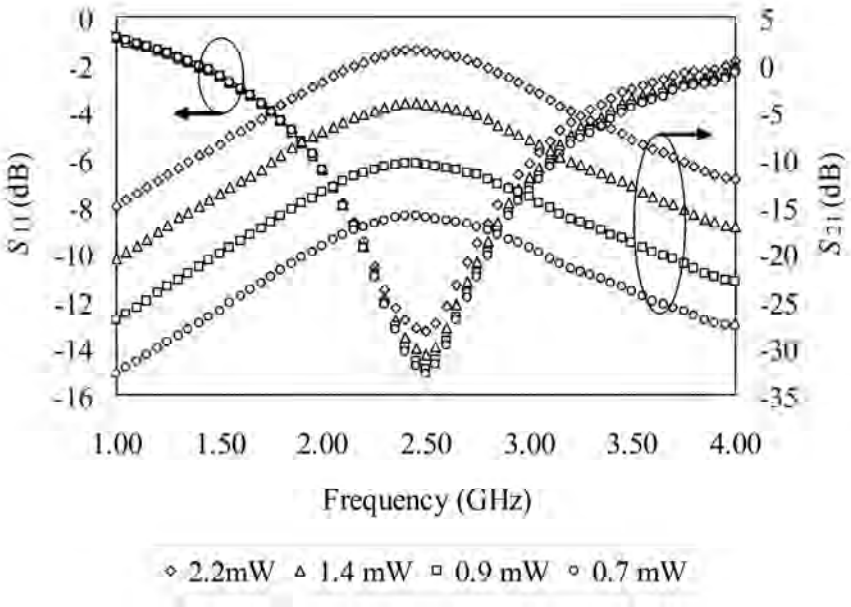


**Fig. 8.** Measured *S*-parameters of the LNA for all four receiver power states. The input port is terminated in 50 Ω while the output port is terminated in 2 kΩ. For the voltage gain, 16 dB should be added to $S_{21}$.

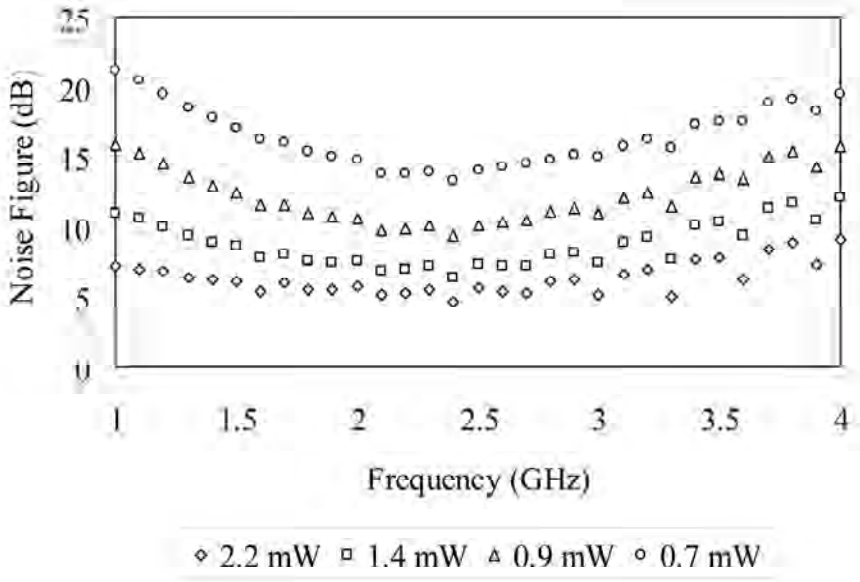


**Fig. 9.** Measured *NF* of the proposed LNA for all four receiver power states.

### 3.2 The Passive Mixer

The passive mixer consists of a switching core, replica passive mixers, and a tuning loop. These are shown in Fig. 10. The core switches act as variable resistors in series with the signal path, and hence were sized according to a tradeoff between noise performance, and capacitive loading to the LNA and frequency synthesizer. In this work, the 2.4 GHz LO signal is provided by a signal generator external to the chip, and split into quadrature signals using an on-chip RC poly-phase filter. The simulated LO amplitude is 300 mV for each switch. The IQ mixer core in the signal path is differentially loaded by tunable capacitors at each output, with a unit capacitance of 100 fF and 6-bit control.

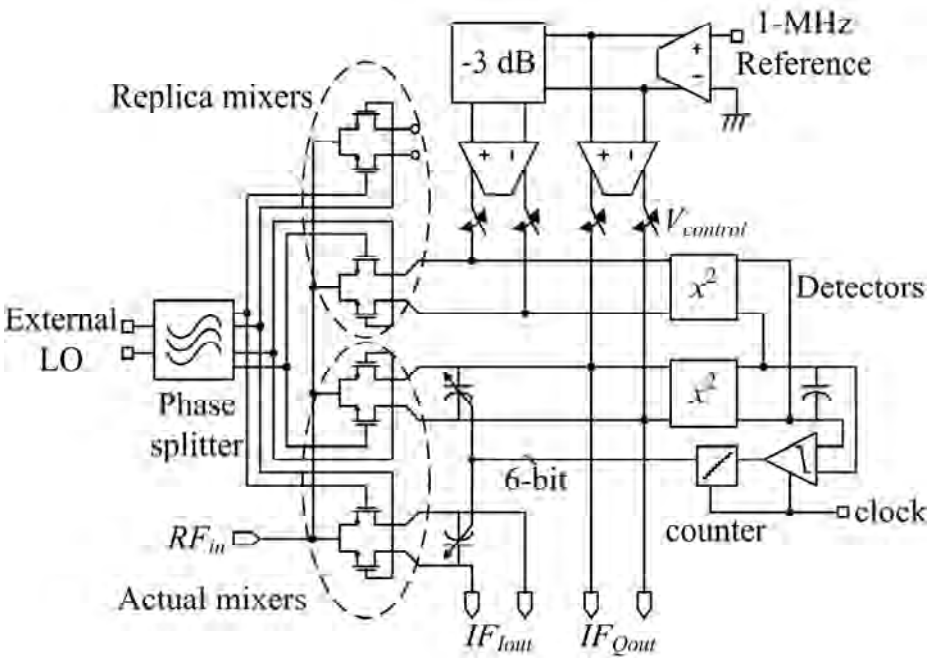


**Fig. 10.** Complete schematic of the proposed tuned-output-pole passive mixer.

The mixers also perform the single-ended to differential conversion operation. This allowed the use of a single-ended LNA thereby saving half of the LNA power consumption. The justification for this strategy is the relaxed $IIP_2$ requirements of the IEEE 802.15.4 standard. The main concern is unwanted DC-offset related to the self-mixing of either LO signals or strong interfering signals. Self mixing of LO signals results in a static DC offset which can be filtered before introducing any high gain stages to the signal. We can estimate the required $IIP_2$ based on self mixing of interfering signals as,

$$IIP_{2,req}(\text{dBm}) \geq 2P_{blk} - (P_{sen} + 3) + SNR_{req} \quad (\mathbf{6})$$

Given alternate channel interferers equal to -52 dBm, the required *$IIP_2$ is* 2(-52) – (-82) + 14 = -8 dBm. The achieved $IIP_2$ of the down-converter can be estimated as $P_{LO}/G_{leak}$ where $G_{leak}$ is the ratio of the differential RF signal at the gates of the switching stages to the single-ended RF signal at the source of the switching stages (note that $G_{leak}$ does not include common-mode leakage) and $P_{LO}$ is the LO power. $G_{leak}$ is effectively a single-ended to differential leakage gain. In [24], it is shown that the $IIP_2$ of active mixers has similar dependency, while $IIP_2$ on the order of +40 dBm is typical.

To understand the operation of the tuning loop, we must first state that $IF_{Iout}$ and $IF_{Qout}$ are loaded by capacitive impedances. The replica passive mixer cores in Fig. 10 have no explicit capacitive loading and therefore, at the desired tuning frequency (1

MHz), present an impedance which is 3-dB higher than the impedance presented by the actual mixer core. We can inject 1-MHz signals into the mixer output nodes without affecting the impedances at the mixer nodes by using high output impedance transconductance amplifiers. On the replica mixer side, the 1-MHz reference signals are pre-attenuated by 3-dB to account for the 3-dB higher mixer output impedance. The resulting voltages which develop at the actual mixer output and the replica mixer output are then compared and used to tune the load capacitance of the actual mixer.

For the comparison loop, the two 1-MHz signals are first squared using Gilbert-Cell based multipliers. The outputs of the multipliers include even order harmonics which are filtered using a low-pass filter. The level of the harmonics determines the corner frequency of the loop filter and hence the maximum rate at which the comparator and counter can be clocked. As the Gilbert-Cells output a current-mode signal, the replica signal is easily subtracted from the desired signal before filtering. The resulting differential signal is input to a comparator to extract its sign. The output of the comparator drives a counter which is used to either increase or decrease the actual mixer's load capacitance. The comparison loop was designed simply to illustrate the principle of the proposed mixer. In theory, the loop could be significantly sped up by using a successive approximation architecture, or by attempting to cancel off the even-order harmonics. Fig. 11 shows the voltage on the loop filter node. When it reaches its steady state, the 6-bit control signal oscillates around the desired value by 1 least-significant-bit (LSB).

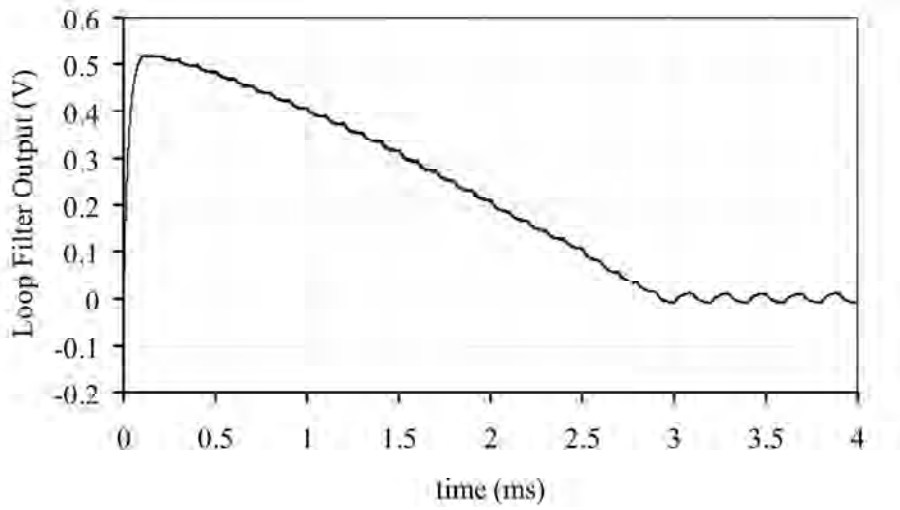

**Fig. 11.** he loop filter voltage versus time upon initiation of the tuning sequence.

### 3.3 The $G_m$-C Filters

As previously mentioned, the first pole of the third-order Butterworth filters were provided by the output pole of the IQ passive mixer. Therefore, the active $G_m$-C filters are of second-order. A schematic of the filters is shown in Fig. 12. Each transconductor consists of a simple differential pair, and selected amplifiers include common-mode feedback (CMFB). It is easy to show that the DC gain of the filter is equal to $g_{m1}/g_{m2}$ while the corner frequency is equal to $C^{-1}\sqrt{(g_{m2}g_{m3})}$ and the $Q$ is equal to $\sqrt{(g_{m3}/g_{m2})}$. With four variables and three equations, we have one degree of freedom. This was used to select $g_{m1}$ to provide the desired overall noise performance of the receiver system.

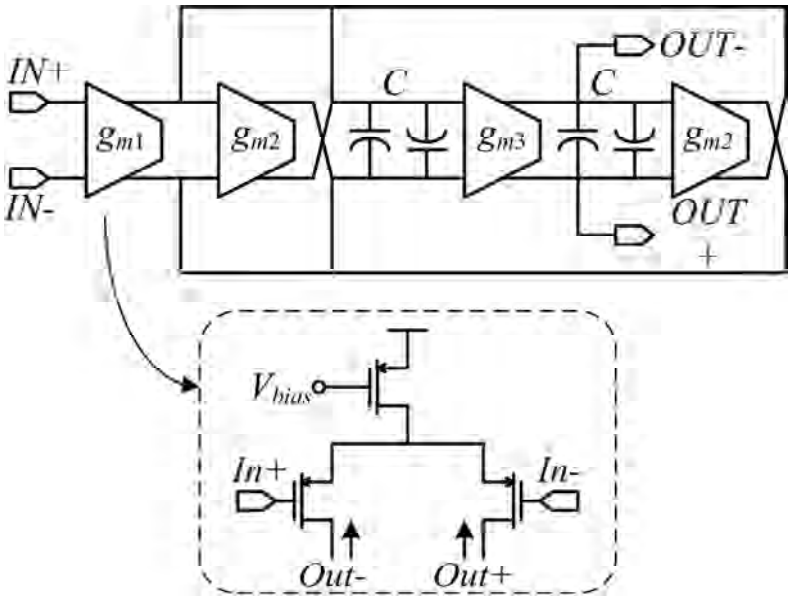


**Fig. 12.** Schematic of the $G_m$-C filters.

The transconductors used PMOS differential pairs to minimize the effects of flicker noise. Given a bandwidth of 1 MHz, a 100 kHz flicker noise corner frequency is sufficiently low as to have a negligible effect on the overall noise performance. Note that due to the 1/*f* nature of flicker noise, the intergrated flicker noise over any frequency decade is equal. If the flicker noise corner frequency is 100 kHz, then the flicker noise contribution from 100 kHz to 1 MHz is insignificant compared to the thermal noise contribution. This implies the same for the flicker noise contribution between 10 kHz and 100 kHz. Any flicker noise below that frequency can be removed

by some form of high-pass filtering which is a standard feature of several IEEE 802.15.4 compatible receivers, and is mainly used to remove DC offset [1], [5].

Given only a 1-V power supply, the common-mode voltage of the IF section was selected to be 0.3 V. Gain compression in the receiver is dealt with by varying the gain of the LNA, and it should be noted that the IEEE 802.15.4 standard does not specify any large blocking signals which could otherwise desensitize the receiver. Nevertheless, any blocker sufficiently removed from the desired channel would be suppressed by the passive filtering at the mixer output pole.

## 4 Measurement Results

The design in Fig. 5 was implemented in a 0.18-μm RFCMOS process with 1 poly layer and 6 metal layers. The aluminum top metal is 2.52 μm thick allowing for sufficiently high-Q (around 8) on-chip inductors. The process also features metal-insulator-metal (MIM) capacitors. A micrograph of the proposed receiver is shown in Fig. 13. The chip was characterized using on-wafer probing. A 10-pin probe was used at the bottom part of the chip to provide the biasing, control signals and the clock signals. The LO was provided at the top of the chip via a ground-signal-signal-ground (GSSG) probe. At the low-frequency outputs, buffers were used to drive the 50-Ω instrumentation. The entire chip measures 1.5 mm by 1.5 mm, but less than half of that is used for the receiver design. Simple flash ADCs were used to convert the off-chip analog control signals into on-chip digital ones. These were used to control the receiver's gain-state, to initiate the calibration sequence, and to provide one-time tuning of the frequency selective networks. These ADCs are only for measurement purposes and in more complete works [1], a serial-peripheral interface (SPI) is commonly used.

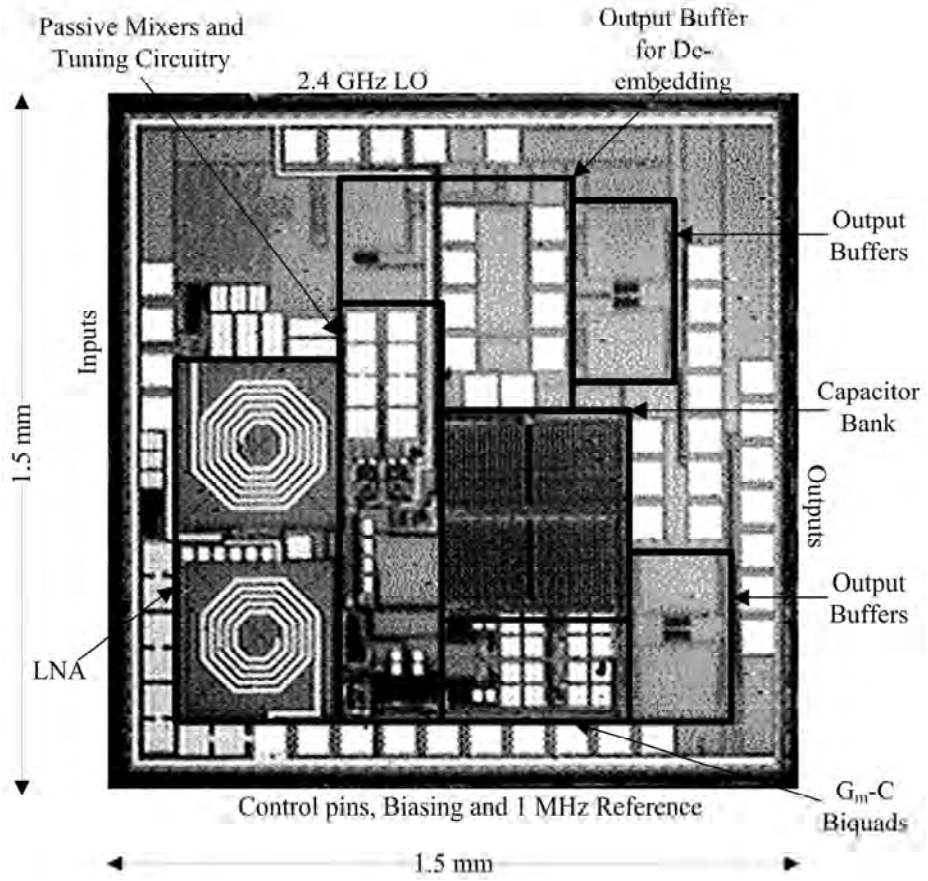


**Fig. 13.** Chip micrograph with labels.

### 4.1 Measured Performance

Measured performance of the LNA was presented in Section III. The performance of the calibration loop is shown in Fig. 14. As mentioned in Section III.B, after a fixed amount of time (no more than 6.4 ms), the loop settles to its final state. For these measurements, the calibration sequence was manually initiated and stopped. From Fig. 14, before calibration, the passive mixer output pole frequency was around 500 kHz, while after calibration the pole frequency was 900 kHz. The 10 % error in the calibrated frequency may have been due to a mismatch in the resistor sizes in the 3-dB attenuator (see Fig. 10), or possibly due to a somewhat noisy power supply. This requires further investigation, however the basic principle of the calibration loop is verified.

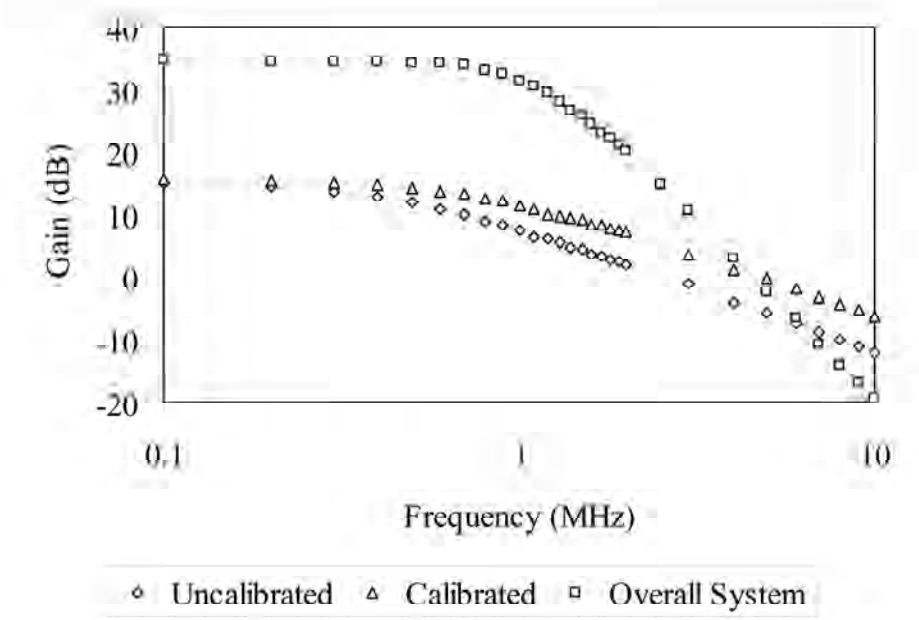


**Fig. 14** Measured calibration loop performance.

The overall single sideband (SSB) NF of the receiver is shown in Fig. 15. The NF was measured using the gain method. In this method, the total output noise, $N_{out}$, and the conversion gain, $G_{conv}$, are measured, allowing the overall NF to be calculated using the following formula,

$$NF = N_{out} - [10\log(kT\Delta f) + G_{conv}] \quad (7)$$

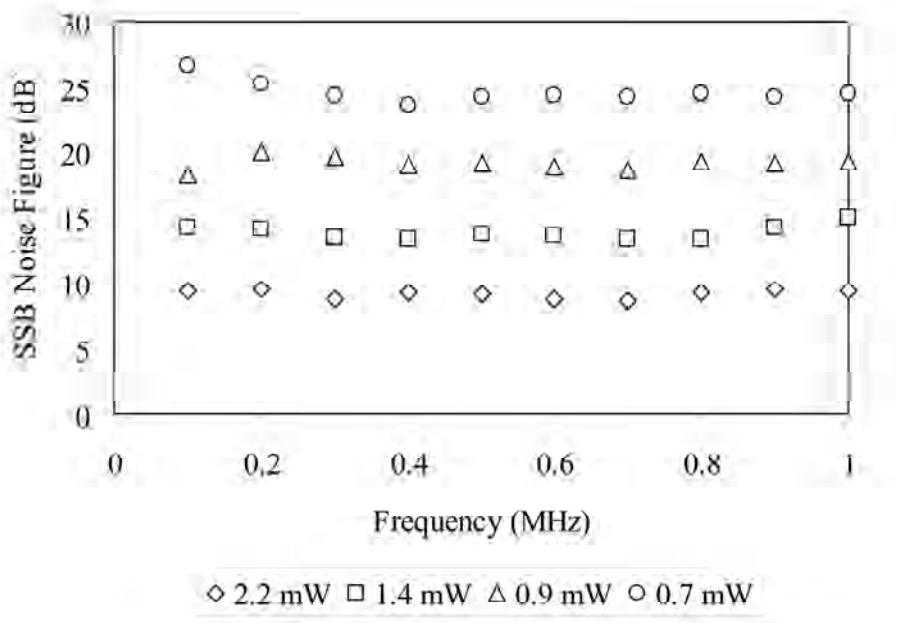


**Fig. 15.** Measured *NF* of the receiver.

When compared to other works, the DSB NF should be estimated from the SSB NF. NF is calculated as the ratio of the total input referred noise to the source noise. Defining $LNA_{NF}$, $SSB_{NF}$, and $DSB_{NF}$ as the LNA NF, the receiver SSB NF, and the receiver DSB NF, and $N_S$, $LNA_{IRN}$, and $MixCSF_{IRN}$, as the source noise, the LNA input-referred-noise, and the Mixer plus CSF input-referred-noise (the RF input) respectively, we can approximate $DSB_{NF}$ using the following formulae.

$$LNA_{NF} = N_S^{-1}(N_S + LNA_{IRN}) \quad (\mathbf{8})$$

$$SSB_{NF} = N_S^{-1}[2(N_S + LNA_{IRN}) + MixCSF_{IRN}] \quad (\mathbf{9})$$

$$DSB_{NF} = N_S^{-1}[N_S + LNA_{IRN} + MixCSF_{IRN}] = SSB_{NF} - LNA_{NF} \quad (\mathbf{10})$$

Therefore, for comparison purposes, the DSB NF is 6.3 dB at the highest power state.

The overall receiver $IIP_3$ was measured using a two-tone test with the first tone at 5.0 MHz offset from the LO and the second tone 10.5 MHz offset from the LO to create a third-order intermodulation product at 0.5 MHz. The overall $IIP_3$ versus power state is shown in Fig. 16. In the worst case, the $IIP_3$ is -17 dBm which is well within specifications even for the more stringent interferer powers (Section 2.2).

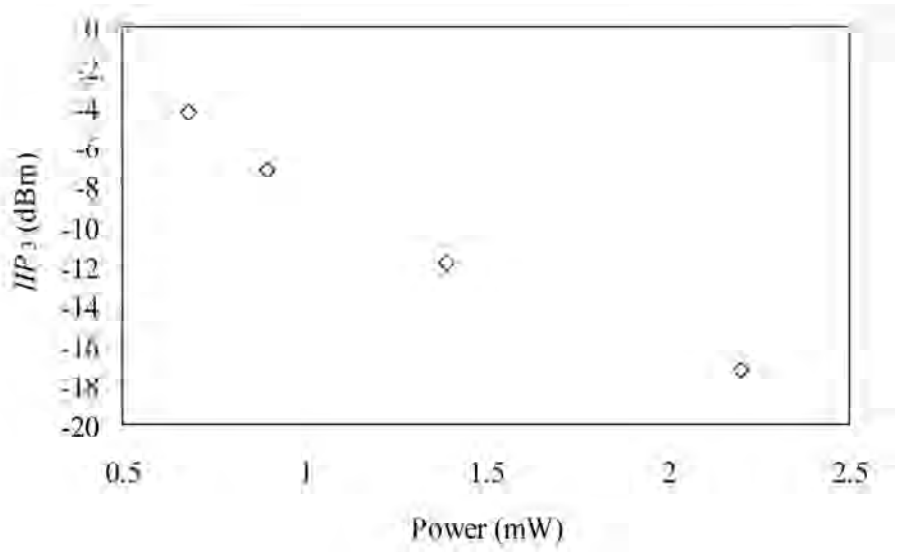


**Fig. 16.** Measured $IIP_3$ of the overall receiver.

### 4.2 Comparison

The proposed receiver uses a combination of a tuned passive mixer output pole, and energy-aware control to achieve low power consumption without sacrificing performance. Table 2 summarizes the receiver's performance and compares it with several recent works. Using the proposed method, the IF power consumption was just 0.45 mW and the total power consumption was 2.2 mW in the highest power state.

**Table 2.** Comparison with Recent Literature

| Reference | This Work | | | | [1] | [2] | [3] | [4] |
|---|---|---|---|---|---|---|---|---|
| Band (GHz) | 2.4 | | | | | | | |
| Process (nm)[A] | 180 | | | | | | 130 | 90 |
| IF (MHz) | 0 | | | | 2.0 | 10.0 | - | 6.0 |
| Voltage (V) | 1.0 | | | | 1.8 | 1.2 | 0.4 | 1.35 |
| Power (mW) | 2.2 | 1.4 | 0.9 | 0.7 | 10 | 1.4 | 0.75 | 5.4 |
| *NF* (dB) | 5.6 | 10.4 | 15.6 | 21.2 | 5.7 | 5.0 | 5.1 | 6.0 |
| $IIP_3$ (dBm) | -17 | -12 | -7 | -4 | -16 | -37 | -7.5 | -12 |

[A] CMOS only

The table of comparison deserves some discussion before drawing any final conclusions. Firstly, the design in [1] was a very complete design including a full transceiver and supply regulation with a wide supply voltage compatibility range. Considering all of the auxiliary circuitry such as biasing circuits, it is difficult to gauge the performance in relation to the power consumption of the full design. We have mentioned the low power performance of [2], and [3] in the introduction, and have also discussed their short-comings.

Overall, the *NF* achieved in this work is comparable to state-of-the art designs, while still offering impedance matching at the input (impedance matching is not used in [3] and [4]). The power consumption is controllable from 2.2 mW down to 0.7 mW. This is comparable with the state-of-the-art for this application, and further improvement may not be meaningful given the power consumption requirements of other blocks such as the frequency synthesizer; to our knowledge, the lowest power 2.4-GHz frequency synthesizer for IEEE 802.15.4 standard applications uses 2.4 mW [25]. The $IIP_3$ in the proposed design is also well within specifications, despite the use of an un-linearized IF section, and is comparable with recent literature.

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## References

1. W. Kluge, F. Poegel, H. Roller, M. Lange, T. Ferchland, L. Dathe, D. Eggert, "A Fully Integrated 2.4-GHz IEEE 802.15.4-Compliant Transceiver for ZigBeeTM Applications", IEEE Journal of Solid-State Circuits, vol. 41, issue 12, pp. 2767-2775, Dec, 2006.
2. B. G. Perumana, R. Mukhopadhyay, S. Chakraborty, C.-H. Lee, and J. Laskar, "A low-power fully monolithic subthreshold CMOS receiver with integrated LO generation for 2.4 GHz wireless PAN applications," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2229–2238, Oct. 2008.
3. B. W. Cook, A. Berny, A. Molnar, S. Lanzisera, K. S. J. Pister, "Low-Power 2.4-GHz Transceiver With Passive RX Front-End and 400-mV Supply", *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, Dec. 2006, pp. 2757-2766.
4. M. Camus, B. Butaye, L. Garcia, M. Sié, B. Pellat, T. Parra, "A 5.4 mW/0.07 mm2 2.4 GHz Front end Receiver in 90 nm CMOS for IEEE 802.15.4 WPAN Standard", *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1372-1383, June 2008.
5. T –K. Nguyen, N –J. Oh, V.–H. Hoang, S. –G. Lee, "A Low-Power CMOS Direct Conversion Receiver With 3-dB NF and 30-kHz Flicker Noise Corner for 915-MHz Band IEEE 802.15.4 ZigBee standard", *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 2, pp. 735-741, Feb, 2006.

6. I. Nam, K. Choi, J. Lee, H. –K. Cha, B. –I. Seo, K. Kwon, K. Lee, "A 2.4-GHz Low-Power Low-IF Receiver and Direct-Conversion Transmitter in 0.18-μm CMOS for IEEE 802.15.4 WPAN Applications", *IEEE Transactions on Microwave Theory and Techniques*, Vo. 55, No. 4, pp. 682- 689, April, 2007
7. A. V. DO, C. C. Boon, M. A. Do, K. S. Yeo, A. Cabuk, "An Energy-Aware CMOS Receiver Front End for Low Power 2.4-GHz Applications", *IEEE Transactions on Circuits and Systems – I: Regular Papers*, vol. 57, no. 10, pp. 2675-2684, Oct. 2010.
8. C.C. Boon, M.A. Do, K.S. Yeo and J.G. Ma, "Fully Integrated CMOS Fractional-N Frequency Divider for Wide-Band Mobile Applications with Spurs Reduction", *IEEE Transaction on Circuits and Systems- I,* Vol 52, No. 6, pp. 1042-1048, Jun. 2005.
9. A. Meaamar, C. C. Boon, K.-S. Yeo, M. A. Do, "A Wideband Low Power Low-Noise Amplifier in CMOS Technology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.57, no.4, pp.773-782, April 2010.
10. IEEE 802.15.4 Standard For Local and Metropolitan Area Networks, 2003.
11. B. W. Cook, "Low Energy RF Transceiver Design", PhD Thesis, University of California at Berkeley, May 16th, 2007.
12. A. V. Do, C. C. Boon, M. A. Do, K. S. Yeo, A. Cabuk, "A 1-V CMOS Ultralow-Power Receiver Front End for the IEEE 802.15.4 Standard Using Tuned Passive Mixer Output Pole", *Accepted for Presentation at the IFIP/IEEE International Conference on Very Large Scale Integration*, Sept 27-29, 2010.
13. P. Gorday, "802.15.4 Multipath", Internet: https://mentor.ieee.org/802.15/file/04/15-04-0337-00-004b-802-15-4-multipath.ppt, July 2004 [Oct. 2009].
14. T –K. Nguyen, V. Krizhanovskii, J. Lee, N –J. Oh, S. –K. Han, S. –G. Lee, N. –S. Kim, C. –S. Pyo, "A Low-Power RF Direct-Conversion Receiver/Transmitter for 2.4-GHz-Band IEEE 802.15.4 Standard in 0.18-μm CMOS Technology", *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 12, pp. 4062-4071, Dec. 2006.
15. J. Crols, M. S. J. Steyaert, "Low-IF Topologies for High-Peformance Analog Front Ends of Fully Integrated Receivers", *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 45, no. 3, March 1998, pp. 269-282.
16. R. D. Middlebrook, "The general feedback theorem: a final solution for feedback systems", *IEEE Microwave Magazine*, vol. 7, no. 2, 2006, pp. 50-63.
17. W. Sansen, "Distortion in Elementary Transistor Circuits", *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing*, vol. 46, no.3, March 1999, pp. 315-325.
18. A. A. Abidi, "General Relations Between IP2, IP3, and Offsets in Differential Circuits and the Effects of Feedback", *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 5, May 2003, pp. 1610-1612.
19. D. A. Johns, K. Martin, "Continuous-Time Filters", *Analog Integrated Circuit Design*, John Wiley and Sons, 1997, Ch. 15, Section 15.2-15.5, pp. 584-620.
20. A. V. Do, C. C. Boon, M. A. Do, K. S. Yeo, A. Cabuk, "A Subthreshold Low-Noise Amplifier Optimized for Ultra-Low-Power Applications in the ISM Band", *IEEE Trans. on Microwave Theory and Tech*., Vol. 56, No. 2, pp. 286-292, February 2008.
21. R. Ludwig, P. Bretchko, "RF Transistor Amplifier Designs", *RF Circuit Design*, Upper Saddle River, NJ/USA: Prentice Hall PTR, 2000, Chapter 9, Section 9.2-9,4, pp. 465-502.
22. T. H. Lee, "LNA Design", *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd Ed., Cambridge, UK: Cambridge University Press, 2004, Chapter 12, pp. 365-380.
23. K. Kurokawa, "Power Waves and the Scattering Matrix", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 13, no. 2, March 1965.
24. D. A. Johns, K. Martin, "Continuous-Time Filters", *Analog Integrated Circuit Design*, 111 River Street, Hoboken, NJ 07030, John Wiley and Sons, Inc, 1997, Chapter 15, pp. 574-647.
25. C. Bernier, F. Hameau, G. Billiot, E. de Foucauld, S. Robinet, J. Durupt, F. Dehmas, E. Mercier, P. Vincent, L. Ouvry, D. Lattard, M. Gary, C. Bour, J. Prouvee, S. Dumas, "An

ultra low power 130nm CMOS direct conversion transceiver for IEEE802.15.4", *IEEE Radio Frequency Integrated Circuits Symposium*, April & June 2008, pp. 273-276.