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# A 1.8-V 3.6-mW 2.4-GHz fully integrated CMOS Frequency Synthesizer for the IEEE 802.15.4

M.Vamshi Krishna<sup>1</sup>, Xuan Jie<sup>1</sup>, Anh Manh Do<sup>1</sup>, Chirn Chye Boon<sup>1</sup>, Kiat Seng Yeo<sup>1</sup>, Aaron V. T. Do<sup>2</sup>

<sup>1</sup> Nanyang Technological University, Singapore 639798  
{mkvamshi, xiej0005, emado, eccboon, eksyeo}@ntu.edu.sg

<sup>2</sup> Marvell Asia Pte. Ltd., Singapore 534158  
{doaaron}@marvell.com

**Abstract.** This paper presents a low power 2.4-GHz fully integrated 1 MHz resolution IEEE 802.15.4 frequency synthesizer designed using 0.18 $\mu$ m CMOS technology. An integer-N fully programmable divider employs a novel True-single-phase-clock (TSPC) 47/48 prescaler and a 6 bit P and S counters to provide the 1 MHz output with nearly 45% duty cycle. The PLL uses a series quadrature voltage controlled oscillator (S-QVCO) to generate quadrature signals. The PLL consumes 3.6 mW of power at 1.8 V supply with the fully programmable divider consuming only 600  $\mu$ W. The S-QVCO consumes 2.8 mW of power with a phase noise of -122dBc/Hz at 1 MHz offset.

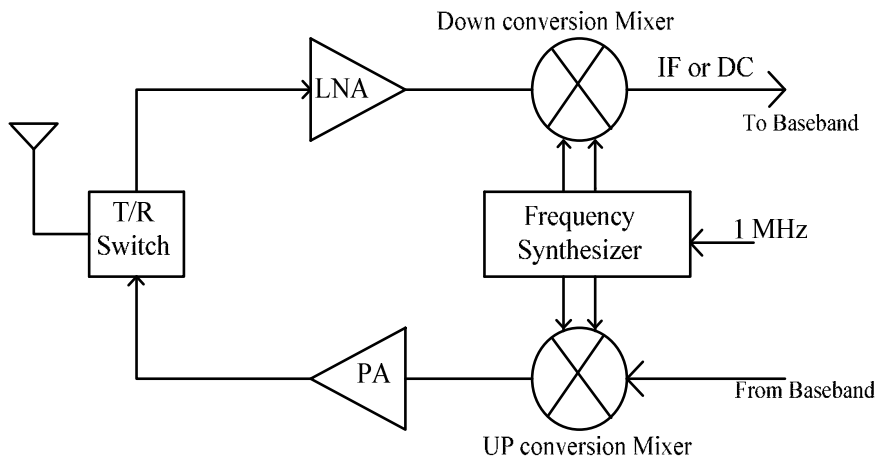
**Keywords:** D flip-flop (DFF), Frequency synthesizer, Phase-locked loop (PLL), Voltage controlled oscillator (VCO), Dual-modulus prescaler.

## 1 Introduction

Most of the wireless communication standards prior to IEEE 802.15.4/Zigbee were tailored towards high data rate and multimedia friendly applications. The need for low data rate and low power wireless solutions with emphasis on sensor network applications resulted in the development of IEEE 802.15.4 standard. The recent development and advanced scaling CMOS technologies have made it more attractive to implement a single chip CMOS wireless transceiver featuring both high level of integration and low power consumption [1].

The higher power consumption in the frequency synthesizer is mainly due to the VCO and the first stage divider which is driven by the VCO. The 2.4 GHz synthesizer reported in [2] with a frequency resolution of 5 MHz consumes a power of 7.85 mW at 1.8 V power supply in 0.18  $\mu$ m CMOS technology. Here, the first stage divider is designed using current-mode logic (CML) [6] which consumes a large amount of power. The synthesizer reported in [3] consumes 2.4 mW at 1.2 V supply in 0.13  $\mu$ m CMOS technology. It uses a 16/17 dynamic logic prescaler as first stage divider which consumes only 176  $\mu$ A at 2.5 GHz and the complete divider is designed with 5

MHz resolution. Here, the VCO provides only differential phase signals. The frequency synthesizer reported in [4] proposes a new spur suppression technique, but consumes a power of 18 mW. Reference [5] provides a synthesizer for IEEE 802.15.4/Zigbee applications consumes a power of 15 mW in 0.18  $\mu\text{m}$  CMOS technology. For the popular transceiver's architecture shown in Fig.1 with direct up-conversion for the TX and low IF down-conversion, the synthesizer needs to generate LO outputs having both I-Q outputs. In this article, an integer-N, low power 2.4 GHz frequency synthesizer with quadrature signal generation is proposed. In this design, the fully programmable 1 MHz resolution divider is implemented using dynamic logic circuits.



**Fig. 1.** Transceiver architecture.

## 2 System Specification

### 2.1 Frequency Synthesis

The IEEE 802.15.4 standard has 16 channels, spaced at 5 MHz apart over the frequency range from 2405 MHz to 2480 MHz. The synthesizer needs to synthesize 16 channel selection frequencies with 40-ppm frequency accuracy. If direct conversion is used in both the transmitter and receiver, then the 16 channel selection frequencies would be from 2405 MHz to 2480 MHz in steps of 5 MHz. If a low IF architecture is used for the RX, then the local oscillator frequencies could be different from the channel frequencies for both the transmitter and receiver. In order to have more flexibility to accommodate channel selections for both kind of architecture, the resolution of the divider and reference frequency chosen is 1 MHz which gives a

resolution of 1 MHz to the channel selection frequency. For example, if the IF frequency is chosen to be 2 MHz, the divider is programmed to have the local oscillator frequencies equal to 2403, 2408....2478 MHz or 2407, 2412....2482 MHz. For the IEEE 802.15.4 standard, the channel bandwidth is 2 MHz.

## 2.2 Phase Noise

According to [7], the required phase noise at a frequency offset determined by the frequency offset of  $P_{int}$  can be calculated by,

$$PN(dBc/Hz) = (P_{sig} - P_{int}) - SNR_{req} - 10 \log(BW) \quad (1)$$

The system simulations in [8] shows that  $SNR_{out}$  should be at least 14 dB. Based on this value, from (1) the required phase noise at 5 MHz offset and 10 MHz offset would be -77dBc/Hz, and -107dBc/Hz respectively. Assuming a margin of 10 dB due to non-idealities of the system, the required phase noise at 5 MHz offset and 10 MHz offset is -87dBc/Hz and -117dBc/Hz respectively.

## 2.3 Spur Rejection

The IEEE 802.15.4 standard specifies the adjacent channel interference of +0 dB (relative to the carrier) at an offset of 5 MHz. The spur suppression requirement for the synthesizer can be calculated by [5]

$$PN(dBc/Hz) = (P_{sig} - P_{int}) - SNR_{req} - 10 \log(BW) \quad (2)$$

For the IEEE 802.15.4 standard, the required spur suppression is -14 dBc at 5 MHz offset, and -44 dBc at 10 MHz offset.

## 2.4 Settling time

The IEEE 802.15.4 supports a data rate of 250 Kbps with each symbol consisting of 4-bits and a symbol rate of 62.5 Ksymbols/sec. The maximum Tx-Rx turn-around time is 12 symbol periods, which is equivalent to 192 us. Thus the worst case settling time of the synthesizer is estimated to be 192 us.

The synthesizer is designed to meet all the above specifications with a supply voltage of 1.8 V and low power consumption with on-chip filter in RF CMOS 01.8um technology.

### 3 Architecture of the implemented frequency synthesizer

The synthesizer is designed to generate quadrature differential output signals of 1 MHz resolution over the 2.4 GHz ISM band. The architecture of the frequency synthesizer is chosen to be a type-2, fourth order loop using a charge pump as shown in Fig.2. The synthesizer consists of a phase-frequency detector (PFD), a charge pump (CP), a series Q-VCO, a 3<sup>rd</sup> order loop filter and a fully programmable 1 MHz resolution divider.

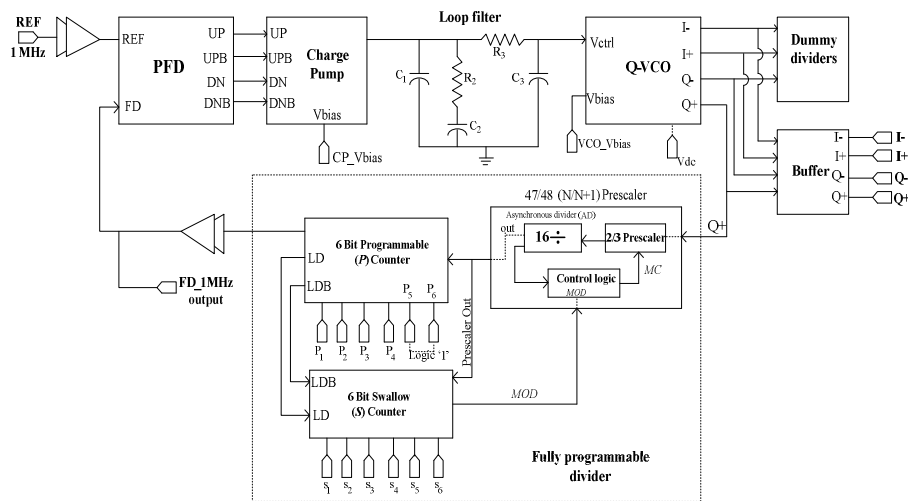


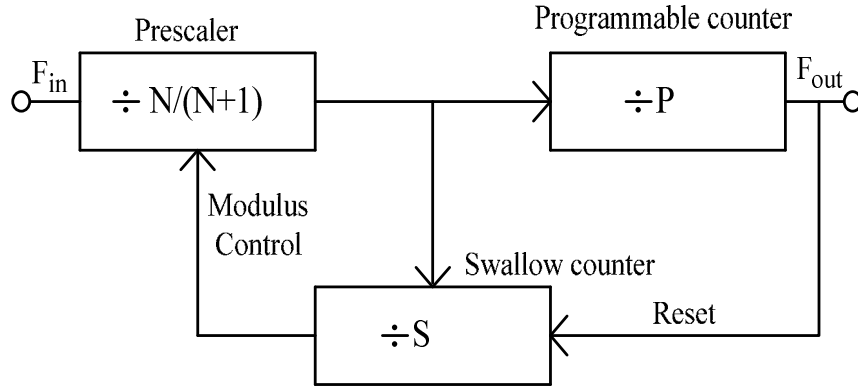
Fig. 2. System Level architecture of the implemented 2.4 GHz frequency synthesizer

Compared to lower order loop, the additional poles provide higher spurious filtering, thus reducing the spurs generated by the input reference without decreasing the loop bandwidth or increasing the settling time. Since the divider is based on dynamic logic circuits whose input is single-phase, only one of the outputs of the quad-phase VCO is applied to the divider while the remaining 3 outputs of the VCO are connected to the dummy divider loads. Based on the optimization of the loop parameters, the loop bandwidth is chosen to at 45 KHz as described in section 6.

### 4 Fully Programmable 1 MHz Resolution Divider

The fully programmable 1 MHz resolution divider used in this design is based on the pulse-swallow topology shown in Fig.3. The pulse-swallow frequency divider consists of a dual-modulus prescaler (DMP), a programmable (P) counter and a swallow (S) counter. The dual-modulus prescaler is based on both synchronous and asynchronous divider which scales the input frequency to a lower frequency to ease the complexity of asynchronous presettable modulo-P and modulo-S counters. In this

technique,  $S$  input pulses are swallowed in the preceding arrangement such that the output period becomes longer by  $S$  reference periods.



**Fig. 3.** Pulse-swallow frequency divider

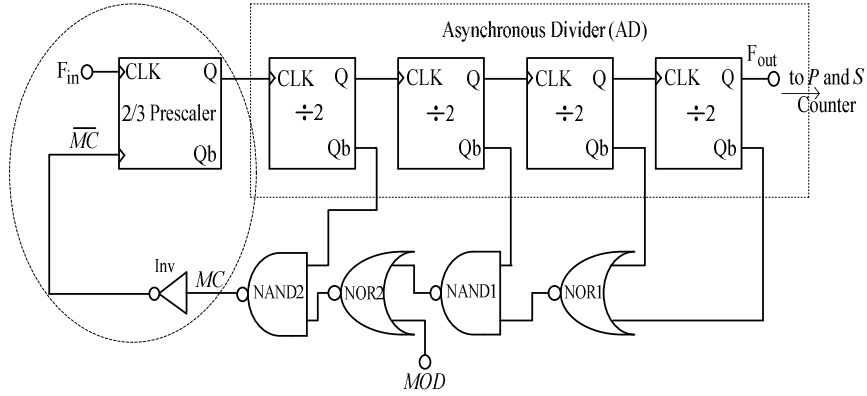
In the initial state, the modulus control ( $MC$ ) signal remains at logic '0' and allows the DMP to operate in the divide-by- $(N+1)$  mode and the programmable  $P$ -counter and swallow  $S$  counter are loaded to their initial states. Since  $P > S$ , the  $S$ -counter reaches the final state earlier than  $P$ -counter and the end-of-count logic of the  $S$ -counter changes the  $MC$  to logic '1' allowing the DMP to switch to divide-by- $N$  mode where the  $P$ -counter counts the remaining  $(P-S)$  input periods of ' $N$ '. Thus the total division ratio is given by

$$F_{out} = ((N+1)S + N(P-S))F_{in} = (NP + S)F_{in} \quad (3)$$

In this design, the fully programmable divider is constructed using a TSPC [9] 47/48 ( $N/N+1$ ) dual-modulus prescaler, a 6-bit programmable  $P$ -counter and a 6-bit swallow  $S$ -counter.

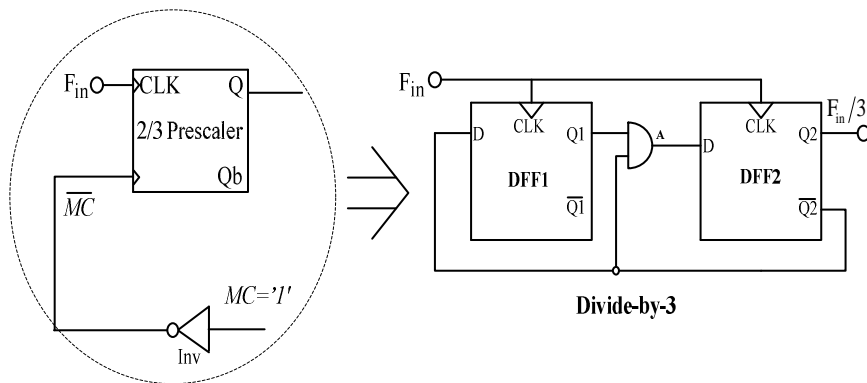
#### 4.1 A TSPC 47/48 Dual-modulus prescaler

The proposed 47/48 prescaler circuit as shown in Fig.4 is similar to the 32/33 prescaler reported in [10] except for an additional inverter which is added between the output of the NAND2 gate and the control signal ( $MC$ ) input of the 2/3 prescaler. The 47/48 prescaler consists of 2/3 prescaler [10], four asynchronous divide-by-2 circuits and additional logic gates to control the division ratio between 47 and 48. When  $MC = '0'$ , the 2/3 prescaler of the 32/33 prescaler in [10] operates in divide-by-3 mode whereas the 2/3 prescaler in the proposed 47/48 prescaler operates in divide-by-2 mode. Thus the inverter swaps the operation modes of the 2/3 prescaler.



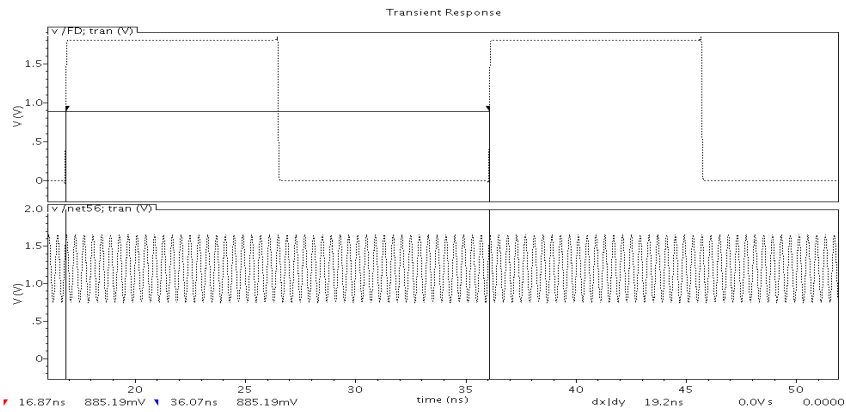
**Fig. 4.** Proposed TSPC 47/48 prescaler

**Divide-by-48 operation ( $MOD='1'$ ):** When the control signal  $MOD$  is '1', the output of NOR2 in Fig.4 always remains at logic '0' and forces the output of NAND2 to logic '1' irrespective of data on  $Q_{b1}$ . Since  $MC$  is always equal to logic '1' ( $\overline{MC} = '0'$ ), the 2/3 prescaler remains in divide-by-3 mode. The equivalent circuit of inverter and the 2/3 prescaler is equal to divide-by-3 counter as shown in Fig.5. Thus the 47/48 prescaler operates in divide-by-48 mode when  $MOD='1'$ . Fig.6 shows the transient simulations of divide-by-48 mode of operation. If we denote the synchronous 2/3 prescaler as  $M/M+1$  and the four asynchronous dividers whose division ratio equal to 16 by 'AD', the division ratio of the 47/48 prescaler in this mode ( $MOD='1'$ ) is given by



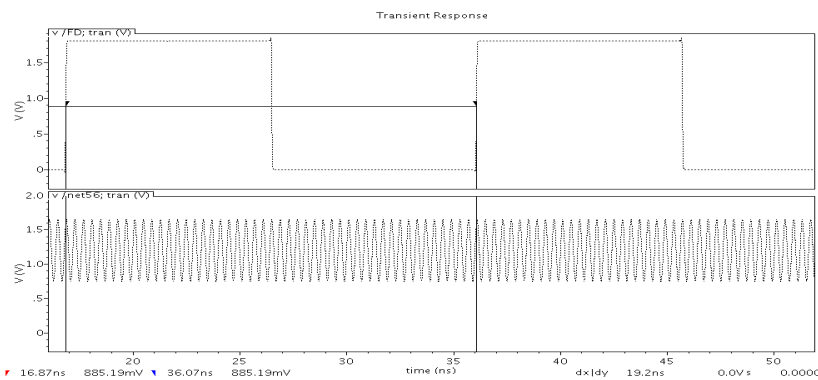
**Fig. 5.** Divide-by-48 mode of operation

$$F_{48} = (AD - \overline{MOD}) \times (M + 1) + \overline{MOD} \times M = (16 - 0) \times (2 + 1) + 0 \times 2 = 48 \quad (4)$$



**Fig. 6.** Transient simulations of divide-by-48 mode of operation

**Divide-by-47 operation ( $MOD='0'$ ):** The proposed 47/48 prescaler operates as divide-by-47 when  $MOD='0'$ . By using the combination of logic NOR and NAND gates, the asynchronous divide-by-16 counter is made to count an extra input clock. In the initial state, the 2/3 prescaler will be in divide-by-3 mode ( $MC='1'$ ) and the asynchronous divide-by-16 starts counting the output pulses of 2/3 prescaler from “0000” to “1111”. When the asynchronous counter value reaches “1110”, the logic signal MC goes low ( $MC='0'$ ) and 2/3 prescaler operates in divide-by-2 mode, where the asynchronous counter counts an extra input clock pulse. During this operation, the 2/3 prescaler operates in the divide-by-3 mode for 45 input clock cycles and in the divide-2 mode for 2 input clock cycles. The division ratio of the 47/48 prescaler in this mode is given by



**Fig. 7.** Transient simulations of divide-by-47 mode of operation

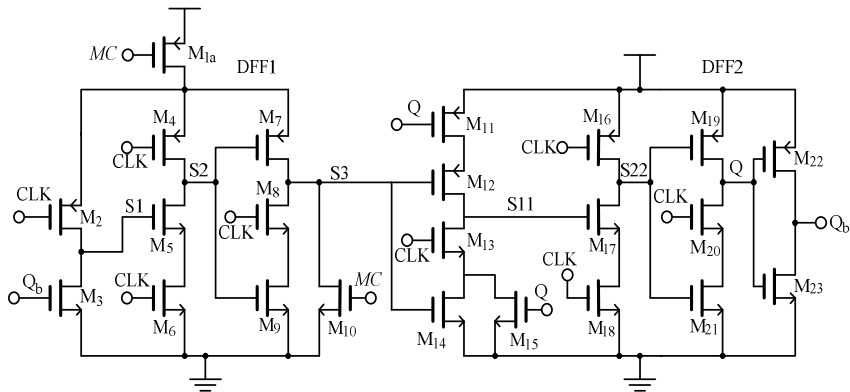
The transient simulation of divide-by-47 mode of operation is shown in Fig.7. The Post layout simulation results shows that the proposed dual modulus 47/48 prescaler



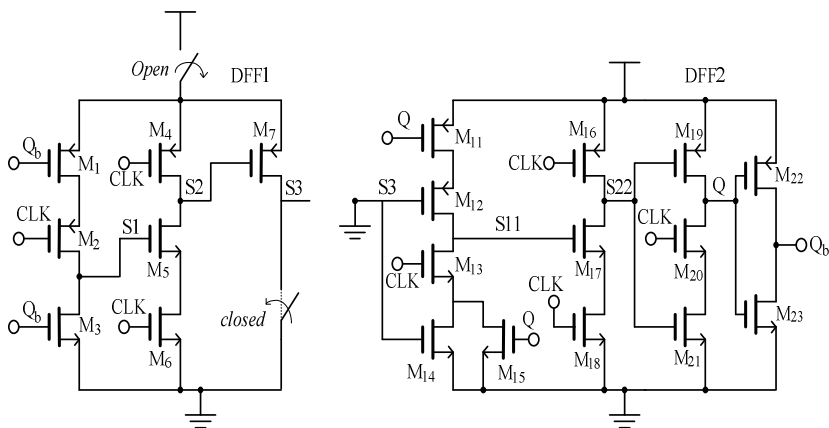
consumes a current of 269.3  $\mu$ A and 262.8  $\mu$ A during the divide-by-47 and divide-by-48 modes respectively and the maximum operating frequency is 4.8 GHz.

#### 4.2 A Low Power TSPC 2/3 Prescaler [10]

Fig.8 shows the ultra-low power TSPC 2/3 prescaler reported in [10]. In this design, an extra PMOS transistor  $M_{1a}$  is connected between the power supply and DFF1 whose input is the controlled by the logic signal  $MC$ . As discussed in the section 3.6.1, during the divide-by-2 operation, one of the input logic signals  $MC$ . During the divide-by-2 operation, one of the inputs of second NOR gate is always zero since transistor  $M_{10}$  blocks the data at the input of DFF1 to propagate to the output node.



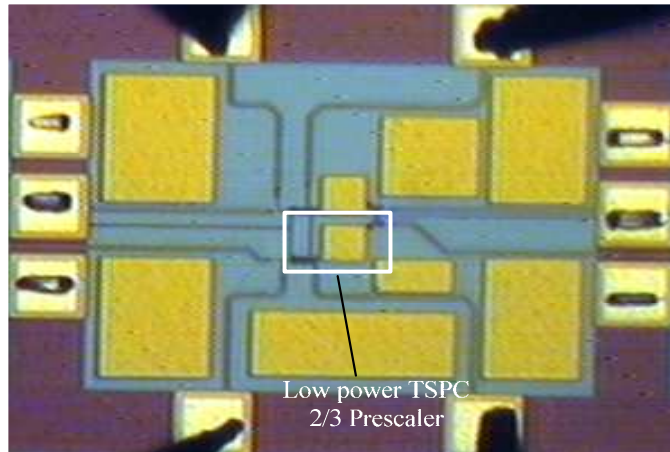
**Fig. 8.** Ultra-low power TSPC 2/3 prescaler [10]



**Fig. 9.** Divide-by-2 operation of the ultra-low power TSPC 2/3 prescaler [10]

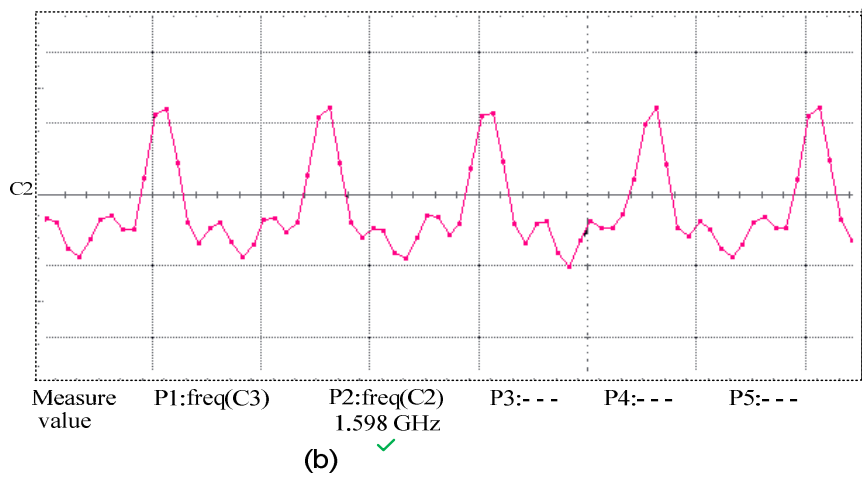
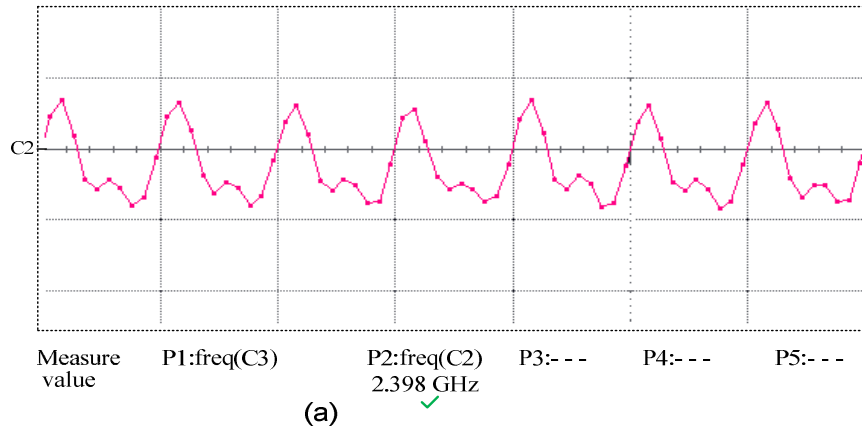
In this design, when the control logic signal  $MC$  is '1' during the divide-by-2 mode, the PMOS transistor  $M_{1a}$  is turned-off and DFF1 is disconnected from the power supply. Fig.9 shows the simplified schematic of the 2/3 prescaler in the divide-by-2 mode of operation. Even though  $M_{10}$  is always turned-on, the source of  $M_7$  is at virtual ground and short-circuit power is completely avoided. Even if the output ' $Q_b$ ' switches continuously, the nodes S1 and S2 and S3 always remain at logic '0' and thus the switching activities are blocked in DFF1 resulting in zero switching power.

The ultra-low power 2/3 prescaler is fabricated using the chartered 1P6M 0.18  $\mu\text{m}$  CMOS process and the PMOS and NMOS transistor sizes are fixed to 3  $\mu\text{m}/0.18 \mu\text{m}$ , 2  $\mu\text{m}/0.18 \mu\text{m}$  respectively. On-wafer measurements are carried out using an 8 inch RF probe station. The input signal for the measurement is provided by the 83650B 10 MHz-50 GHz HP signal generator and the output signals are captured by the Lecroy Wave master 8600A 6G oscilloscope.



**Fig. 10.** Die photograph of the ultra-low power TSPC 2/3 prescaler

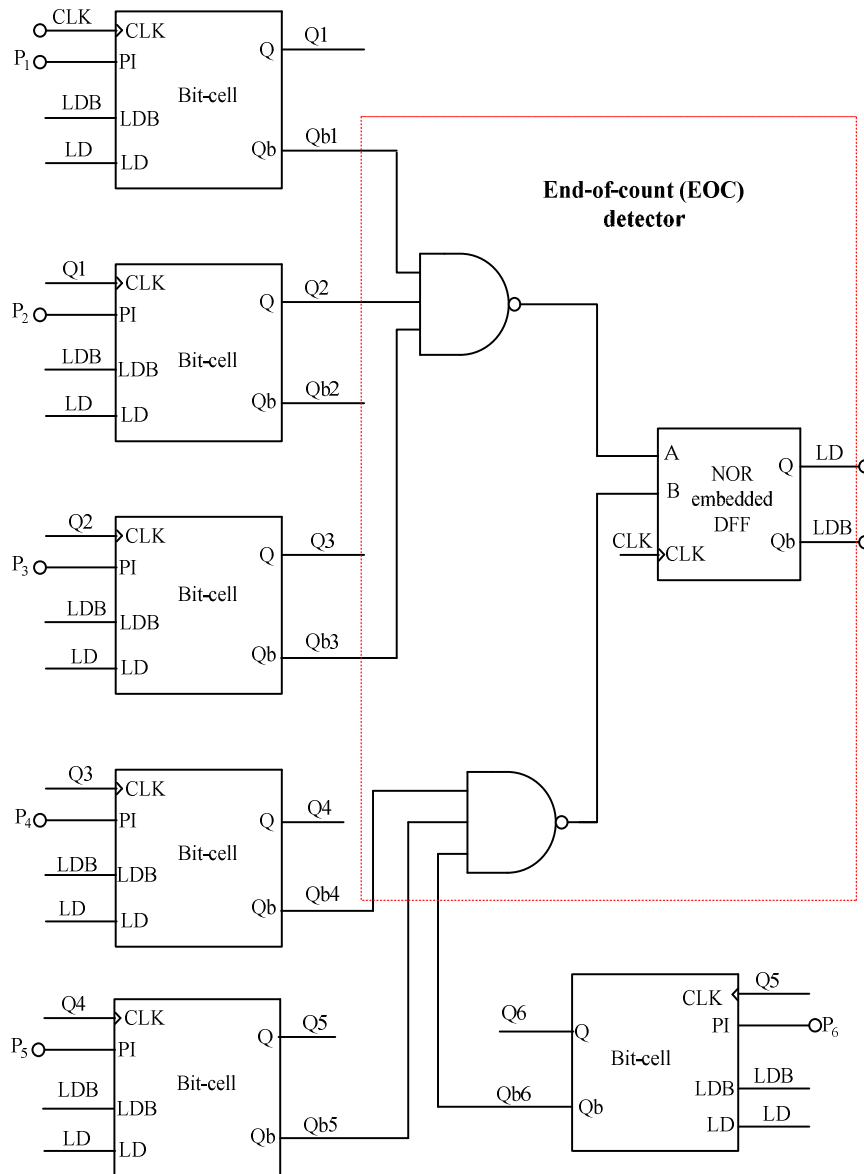
Fig.10 shows the die photograph of ultra-low power TSPC 2/3 prescaler fabricated in Global foundries 0.18 $\mu\text{m}$  CMOS technology. The measured maximum operating frequency of 2/3 prescaler is 4.9 GHz. The power consumption of the 2/3 prescaler during the divide-by-2 and divide-by-3 modes is 0.6 mW, 0.922 mW respectively, when the input frequency is 4.8 GHz. Fig.11 shows the measured output waveforms of the 2/3 prescaler at 4.8 GHz during the divide-by-2 and divide-by-3 modes of operation.



**Fig. 11.** Measured waveforms of the proposed prescaler at 4.8 GHz (a) divide-by-2 mode, (b) divide-by-3 mode

## 4.2 Programmable P-counter

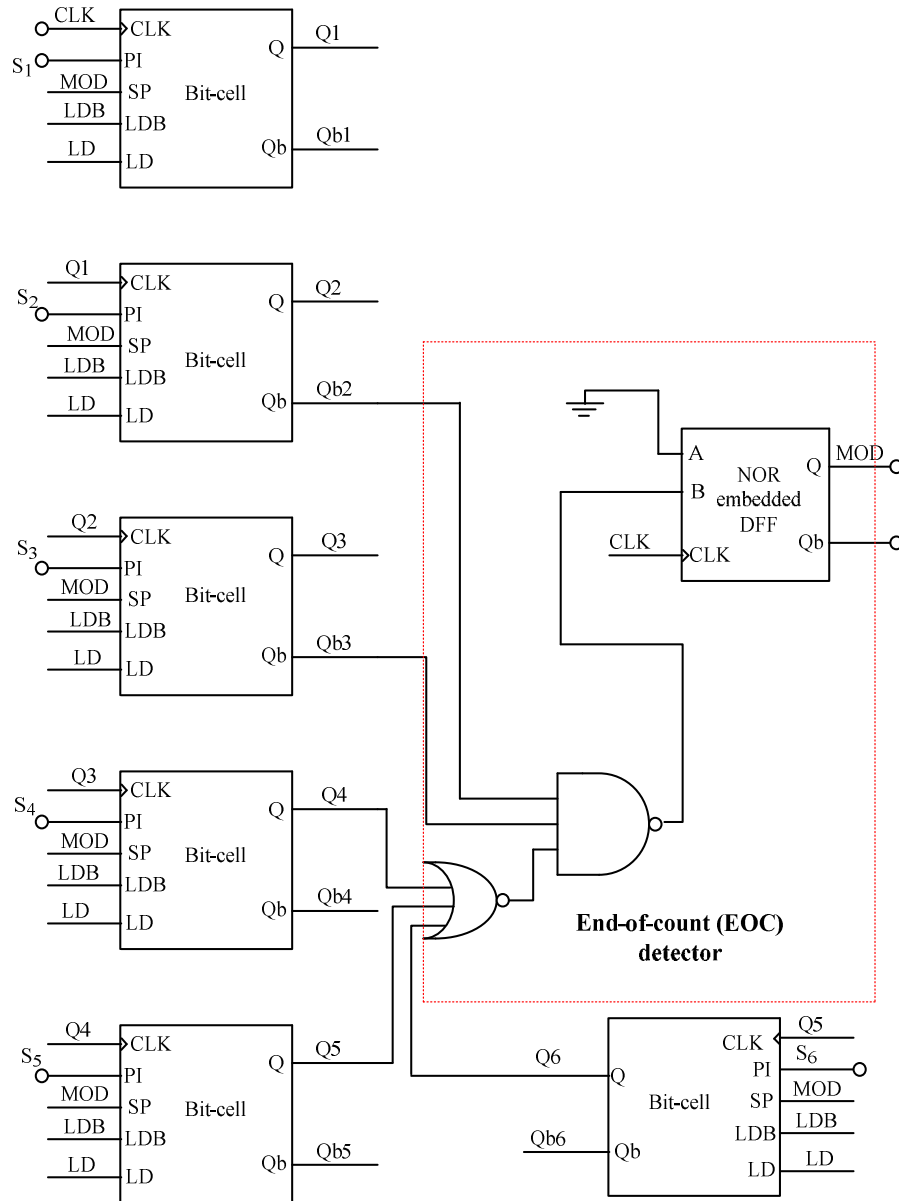
The 6 bit programmable P-counter used in the design of fully programmable divider is shown in Fig. 12. It consists of proposed 6 asynchronous reloadable bit-cells [11], a NOR-embedded DFF [12] and an end-of-count (EOC) detector with reload circuit. Here, bit  $P_6$  and  $P_5$  are always at logic '1' and bit  $P_4$  at logic '0' to have a programmable values of 51 and 52. By choosing a fixed value of 51 and 52, the swallow S-counter is programmed in steps of one-bit to provide a division ratio from 2400 to 2484 with 1 MHz resolution.



**Fig. 12.** A 6-bit Programmable P-counter with EOC logic circuit

In this design, the state  $Q_6Q_5Q_4Q_3Q_2Q_1 = "000010"$  is detected by the EOC logic circuit. As soon as the state "000010" is reached, the signals A and B go low after a delay introduced by the logic gates which is assumed to be less than half of the input clock cycle. However, the output of the embedded-NOR gate is latched to output only at the next rising edge of clock after the state "000001" is reached. This output "LD" signal will initialize the P and S counters and the counting process continues. If the

state “000001” is chosen to detect, then it results in the undercounting due to the delays.

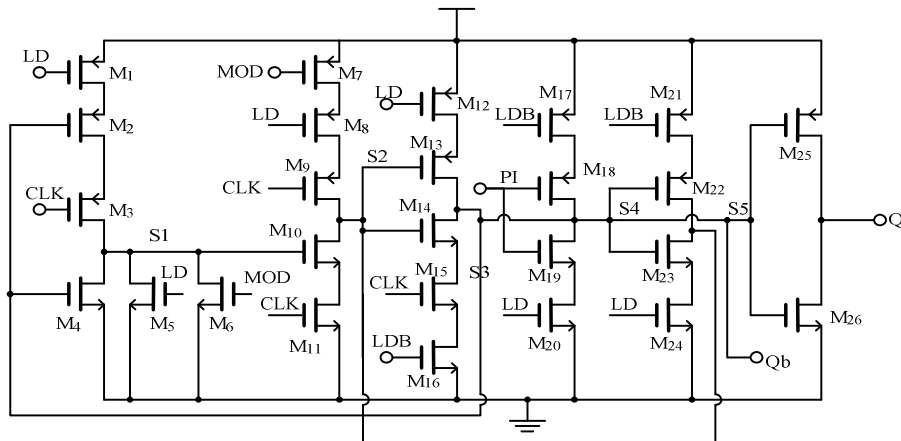


**Fig. 13.** A 6-bit Swallow S-counter with EOC logic circuit

## 4.2 Swallow S-counter

The 6 bit swallow S-counter used in the fully programmable divider is shown in Fig. 13. It consists of proposed 6 asynchronous reloadable bit-cells, a NOR-embedded DFF [12] and an end-of-count (EOC) detector with reload circuit. Here the state  $Q_6Q_5Q_4Q_3Q_2=$ “000000” is detected by the EOC logic circuit. The S-counter in this programmable divider can be programmed from 0-47 in steps of 1 for a fixed value of the P-counter.

Since the counter is asynchronous and based on the ring topology, the complementary output of the first DFF is fed as the clock signal to the input of next flip-flop. In the initial state, all the reloadable FF's are loaded by the programmable value set by pins  $S_1$ - $S_6$ . In the S-counter all states from 0-47 are usable and adjustable in steps of 1 to obtain a resolution of 1MHz. Once the counter is triggered by the output of the prescaler, the S-counter starts down counting till the final state is reached, which is detected by the EOC logic circuit and the MOD signal goes high until the P-counter finishes its counting. Since the value of ‘P’ is always greater than value of ‘S’ in pulse-swallow divider, the S-counter remains idle for a period of  $(P-S)*N$  clock cycles.



**Fig. 14.** Reloadable TSPC DFF for S-counter

The signal MOD goes high only when the outputs of all the reloadable DFF in the S-counter go low and remain in the same state until the LD signal from the P-counter goes high. The state where MOD remains at logic high indicate the S-counter has finished counting. The S-counter cannot use the EOC logic circuit of the P-counter since MOD has to remain high until the P-counter reaches the state “000010” when the LD signal goes high for one clock cycle. Moreover in the S-counter, all zero state is detected by EOC circuit unlike in the P-counter.

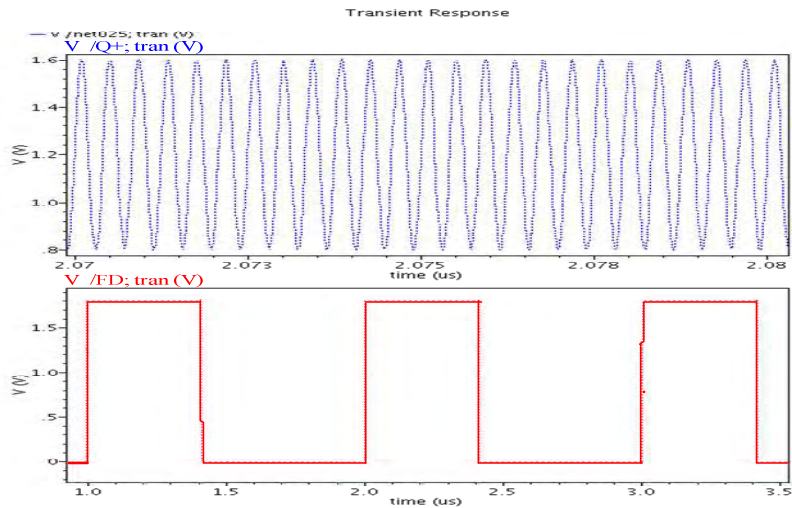
Fig.14 shows the schematic of an improved reloadable TSPC DFF used in the design of 6-bit S-counter. This reload DFF is similar to the reloadable DFF used in the design of P-counter [11]. However, the reloadable DFF for the S-counter needs an extra logic function MOD to be incorporated. When MOD goes high, the S-counter

remains idle for a period of  $N*(P-S)$  clock cycles and the reloadable DFF of the S-counter consumes some switching power. In the improved design, transistors  $M_6$  and  $M_7$  are added to reduce the switching activities in the reloadable DFF. When the state "0000" is reached, MOD goes high,  $M_6$  is turned-on and  $M_7$  is turned-off such that node S1 and S2 remain at logic '0' for the remaining  $N*(P-S)$  clock cycles until LD becomes high. During this period, since  $LD='0'$ , the right hand side portion of the circuit is de-activated similar to the reloadable DFF reported in [11]. Thus there is no switching activity at any node during the idle state of the S-counter and switching power is saved for a period of  $N*(P-S)$  clock cycles.

**Table 1.** Operation of the Reloadable DFF of the S-counter

MOD	Load (LD)	Programmable Input (PI)	Output (Q)
1	X	X	1
0	0	0	CLK/2
0	0	1	CLK/2
0	1	0	0
0	1	1	1

In other conditions, the operation of the improved reloadable DFF for S-counter is similar to the operation of the reloadable DFF used for the P-counter described in previous section. Table 1 shows the operation of reloadable DFF used in the S-counter. In this design, the P-counter is programmable from 51 to 52 ( $P_1$  and  $P_2$  are only programmable) and the S-counter is programmable from 0 to 47 ( $S_1$  to  $S_6$ ) in steps of 1 to accommodate division ratios from 2400 to 2484. The frequency division (FD) performed by the programmable divider is given by,



**Fig. 15.** Post layout results of the fully programmable divider with 2400 division ratio

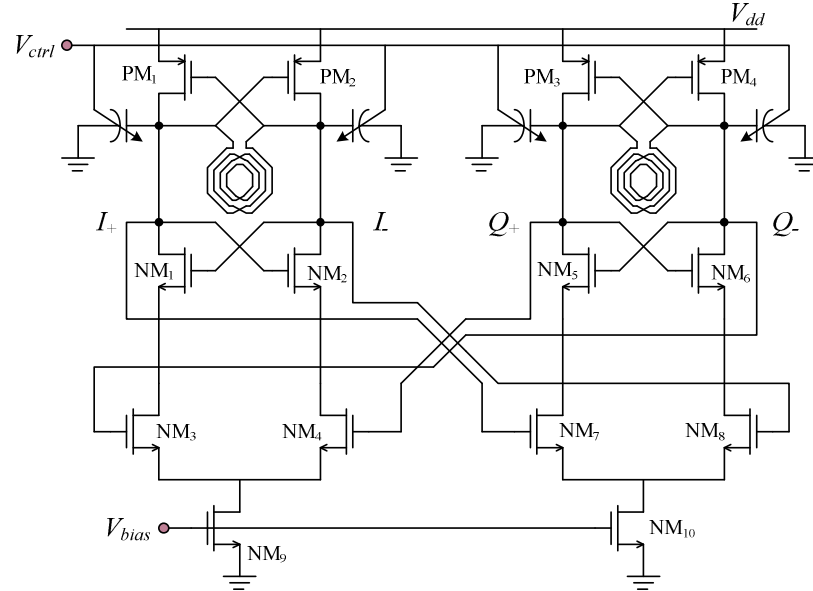
$$FD = N \times S + ((N + 1) \times (P - S)) = ((N + 1) \times P) - S \quad (5)$$

The fully programmable divider at 2.4 GHz consumes a power of 0.6 mW. Fig. 15 shows the post layout results of the fully programmable divider at 2.4 GHz with 1 MHz output signal of the divider having nearly 45% duty cycle. The P and S counter's programmable value for the division ratios between 2400-2484 is shown in Table 2.

**Table 2.** Programmable values of the programmable counters

Frequency division ratio	Prescaler (N/N+1)	Programmable-counter (P)	Swallow counter (S)
2400-2448	N=47	P=51	S=0-47
2449-2484	N=47	P=52	S=14-47

## 5 Quadrature Voltage-Controlled Oscillator (QVCO)



**Fig. 16.** Schematic of the implemented Q-VCO



The VCO implemented in this design is a series quadrature VCO (S-QVCO) and its schematic is shown in Fig.16. The S-QVCO has been proven to eliminate the trade-off between phase noise and I/Q mismatch [13]. Therefore, the design can be optimized for phase noise performance, while keeping I/Q mismatch low. Compare to the parallel QVCO, the coupling transistors NM<sub>3</sub>-NM<sub>4</sub> and NM<sub>7</sub>-NM<sub>8</sub> are in series with the switching transistors NM<sub>1</sub>-NM<sub>2</sub> and NM<sub>5</sub>-NM<sub>6</sub>. Hence the tail current for the coupling transistor is removed and the S-QVCO consumes less power.

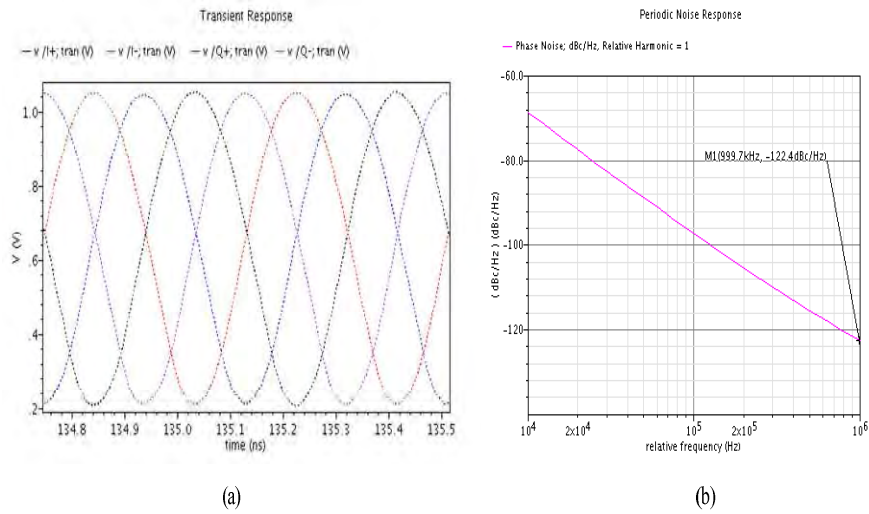


Fig. 17. a) Quadrature signals of S-QVCO b) Phase noise

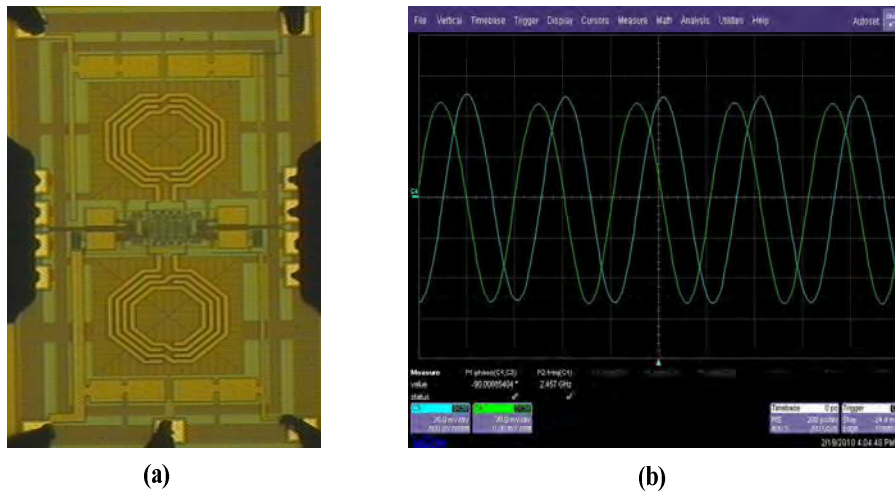


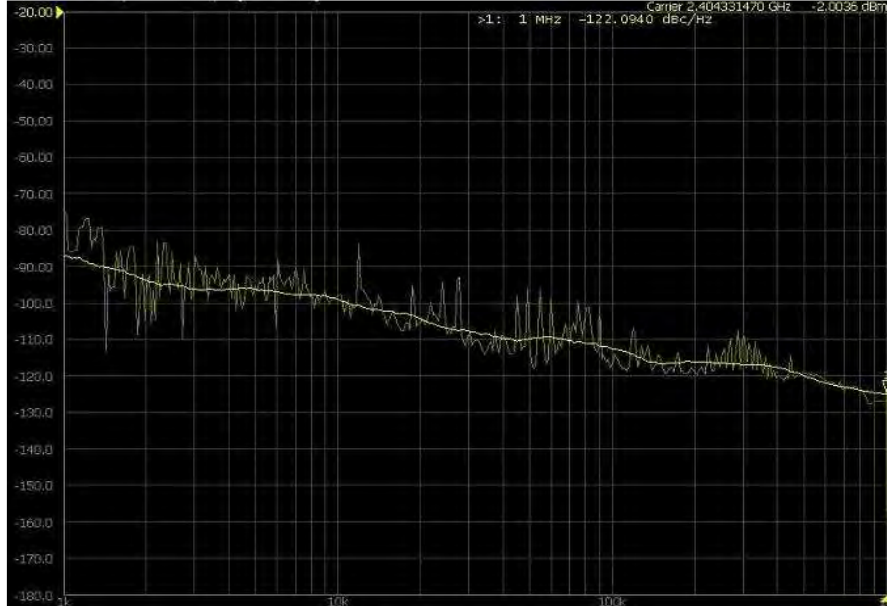
Fig. 18. a) die photograph of S-QVCO b) I/Q signal

The current reuse technique is used to further reduce the current consumption of the S-QVCO by adding cross-coupled PMOS transistors on top of the cross-coupled NMOS transistors. Open-drain transistors are added to the output nodes of the S-QVCO to serve as the buffer to the testing equipment. The gain of the S-QVCO from post layout results is 280 MHz/V and Fig. 17 shows the quadrature output signals and phase noise of the S-QVCO. The S-QVCO has phase noise of -122.4dBc/Hz at 1 MHz. The 2/3 prescaler is directly driven by the S-QVCO and it requires input signal with smaller amplitude for low power consumption. Thus S-QVCO bias current can be reduced to provide smaller amplitude which in turn reduces the power consumption of S-QVCO.

The measured phase noise is -122dBc/Hz at 1 MHz offset as shown in Fig.19 and the output signal amplitude is around 300 mV. The total power consumption of the S-QVCO is 2.7 mW at 1.8 V power supply. A widely used figure of merit (FOM) for the VCO is defined as [14]

$$FOM = L\{f_{offset}\} - 20 \log\left(\frac{f_o}{f_{offset}}\right) + 20 \log\left(\frac{P_{DC}}{1mW}\right) \quad (6)$$

Where  $L\{f_{offset}\}$  is the measured phase-noise at offset frequency  $f_{offset}$  from the carrier frequency  $f_o$ .  $P_{DC}$  is VCO power consumption in mW. Table 3 summarizes the performance of the S-QVCO.



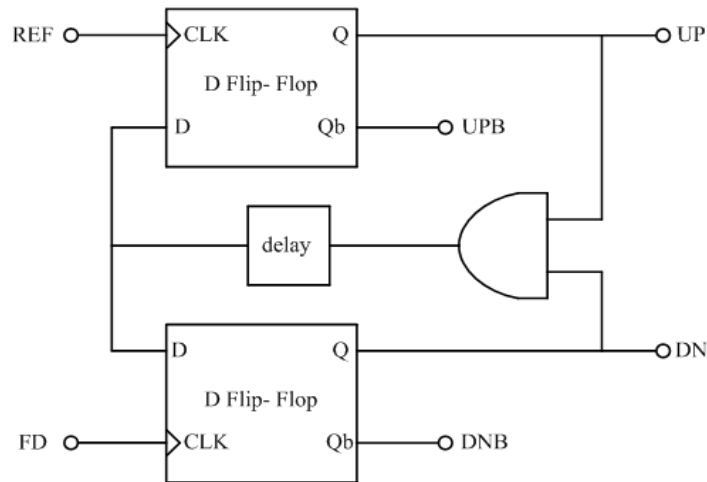
**Fig. 19.** Measured phase noise of the S-QVCO

**Table 3.** Performance of S-QVCO

Parameters	This Design
Power supply	1.8V
Technology	RF CMOS 0.18um
Frequency	2.2 -2.7 GHz
Tuning range	20.4%
VCO gain (KVCO)	414 MHz/V
Phase Noise	-122 dBc/Hz @ 1 MHz offset
Output amplitude	300 mV
I/Q phase difference	90.2°
Power consumption	2.88 mW
FOM	--177.4

## 5 Phase Frequency Detector (PFD) and Charge Pump (CP)

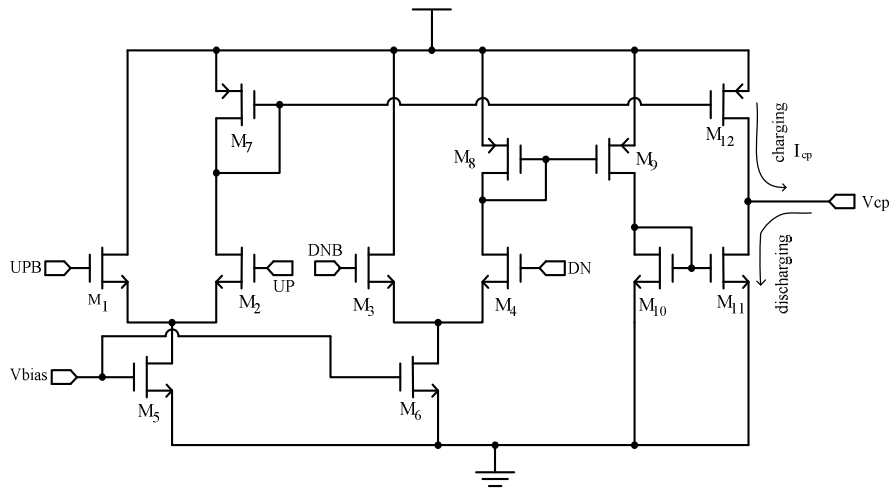
The PFD used in this design is a conventional NAND based circuit [15] as shown in Fig.20 which consists of two TSPC DFF registers, a AND gate. A certain amount of delay is introduced after the AND gate before resetting the DFF to keep the pulse width of UP and DN signals finite so as to eliminate the problem caused by dead zone. The half-transparent DFF reported in [12] is implemented as the DFF register in this design. The dead-zone removal pulse is of 1 ns, which is sufficient to turn-on UP and DN switches of the charge pump during the locked condition.



**Fig. 20.** Phase frequency detector (PFD)

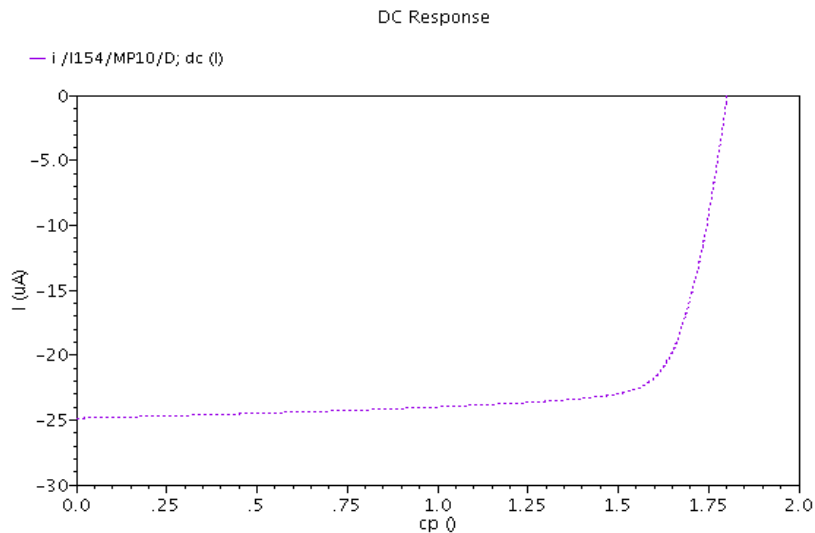
The schematic of the charge pump used in the design of PLL synthesizer is shown in Fig.21. The charge pump circuit consists of two input differential pairs  $M_1$ - $M_2$  and  $M_3$ - $M_4$  which act as the switches, two current sources  $M_5$  and  $M_6$  supply stable current to the differential switches, a pump-up sub circuit formed by  $M_7$  and  $M_{12}$

outputs the charge current  $I_{\text{charge}}$  and a pump-down sub-circuit formed by  $M_8$ ,  $M_9$ ,  $M_{10}$  and  $M_{11}$  which helps to discharge the current  $I_{\text{discharge}}$ .



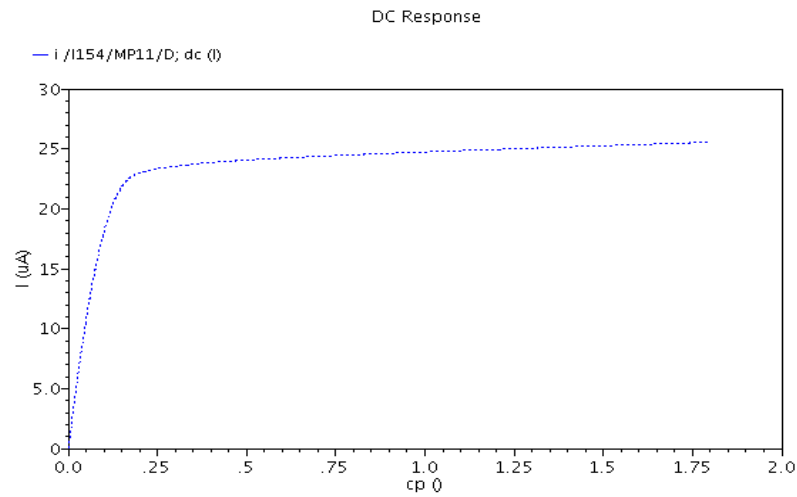
**Fig. 21.** Implemented Charge pump

*Case-I: UP='1' and DN='0'.* When the UP signal is high (UP='1') and the DN signal is low (DN='0'),  $M_4$  is turned-off,  $M_2$  is turned-on which switches on the pump-up sub-circuit. Hence the charging current  $I_{\text{charge}}$  flows through  $M_{12}$  charging up the loop filter. Since  $M_4$  is turned-off, the pump-down sub-circuit is turned-off and no discharge current  $I_{\text{discharge}}$  current flows in  $M_{11}$ .

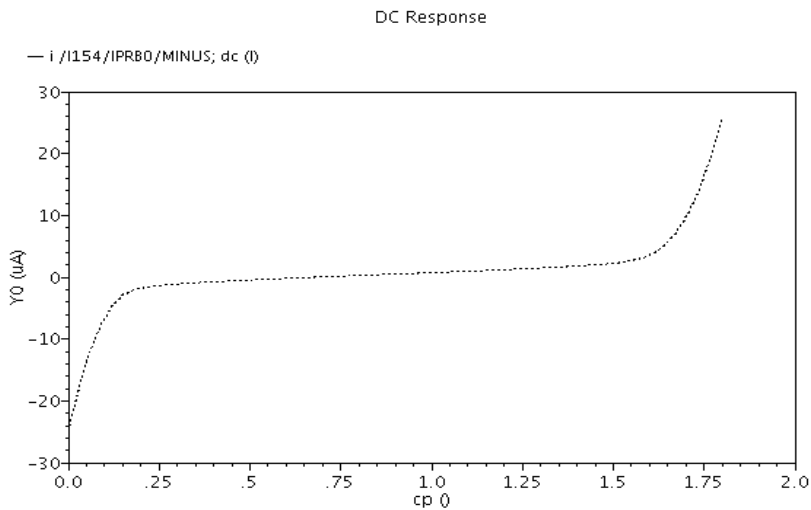


**Fig. 22.** Charging current from charge pump when UP is high and DN is low

*Case-II: UP='0' and DN='1'*. When the UP signal is low (UP='0') and the DN signal is high (DN='1'),  $M_2$  is turned-off,  $M_4$  is turned-on which switches on the pump-down sub-circuit. Hence the discharging current  $I_{\text{discharge}}$  flows through  $M_{11}$  to the ground discharging the loop filter. Since  $M_2$  is turned-off, the pump-up sub-circuit is turned-off and no charge current  $I_{\text{charge}}$  current flows in  $M_{12}$ . Fig.22 and Fig.23 shows the simulated DC simulations of UP and DN currents of the charge pump.



**Fig. 23.** Discharging current from charge pump when UP is low and DN is high

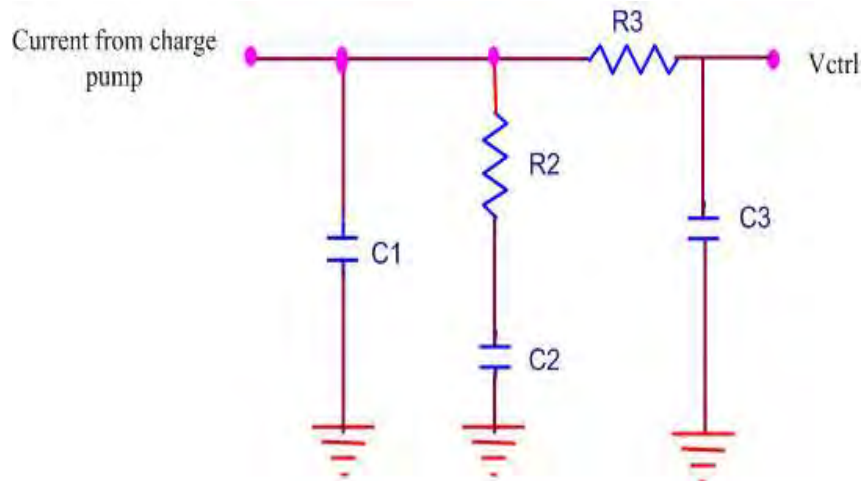


**Fig. 24.** Mismatch current from charge pump when UP and DN are high

*Case-III: UP='1' and DN='1'.* When both the UP and DN signals are driven high (UP='1' and DN='1'), both  $M_4$  and  $M_2$  are turned-on and switch on both the pump-up and pump-down sub-circuits allowing the currents to steer through  $M_{11}$  and  $M_{12}$ . If both charging ( $I_{\text{charge}}$ ) and discharging ( $I_{\text{discharge}}$ ) currents are equal, the charge stored on the loop filter remains same and doesn't affect the control voltage at the input of VCO. However, there exists a mismatch between charging and discharging current due to the mismatch of devices  $M_{11}$  and  $M_{12}$ , and a net current of ( $I_{\text{charge}} - I_{\text{discharge}}$ ) leaks in to the loop filter and alters the control voltage.

In this design, both the differential switches  $M_1$ - $M_2$  and  $M_3$ - $M_4$  are implemented by NMOS transistors to avoid the switching mismatches. To have precise matching in the charging and discharging currents, the length of the output stage transistors are kept high to increase the output impedance. Here the charge pump current chosen is 25  $\mu\text{A}$ . Fig.24 shows the mismatch between the UP and down currents and the average mismatch current is around 1.4  $\mu\text{A}$ .

## 6 Loop filter Design



**Fig. 25.** 3<sup>rd</sup> order loop filter

The loop filter used in this design is 3<sup>rd</sup> order as shown in Fig. 25. The loop filter parameters are imposed by the system level performance specifications such as settling time, phase noise and spur suppression. Initially a 2<sup>nd</sup> order filter is designed and later a RC low-pass section is added to improve the spurs and reduce the ripples on control voltage. The reference frequency used in this design is 1 MHz. The 2<sup>nd</sup> order filter is assumed to be a critically damped system ( $\xi = 1$ ) with a loop bandwidth ( $f_c$ ) of 45 KHz to satisfy the Gardner's stability criterion [16]. For an optimal stability, for a passive second order filter, the relation between unity gain cross-over frequency ( $\omega_c$ ) and natural frequency ( $\omega_n$ ) is given by [17]

$$\omega_c = 2\xi\omega_n \quad (7)$$

Since the damping factor is equal to unity, the natural frequency ( $f_n$ ) is found to be 22.5 KHz. For a charge pump PLL with 2<sup>nd</sup> order loop filter and damping factor  $\xi=1$ , the relation between zero frequency ( $f_{z1}$ ) and cross-over frequency ( $f_c$ ) is given by [5]

$$4 = \frac{(K_{vco}I_{cp}R_2) \times (C_2R_2)}{2\pi N} = \frac{f_c}{f_{z1}} \quad (8)$$

Similarly, the relation between pole frequency ( $f_{p1}$ ) and cross-over frequency ( $f_c$ ) is given by

$$4 = \frac{(K_{vco}I_{cp}R_2) \times (C_2R_2)}{2\pi N} = 2\pi f_c (16 \times C_1R_2) = \frac{16 \times f_c}{f_{p1}} \Rightarrow f_{p1} = 4f_c \quad (9)$$

Based on (9) and (10), the zero frequency and pole frequency are 11.25 KHz and 180 KHz respectively. The phase margin is given as

$$\phi = \tan^{-1}\left(\frac{f_c}{f_{z1}}\right) - \tan^{-1}\left(\frac{f_{p1}}{f_c}\right) = \tan^{-1}(4) - \tan^{-1}\left(\frac{1}{4}\right) = 61.92^\circ \quad (10)$$

With a charge pump current of 25 uA ( $I_{cp}$ ), VCO gain ( $K_{vco}$ ) of 414MHz/V and division ratio ( $N$ ) of 2450, the values of  $R_2$ ,  $C_2$  and  $C_1$  are calculated as,

$$C_2 = \frac{I_{cp} \times K_{vco}}{2\pi \times N \times (2\pi f_n)^2} = 207 \text{ pF} \quad (11)$$

$$R_2 = \frac{1}{2\pi \times f_{z1} \times C_2} = 78.5 \text{ k}\Omega \quad (12)$$

$$C_1 = \frac{C_2}{16} = 12.9 \text{ pF} \quad (13)$$

The open loop PLL with a 2<sup>nd</sup> order loop filter is simulated in Matlab and Fig.26 shows the root locus plot of the open loop PLL. Fig.27 shows the simulated Bode diagram of the open loop PLL where the phase margin is around 62. Fig.28 shows the open loop gain and phase margin.

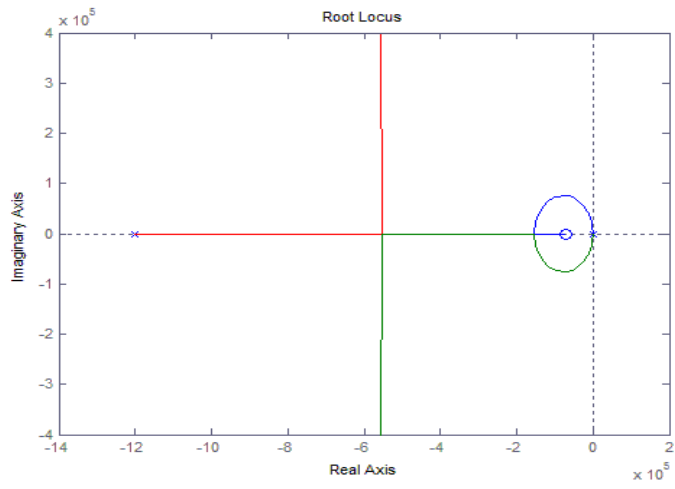


Fig. 26. Root locus of open loop PLL with 2<sup>nd</sup> order filter

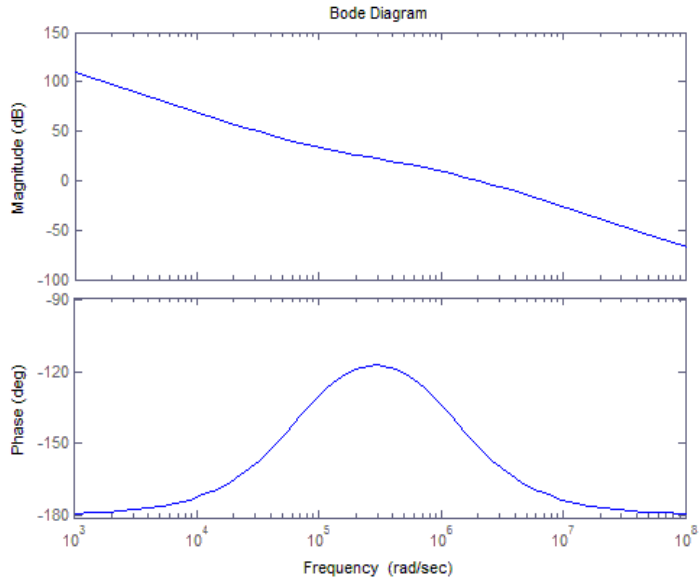


Fig. 27. Bode plot with 2<sup>nd</sup> order filter



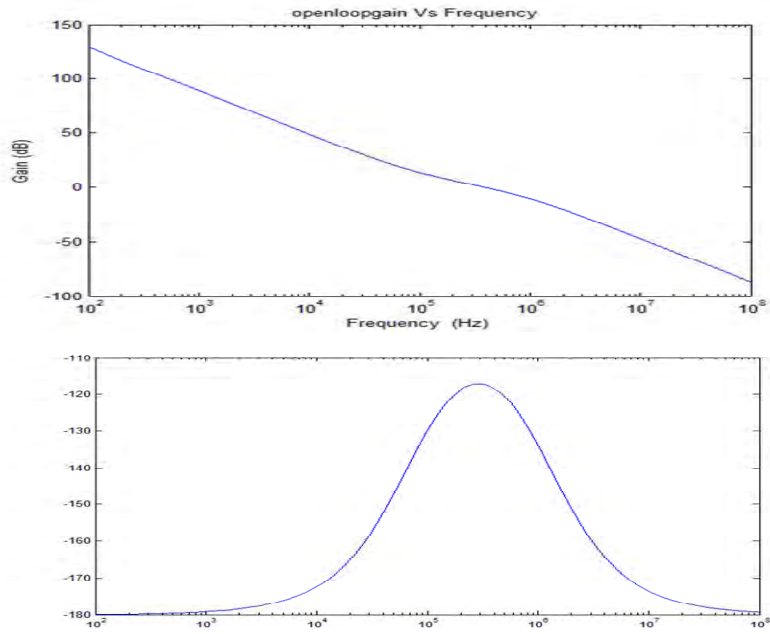


Fig. 28. Open loop response of PLL

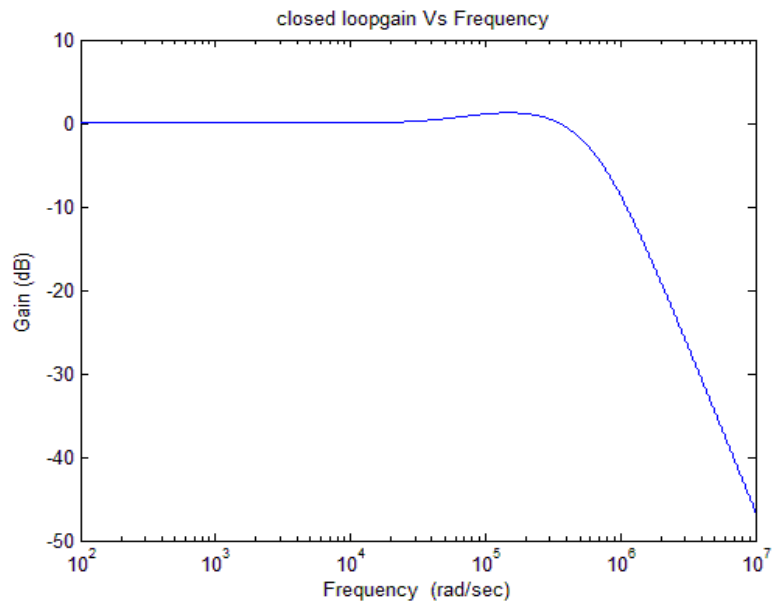
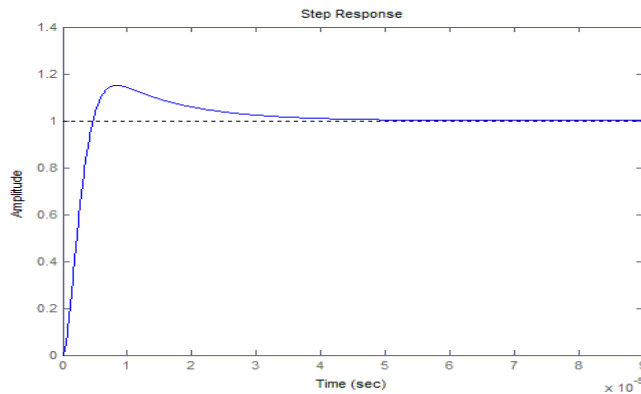
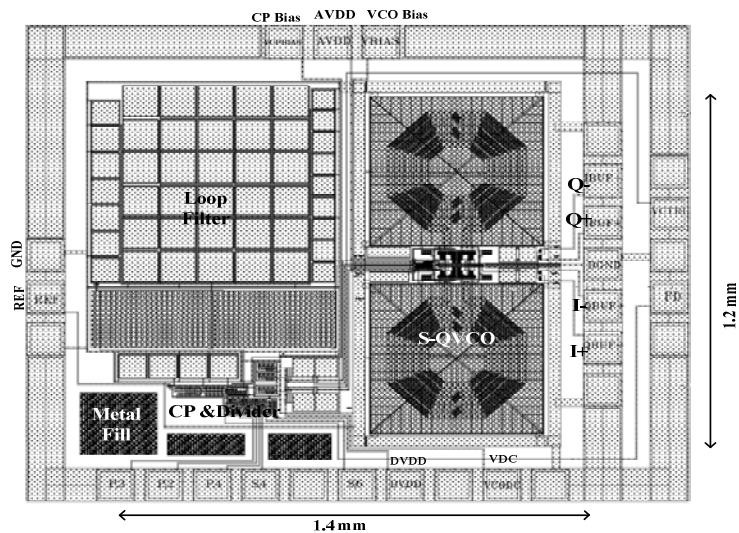


Fig. 29. Closed loop gain of PLL



**Fig. 30.** Step response of the closed loop PLL

Fig. 29 and Fig.30 shows the closed loop gain and step response of the PLL. An additional RC low pass section is added to reduce the amount of reference spurs at the cost of reduced phase margin and increased settling time. The additional RC low pass section is added to the 2<sup>nd</sup> order filter such that the phase margin won't reduce to lesser value than 55 degrees. With additional RC section, damping factor reduces to slightly less than 1. The value of  $R_3$  and  $C_3$  are found to be 98.9 Kohms and 3.75 pF respectively. With frequency accuracy of 40 ppm, the calculated settling time is  $48 \mu s$ , which is nearly four times less than the required settling time for IEEE 802.15.4 standard ( $192 \mu s$ ).



**Fig. 31.** Layout of 2.4 GHz frequency synthesizer with testing pads

The layout of the fully programmable 2.4 GHz synthesizer with on-chip 3<sup>rd</sup> order loop filter and testing pads is shown in Fig. 31. The synthesizer occupies an area of  $1.4 \times 1.2 \text{ mm}^2$  with testing pads and the core area is  $0.95 \times 0.9 \text{ mm}^2$ . The simulations are performed using Cadence SPECTRE RF for a 0.18 $\mu\text{m}$  CMOS process. The settling time for the synthesizer is around  $58 \mu\text{s}$  which is 4 times lesser than the value required by IEEE 802.15.4 standard.

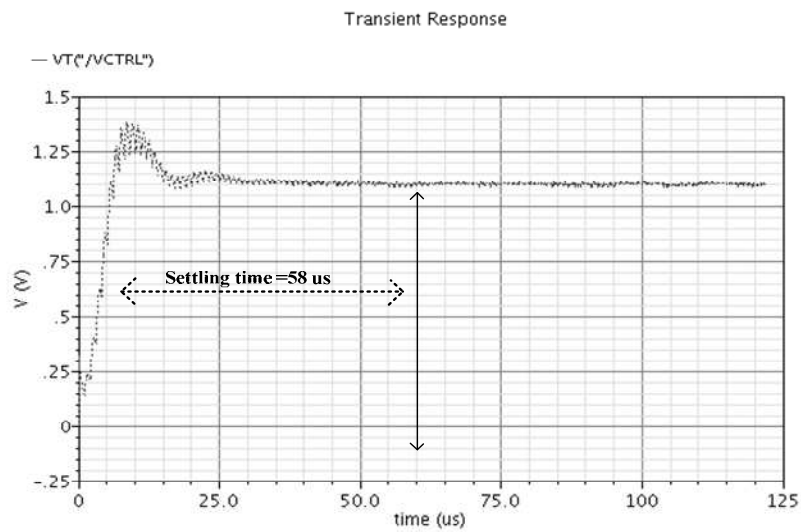


Fig. 32. Settling behavior of the implemented frequency synthesizer

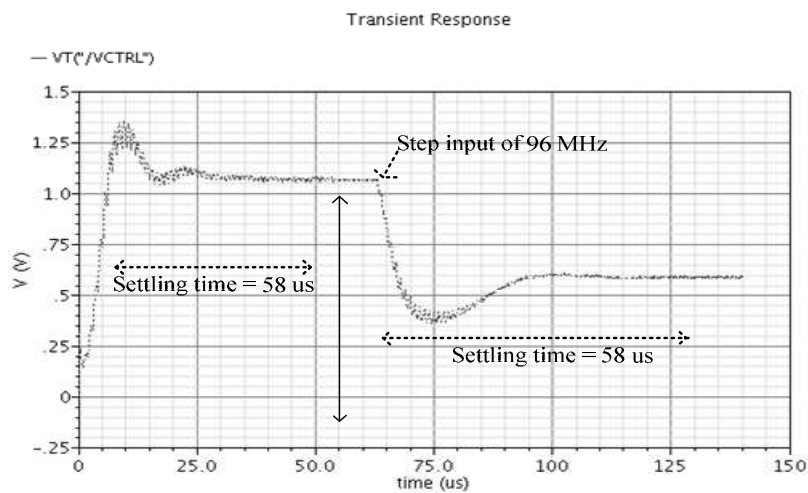
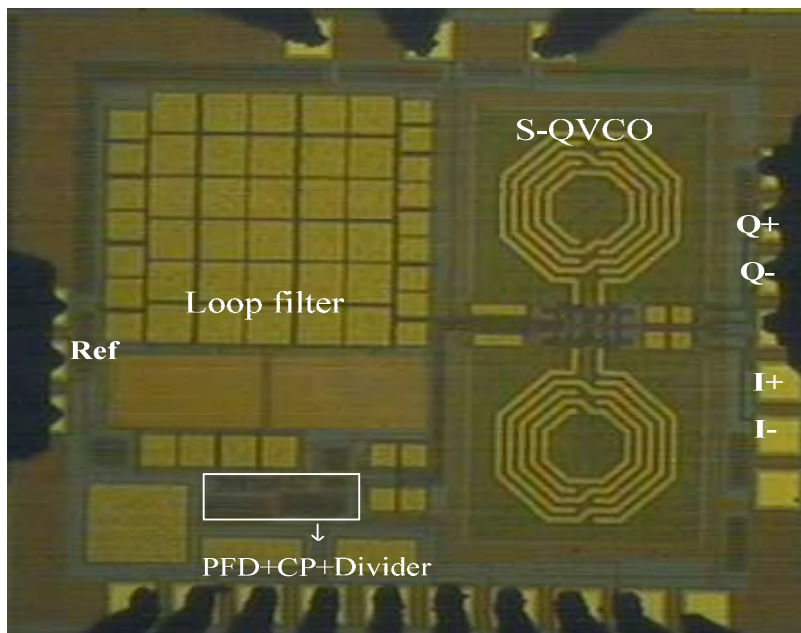


Fig. 33. Settling behavior of synthesizer with change of N from 2400 to 2496

Fig.32 shows the settling behavior of the synthesizer for fixed channel which shows the settling time is around 58 us. Fig.33 shows the settling behavior of the synthesizer when the division ratio is changed from 2400 to 2496. The implemented fully programmable 1 MHz resolution frequency synthesizer consumes 3.6 mW (2 mA) from a power supply of 1.8 V, which is significantly lesser than the synthesizers reported in literature implemented with dynamic logic dividers.

## 7 Measured Results



**Fig. 34.** Die photograph of 2.4 GHz PLL frequency synthesizer

For silicon verification, the proposed fully programmable 2.4 GHz frequency synthesizer is fabricated using the chartered 1P6M 0.18 um CMOS process. Fig.34 shows the die photograph of the implemented 2.4 GHz frequency synthesizer. On-wafer measurements are carried out using an 8 inch RF probe station. The input signal for the measurement is provided by the Agilent 33120A arbitrary signal generator and the output signals are captured by the Lecroy Wave master 8600A 6G oscilloscope. The output spectrum and phase noise of the synthesizer is measured using the Agilent E4407B 9 kHz-26.5 GHz spectrum analyzer. Fig.35 shows the measured output spectrum of the PLL.

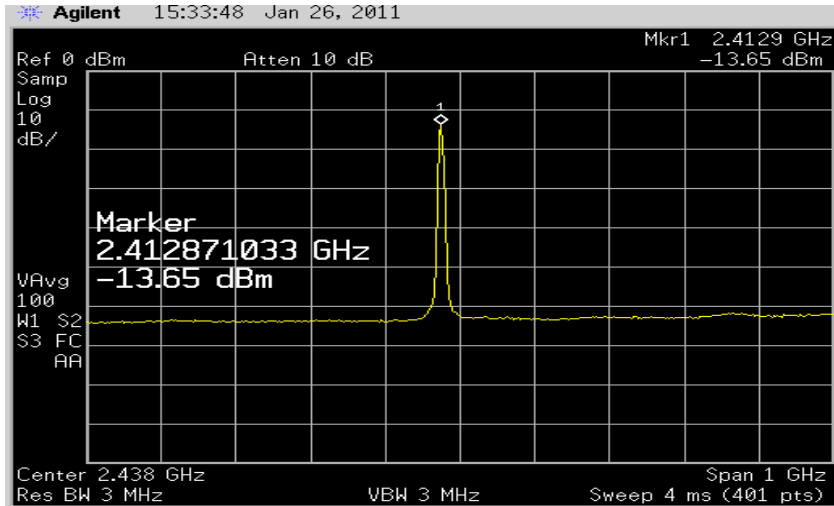


Fig. 35. Measured PLL output spectrum

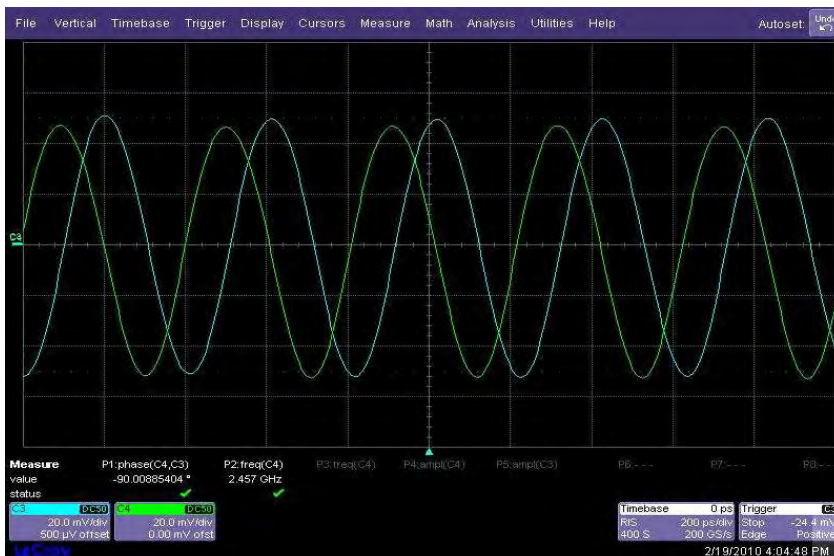


Fig. 36. Measured I/Q signal at PLL output

The VCO tuning range is from 2.369 GHz-2.692 GHz (323 MHz) and output amplitude is around 300 mV as shown in Fig.36. The power consumption of S-QVCO is 2.9 mW. The measured ripples on the control voltage is around 1 mV and power consumption of divider , charge pump other blocks is around 0.9 mW. Fig.37 shows the 1 MHz output from the fully programmable divider whose duty cycle is around 43%. The phase noise of the PLL is -111.4dBc/Hz at 1 MHz offset as shown in

Fig.38. The performance of the implemented low power 2.4 GHz frequency synthesizer is analyzed in Table 4.

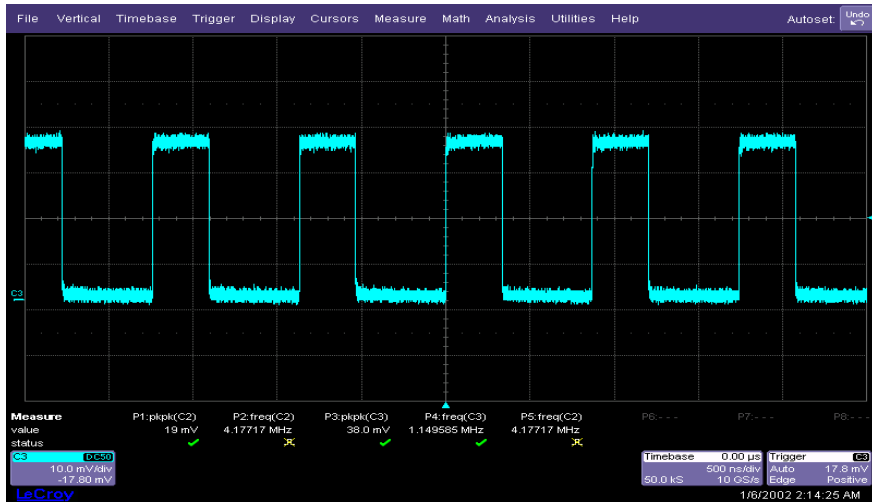


Fig. 37. Measured 1 MHz output of the divider

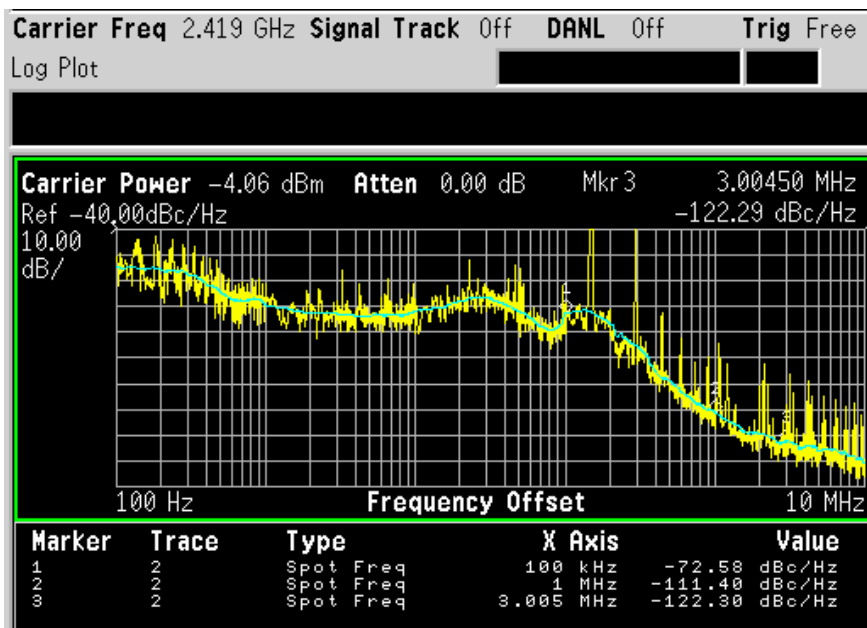


Fig. 38. Measured PLL output phase noise

**Table 4.** State of Art Synthesizer Comparison

Reference	[4]	[5]	[18]	[19]	This work
Process	0.25um	0.18um	0.18 um	0.2 um CMOS/SOI	0.18 um
Channel spacing	1 MHz	5 MHz	3 MHz	1 MHz	1 MHz
Frequency Range (GHz)	2.4-2.527	2.29-2.64	2.44-2.47	2.4	2.2-2.5
Loop filter	On- chip	On- chip	On- chip	Off- chip	On- chip
Phase noise (dBc/Hz)	-112 @1 MHz	-130 @10MHz	-112 @1 MHz	-104 @1MHz	-111.4 @1MHz
Settling time	60 us	55 us	500 us	600 us	35us
Power consumption	20 mW at 2.5V	15 mW at 3 V	8.2 mW at 1.8V	17 mW at 1 V	4.9mW at 1.8V

## 8 Conclusion

In this paper, a fully integrated 1 MHz resolution 2.4 GHz CMOS frequency synthesizer for IEEE 802.15.4 standard is designed using Global foundries 0.18 um CMOS technology is presented. A new 47/48 dual-modulus prescaler based on true-single phase clock is proposed along with the improved reloadable DFF for the swallow S-counter. The fully programmable divider only consumes 600 uW which is very compared to the fully programmable dividers reported in literature. The measured tuning range of the S-QVCO is 2.369 GHz-2.692 GHz and the output amplitude is 300 mV, which is sufficient to drive the divider. The phase noise of the PLL is -111.4dBc/Hz at 1 MHz offset and the total power consumption of the synthesizer is 3.8 mW.

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