A 100dB SFDR 0.5V pk-pk Band-Pass DAC Implemented on a Low Voltage CMOS Process

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Abstract. Direct Digital Synthesis (DDS) systems generate fine frequency resolution signals over a broad spectrum that are used in a wide variety of applications such as multi-mode RF, communications, measurements and test. A high performance DDS band-pass Digital to Analog Converter (DAC) architecture and implementation is presented that delivers high spectral purity over a narrow-band response. The low power D/A Converter is portable to standard CMOS processes and designed to achieve over 100dB narrow-band SFDR performance using Sigma-Delta ($\sum\Delta$) modulation and multi-bit current steering techniques. A 3rd order digital $\sum\Delta$ modulator is combined with a 4th order digital Dynamic Element Matching (DEM) block to shape the noise while calibrating for process mismatch variations. A low silicon area output stage is used to deliver a high performance specification.

Keywords: DDS, Digital to Analog Converter, Band-Pass DAC, Static Mismatch, Noise-shaping, DEM

1   Introduction

Band-Pass DACs achieve high resolution in the band of interest typically around the centre tone at $F_s/4$. Moving from a traditional Nyquist DAC to an oversampling Sigma-Delta ($\sum\Delta$) DAC architecture offers a significant saving in analog components, making the design more portable across technology nodes. Combining a digital multi-bit $\sum\Delta$ modulator design with an analog multi-bit DAC implementation allows for spectral shaping of the quantization noise moving it to frequency bands higher and lower than the band of interest. Multi-bit, high order modulators offer better dynamic range and improved noise shaping at low oversampling rates when compared to their 1-bit counterparts, but rely heavily on the linearity of the analog DAC. Unfortunately CMOS device mismatch severely impacts the DAC performance levels - since its linearity must match the modulator capabilities for the band-pass DAC to operate to a

high specification, it is imperative that this mismatch be removed. This is difficult to achieve especially for low-voltage low nm processes, where process gradients and Shallow Trench Isolation (STI) effects dominate. Dynamic Element Matching (DEM) is a digital signal processing technique that effectively eliminates the error due to component mismatch introduced during fabrication. Several DEM techniques exist such as Data Weighted Averaging (DWA) [1], Butterfly-shuffler [2], Tree structure [3] and Vector Feedback [4] but so far the mismatch shaping provided by these schemes is limited to second order. Research has shown that Vector Feedback DEM has the potential to provide higher orders of mismatch shaping [5], however hardware designs with stable implementations or orders greater than 2 remain difficult to achieve for high frequencies and low silicon area overheads. In particular, the area occupied by the DEM circuitry is known to increase exponentially with higher N-bit DAC sizes and this typically limits the number of bits in the DAC to between 4 and 6 [6].

In this chapter, a band-pass DAC comprising of a 3rd order sigma-delta band-pass modulator, a stable 4th order DEM, and a 5-bit current steering DAC is presented. The plot in Fig 1 shows the simulated DAC performance with and without DEM noise-shaping for 2% (Gaussian distributed) element mismatch. To illustrate the effects of component mismatch on signal quality, the narrow-band Spurious Free Dynamic Range (SFDR) results for a "thermometer coded DAC" with no DEM are displayed on the left hand side of the graph. The results show there is a significant reduction in the SFDR of the converter due to the mismatch between the elements in the DAC. The right hand side plot shows a significant SFDR improvement when the band-pass Vector Feedback DEM switching scheme is employed. The DEM scheme reduces the impact of element mismatch in the narrow frequency band around the centre tone, moving it to frequencies outside the band of interest. Analysis of the switching events with the DEM in place shows that the mapping of the DAC elements is now no longer directly related to the modulator code, but is determined by the usage history of the elements. The DEM scheme allows the DAC to achieve a simulated SFDR of 117dB for a 2% mismatch that is close to ideal SFDR of the DAC with zero element mismatch (120dB).
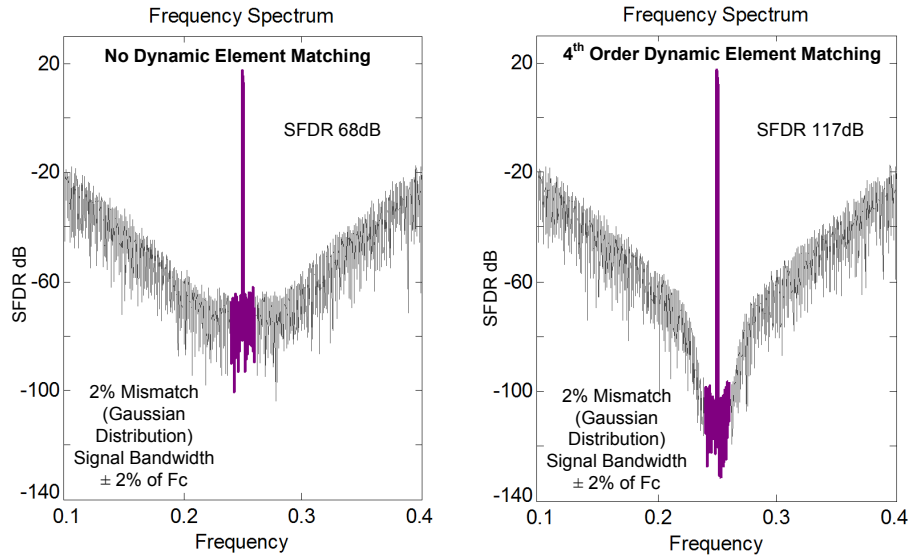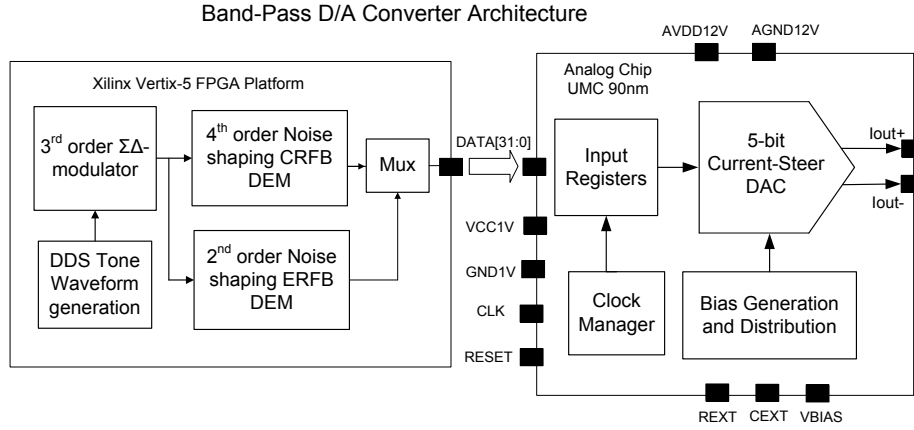
Fig. 1. SFDR level for thermometer DAC (no DEM) (LHS) and with 4th order DEM (RHS)

1.1 DAC Architecture

The band-pass DAC (BPDAC) has a high narrow-band SFDR specification of 100dB over a band of interest (±2% of the signal frequency). In particular, this specification targets DDS and RF applications where distortion over the band of interest must be kept to a minimum. Fig. 2 shows the system level view of the entire DAC. A 3rd order multi-bit $\sum\Delta$ band-pass modulator truncates and noise-shapes the data coming from the DDS generator; the modulator provides this data to the DEM block as a 5-bit word. The DEM maps each 5 bit word to the corresponding elements in the current steering DAC (C-DAC). Simulations have shown that this architecture is capable of achieving the desired performance level without the need for complex analog circuitry. The design focuses on using digitally assisted analog blocks to make the design highly portable across standard CMOS process technologies. The mixed-signal design operates off a 1.0V supply for the digital logic and a 1.2V supply for the analog multi-bit C-DAC section. The DAC can be used in System-on-Chip (SoC) CMOS applications requiring low-power solutions. The design was separated into the digital section containing the $\sum\Delta$ modulator, DEM and input stages to the C-DAC, while the analog part consists of synchronization logic, current sources with differential switches, and bias generation blocks.

Band-Pass D/A Converter Architecture

Fig. 2. Band-Pass DAC Architecture

The output stage is a 5-bit C-DAC, which features the traditional elements of a current-steering DAC using differential switching. High-threshold PMOS (HVTH) cascode devices are used to increase the output resistance for stable operation up to 0.5V pk-pk. The complimentary current signals can be output from the chip either to external resistors or to a band-pass filter. The C-DAC is a mixed-signal design where logic is used to synchronize the 32-bit value from the DEM block into the switch sections to steer the correct current to the output. An operational amplifier generates a stable reference current to bias the current source devices.
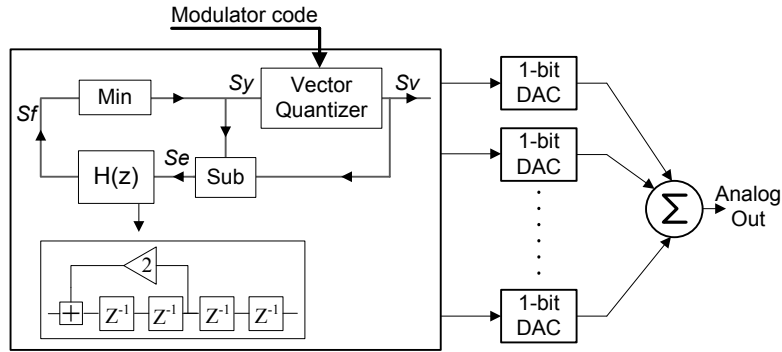
2   Digital Design Overview

The $\sum\Delta$ modulator which quantizes and noise shapes the digital signal was developed from a low-pass cascade of resonators with distributed feedback (CRFB) structure and converted it to a band-pass using the $Z^1 \rightarrow -Z^2$ transform. The result of the transform shapes the quantization noise above and below the centre frequency (located at $F_s/4$), while maintaining the same stability as its low-pass counterpart. The transform of a 3rd order low-pass modulator gives an equivalent 6th order band-pass modulator. Dither is inserted prior to the quantizer to provide a sufficiently busy signal, breaking up unwanted tones and improving SFDR levels by 2~3dB. Equation (1) [7] determines the order (L), quantizer resolution (N) and OSR for the modulator. The shape of the spectrum around the band of interest can be altered by the choice of OSR. A larger OSR will increase the Dynamic Range (DR) over a narrower bandwidth; a lower OSR will reduce the maximum dynamic range but yields a larger bandwidth. For the modulator, a 3rd order (L=3), 5-bit (N=5) quantizer, and an OSR=16 was selected to deliver an ideal SDFR/SNR of 120dB/108dB over a 5% band, centred on $F_s/4$.

$$DR_{dB} = 10\log\left[\frac{3}{2}\left(2^N - 1\right)^2 \frac{(2L + 1)OSR^{2L+1}}{\prod^{2L}}\right] \tag{1}$$

DEM blocks are applied to multi-bit DACs both to suppress the power of the DAC mismatch noise in specific frequency bands and to eliminate harmonic distortion. The objective is to shape these errors so they no longer appear in the signal band of interest, but are pushed out to higher frequencies. The technique involves selecting the DAC elements intelligently so that the mismatch errors are smeared out. Vector Feedback DEM (VFBDEM) maps each modulator code to the DAC element based on their usage history; Fig. 3 shows the signal path of a 2nd order DEM. The Vector Quantizer chooses the appropriate number of DAC elements to turn on based on the value contained in the noise shaped data-stream coming from the primary modulator. The choice of which elements to turn on is based on the value of the vector *Sy* at the input to the Vector Quantizer. The DAC element(s) corresponding to the input(s) with the largest value(s) are given priority in forming the analog signal. The conventional VFB DEM structure is similar to an error feedback modulator structure whereby the output from the Vector Quantizer *Sv* is subtracted from the input; the resulting error signal *se* is then filtered. The outputs from the filter banks are processed whereby the minimum value of the vector *Sf* is calculated and subtracted from each signal before going into the Vector Quantizer for the next modulator code. The order of the filter determines the order of mismatch shaping of the complete system. At present, the order of the mismatch filtering provided by the DEM is limited to 2. An attempt to extend the conventional loop to a higher order Error Feedback (ERFB) structure fails due to instability in the loop. For an error feedback loop of order greater than two to remain stable, a multi-bit feedback path is required.

Replacing the existing ERFB structure of a conventional VFB DEM with a single loop IIR filter allows for higher order noise shaping while maintaining loop stability using a single bit feedback path. The design of these single loop IIR filters is similar to the design of a single loop 1-bit sigma-delta modulator. Setting the oversampling ratio to match the main noise shaper provides for the maximum dynamic range over the entire band of interest. Choosing an out-of-band noise gain of 1.5 permits a high degree of noise shaping while ensuring the modulator remains stable. Increasing the out of band gain yields a more aggressive noise shaping filter but compromises its stability. One key advantage of using high order IIR filter structures is the ability to optimize the zero location by moving the zeros at the real axis along the unit circle. This has the effect of spreading the noise shaping over the entire signal band, leading to a wider signal bandwidth. The effect of zero optimization is evident when evaluating the SNR & SFDR performance over a larger bandwidths e.g. ±2.5% of the centre frequency. The band of interest around the centre frequency remains clear of noise, yielding a higher SFDR when compared to the non-optimized structure. The low pass filter is converted into a specific topology, in this case a CRFB structure. The filter coefficients are quantized to power of two as this avoids the need for

hardware expensive multipliers when implemented in logic. The low-pass filter is then converted to a band-pass filter with the center frequency at Fs/4.

Fig. 3. Modulator and DEM Block Diagram

The extra filtering provided by the 4th order IIR filter adds significant number of bits to each vector making the thermometer decoded Vector Quantizer (VQ) in the ERFB DEM inefficient. To process the filtered signals in the minimum time, an enhanced VQ algorithm was designed. This VQ uses a 2 stage pipeline to reduce the critical path; however inserting an extra delay will cause the DEM loop to go unstable. Loop integrity is maintained by using the path prior to the last register output of the IIR filter counteracting the extra delay introduced in the VQ path. Bit reduction logic within the VQ inspects the max/min vector values and truncates redundant bits on each vector. The VQ implements a fine and coarse ranking algorithm using combinational logic; the coarse VQ ranks the vectors based on the 5 MSB's with the result passed to the fine VQ on the next clock cycle. The fine VQ further sorts and ranks the vectors based on the remaining LSB values.

The 4th order VFBDEM is shown in Fig. 4. The 4th order noise-shaping CRFB modulators use minimum register sizes to contain area, while maintaining stable operation over a 5% band. The DEM sub-blocks containing the signal minimizer and quantizer sections are partitioned and pipelined to enable operation up to 100 MHz F_s. The Verilog RTL is targeted to a Xilinx FPGA for validation with the separate analog chip section. The design was synthesized to 90nm CMOS to get timing, power and area information; this is detailed in the measurements and results section.
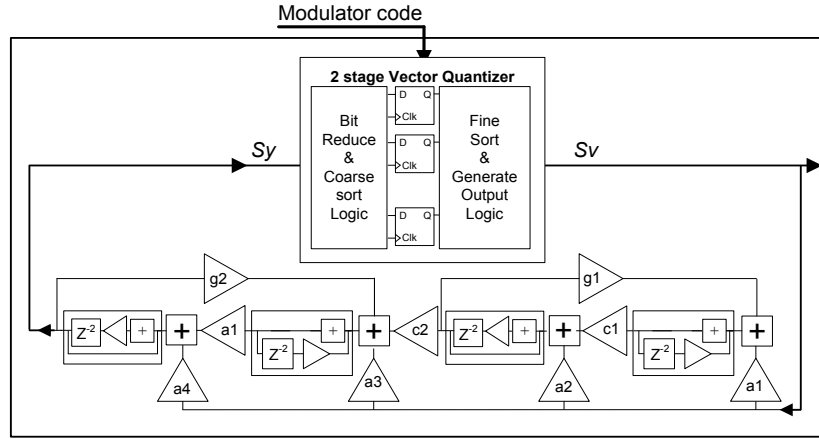
Modulator code

Fig. 4. 4th Order CRFB DEM

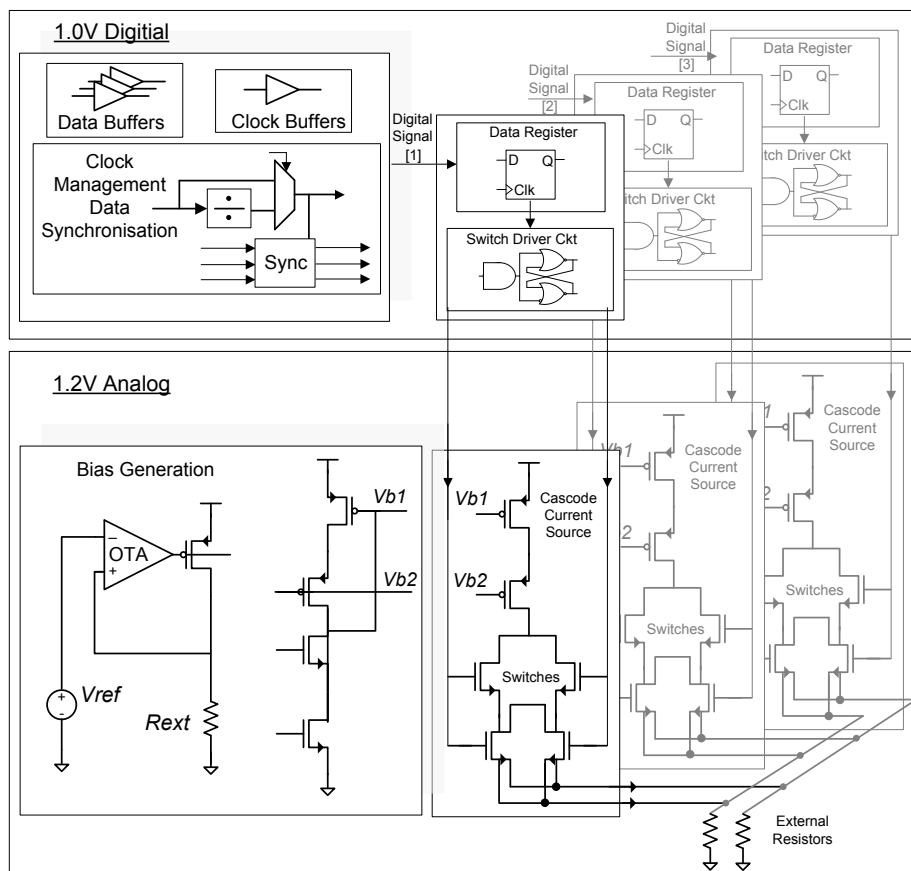## 3   5-bit Unary Current Steering DAC

Nyquist-rate current-steering DACs are used in high-speed lower resolution applications, however dynamic switching at the output of the current sources degrades performance. Architectural and layout concerns restrict the resolution and linearity performance. Smaller multi-bit DACs can be combined with the digital $\sum\Delta$ and DEM stages to achieve the high performance requirements for oversampled signals. C-DACs are typically used, but the glitch energy introduced by the current switching generates non-linear distortions. The glitch effects are related to the clock feed through and switched induced energy of the internal switching circuitry. Clara et al [9] investigated the non-linear distortion effects of switching and determined the harmonic distortion due to asymmetry in the signal switching for harmonic n=1,2,3.. in Equation 2.

$$HD_{2n} \approx 20\log_{10}\left[A\frac{N \cdot Sin\left(\frac{\pi}{OSR}\right) \cdot \left|\varepsilon_{off} - \varepsilon_{on}\right|}{\pi(2n+1)(2n-1)} \right]$$

(2)

Even harmonic distortion products are generated in the differential output signal if the switching error is asymmetric ($\varepsilon_{ON} \neq \varepsilon_{OFF}$). Clearly, the switching signal characteristics need to be symmetrical to minimize the harmonic content at the output of the current-source cell. Careful design and layout consideration for the switched driver must also be used. An optimized 32-bit element C-DAC was developed paying attention to the rise-fall time symmetry at the switch input, utilizing careful layout design practice. Driver voltage levels and circuit jitter considerations were also seen to improve the performance and portability for low-nm processes. The C-DAC was taped-out in 90nm CMOS technology and optimized for generating tones in the low

MHz range for connection to the modulator and DEM blocks implemented on FPGA. As the frequency increases, the MOS device capacitance takes over the tranconductance and output resistance levels. The C-DAC was designed to enable a stable output voltage swing of 0.5V. The basic unary weighted C-DAC architecture is shown in Fig 5. This consists of 32 register and driver cells attached to a switched cascode current source matrix. A gain enhanced folded cascode operational amplifier (opamp) is used to generate a stable accurate reference adjustable via REXT for biasing the cascode and current sources.

Fig. 5. Current-Steer DAC (C-DAC)

The clock manager contains a phase generator used for triggering external measurements. A buffer tree is used to synchronize the data and clock signals to the register cells to reduce jitter effects. The register cell is based on a data input pass gate design and an inverter output stage to reduce clock feed-through to the driver circuit.

Two identical cascaded latches which operate off alternative clock phases are used to reduce power and enable operation from a low-voltage 1.0V digital supply. The register output is then fed to a digital switch driver circuit also operating off the 1.0V supply.

The driver cells use and-inverter logic connected to the output stage for the complimentary signals that control the switches in the current-source circuit. The P/N MOS device sizes adjust the crossing point of the differential switches, so they are not turned off simultaneously. Consequently, voltage fluctuations are reduced at the output nodes of the current sources. The size of the devices in the driver stage are matched to the switches on the current-source as larger o/p devices were seen to impact the glitch energy due to increased capacitance. Other Swing Reduced Drivers [10, 11] based on a diode circuit were also investigated, however the power consumption was considered too high for this application. A controlled switch voltage of 0~1.0V was used as an input to the current-source switches. Total power measured for the digital supply section was 0.3mW at F_s= 4MHz.

The current-source design consists of cascoded PMOS devices for better output resistance and current stability at the summed output node. PMOS devices located in an isolated NWELL were used to provide better immunity from substrate noise. Thick-oxide HVTH and standard NVTH PMOS devices were analyzed for their output current variation over a 0.5V swing. The plot in Fig 6 shows a significantly reduced current variation of 0.0002uA for the HVTH devices (against 0.04uA for NVTH devices) due to the higher output resistances seen at the switch output. Device W/L sizes were chosen with a balance between the area overhead and calculated current factor mismatch [12] to be less than 2%.
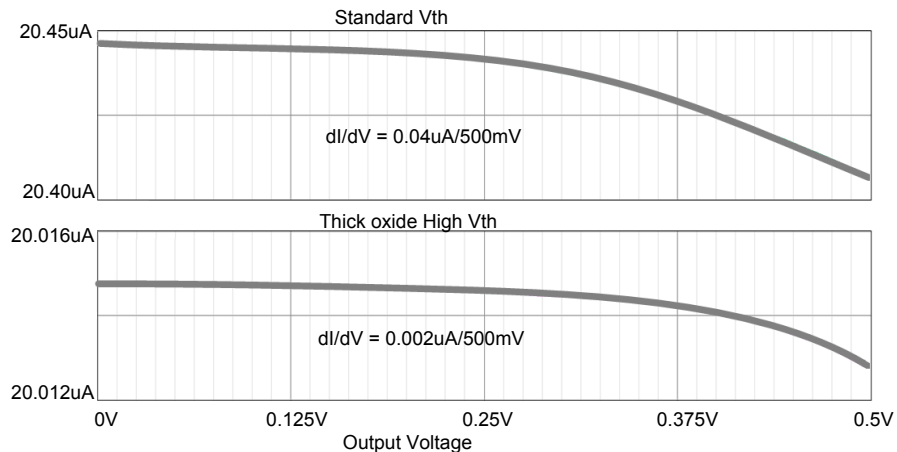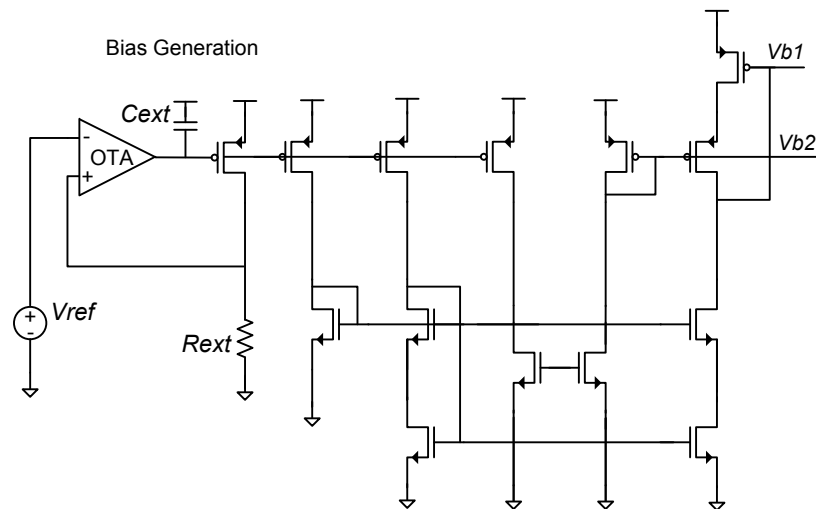

Fig. 6. Current Variation of HVTH PMOS Devices

The switches in the current source cell include a further two dummy transistors to neutralize the feed-through charges. These devices are geometrically the same size as

the switches for matching capacitance. The sources of the dummy devices are floating and follow the gate voltages - hence, they are always off, with no channel formed. The only capacitances are the gate-to-drain overlap capacitors. To ensure cancellation, the switches must operate in either the saturation or the cut-off region.

The analog 1.2V opamp and bias circuit generates the reference voltages to the cascoded current sources, shown in Fig. 7. The op-amp is a folded cascode OTA (operational transconductance amplifier) with gain enhancement to generate an accurate reference current. The op-amp is load compensated with a large external capacitor (Cext) placed on the node Vbp. The negative input terminal of the op- amp is supplied with a fixed voltage reference while the complementary input is connected to the drain of M1. The voltage drop across an external resistor sets the current through M1 while mirroring through MC1 and MC2 connected to the 32 current source cells. Each current source segment delivers 20uA in the 'ON' condition to drive a 0.5V swing into a typical probe load. HVTH transistors are also used in the bias circuitry to match the PMOS devices used in the cascode current source section.

Fig. 7. Opamp and Bias Section

The complete design was developed in Cadence Virtuoso environment using the UMC 90nm technology process. The next section discusses the results including the layout of the design.

4   Measurement and Results

A photograph of the fabricated chip is shown in Fig. 8. The clock-tree, register, and driver circuits functionally operate off a 1.0V or 1.2V supply using standard digital cell design, however customized layouts were used for optimal performance. The total silicon area occupies 0.07sq.mm. The upper design section consists of the digital registers, clock-data buffer tree and driver logic. The lower section shows the current switch and cascode current source matrix. Both the driver section to the current switches and the cascode current source matrix use layout techniques to improve the matching performance such as multiple dummies in the X/Y direction around each active CMOS cells and equal differential signal trace lengths.   The bottom RHS layout contains the op-amp with matched bias cells abutted to the current source matrix. The complete layout combining the 1.0V and 1.2V CMOS sections consumes an average power of 1.7mW during switching operation for a 1MHz tone. The chip was designed with 2.5V pad IOs that interface to an external FPGA which contains the DDS signal generation and modulator/DEM IP. Standard analog IO cells were then used for the VREF, REXT and output current signals. Other IOs for signal measurement were also supported in the standard 68-pin JLCC package.
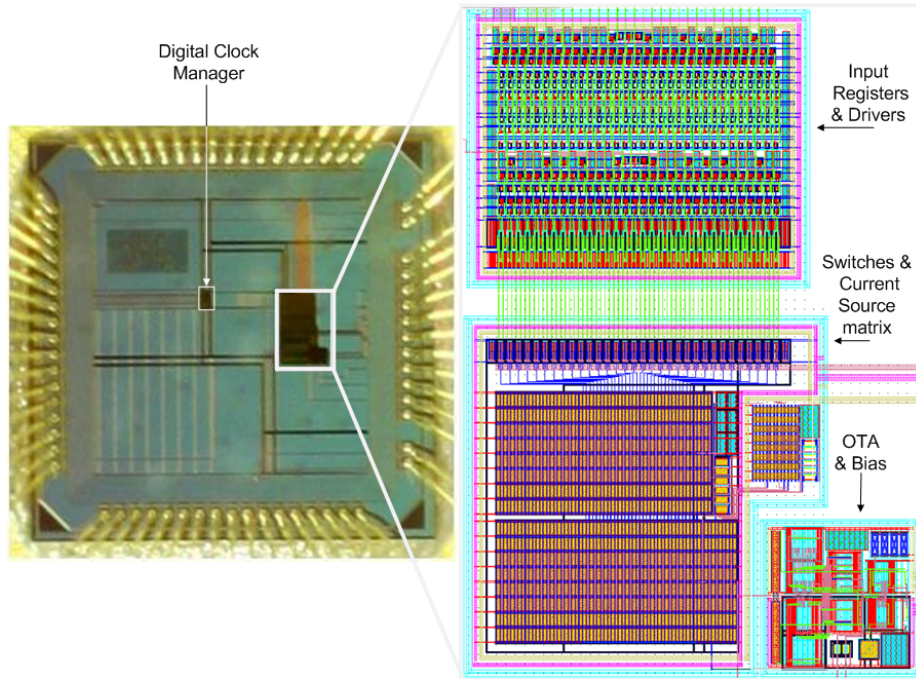

Fig. 8. C-DAC Layout Section

The digital modulator and DEM sections were also synthesized to 1.0V UMC 90nm process generating the results in **Table I.** This shows that our implementation meets the criteria for low voltage, high speed operation capable of generating tones in the low KHz~25MHz range. Power and area overhead are compared for the F_s = 100MHz/ F_c=25MHz tone operation. **Table II** provides a summary overview of the main design parameters.
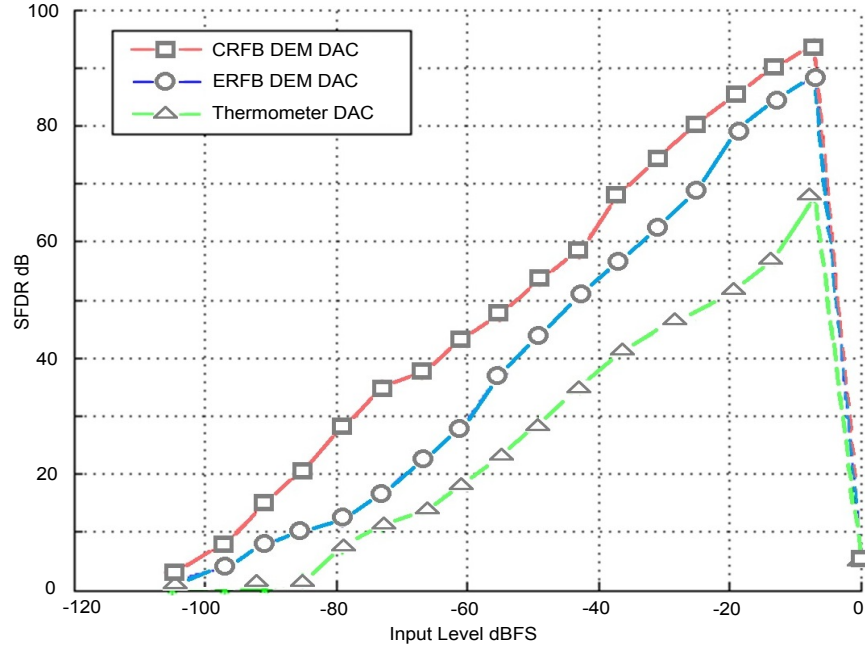
Table 1. UMC90nm Digtial synthesis Results

F_s =100MHz	BCCOM 1.1V/-40°C	TCCOM 1.0V/25°C	WCCOM 0.9V/125°C
Power	17.7mW	15.9mW	14.4mW
Area	320428 Cell units $\approx$ 80K Gates		

Table 2. Band-Pass DAC performance summary

Design Parameters	Extracted Layout
Process	90nm
Supply Voltage	Digital 1.0V
	Analog 1.2V
C-DAC Chip Power Consumption @25°C / F_c=4MHz	Digital 0.3mW
	Analog 1.4mW
C-DAC Chip Size	Digital 0.03mm^2
	Analog 0.04mm^2
90nm Synthesized $\sum\Delta$ +DEM Block Power Consumption	16mW (F_s=100 MHz) 1.4mW (F_s=4 MHz)
Narrow-band SFDR @ F_c =1MHz ±2.5%	110.0dB
Narrow-band SINAD @ F_c =1MHz±2.5%	98.3dB

Due to limitations in the test setup, the current measured SFDR performance of the chip is at 100dB for up to a 1MHz tone. To demonstrate the effectiveness of the 4th order noise shaping, one of the DAC elements is intentionally corrupted to introduce a non-linearity in the C-DAC. Fig. 9 plots the measured SFDR of the 4th order VFB, 2nd order ERFB and thermometer decoded switching scheme with the corrupted DAC element in place. The 4th order VFB DEM achieves on average a 10dB improvement over the conventional 2nd order DEM and a 25dB improvement when compared the thermometer coded DAC.

Fig. 9. SFDR performance of the Band-Pass DAC comparing 4th order DEM, 2nd order DEM and thermometer coded switching schemes.

Table III shows the measured performance for recent comparable CMOS DAC designs [2, 8, 13, 14] that use alternative modulator and DEM schemes. The DAC presented in this work exhibits high DR performance for a narrow bandwidth specification. The DR range was physically measured at 88dB and is lower than the extracted layout simulation results which demonstrated 98dB performance. This loss is due to chip and board noise considerations; nevertheless the 100dB SFDR performance over a narrow bandwidth was confirmed and shows the advantage of a stable 4th order noise-shaper DEM design that provides excellent results when combined with a sigma-delta modulator and current-DAC design.

Table 3. Comparsion to other published DACs

DAC	*Modulator Architecture*	*Shaping DEM scheme*	*Specification DR dB*
Lin [2]	4-bit, 8th order BP	2nd order shuffler	90dB@125KHz
Risbo [8]	6-bit, 3rd order LP	2nd order DWA/1st order ISI	108dB @1KHz
Nguyen[13]	8-bit, 2nd order LP	3-level shuffler	108dB@1KHz
Shui [14]	9-bit, 6th order BP	Modified Mismatch	85dB@125KHz
This work	5-bit, 6th order BP	4th order VFDEM	88dB @ 1MHz

5   Summary

A high-performance narrow-band band-pass DAC suitable for DDS and potential RF applications has been demonstrated to deliver an on-chip 100dB SFDR specification. A digital FPGA and analog DAC chip solution in low-voltage UMC 90nm technology is designed to showcase the potential for generating high performance signals even for low geometry processes where headroom and layout mismatch considerations are increasingly important. Digital DEM calibration using a high 4th order noise shaping Vector Feedback DEM design can operate at high frequencies while keeping area overhead to a minimum. The combined $\sum\Delta$ + DEM + 5-bit C-DAC solution can be fabricated to less than 1.00 sq. mm in 90nm silicon. The analog DAC section was designed for both performance and low-voltage operation and can be easily ported to lower nm CMOS processes such as 65nm and 40nm. The band-pass DAC architecture may also find use in RF transmission systems where large bandwidth and multi-mode operation is a consideration. The design approach enables a FPGA solution to be used for developing further research into other digital calibration techniques. Further research includes developing novel digital assisted analog solutions to reduce the distortion effects of jitter and glitching occurring within the analog section.

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