Application of CPLD in Pulse Power for EDM

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Abstract. In order to improve the precision and surface quality of Electrical Discharge Machining (EDM), the paper studies the application of complex programmable logic device (CPLD) used in pulse power for EDM, according to the characteristics of the device, using VHDL language input and schematic input method to design control circuit for EDM pulse power.

Keyword: EDM; CPLD; VHDL language; pulse power

1 Introduction

EDM is a special processing method, which makes use of the continuous pulse spark discharge generated by two poles in working fluid, relying on each discharge generates partial and instantaneous high-temperature to ablate down metallic material gradually, cutting into necessary shapes, it is also called as discharge machining or electric erosion processing [1]. Pulse power supply as an important part of machine tools of EDM, provides the required breakdown voltage for processing media, and provides energy to ablate metal after breakdown, its performance is well or not will determine the stability of processing equipment and the height of production efficiency [2, 3]. With the development of EDM application technology, the research on technology of pulse power is more and more in-depth.

In the 1980s, it advanced the high and low pressure complex pulse and comb-shaped pulse (pulse group). Subsequent, it advanced the controlled current rising edge pulse and equal energy pulse, and nowadays has proposed to a new technology which can achieve single discharge pulse detection. Now people study of the pulse power variable parameters more refined, parameter adjustment and digital level higher. In this case, if it continues to use discrete components or small and medium-scale integrated circuits as the basic original, obviously doesn't meet the design requirements of power nowadays with high integrated, fast changing, good controllability.

From 80 to 90 during the 20th century made the high and low pressure complex, comb-shaped pulse (pulse packet), the subsequent rising edge of control current, such as the energy pulse, and has proposed to achieve a single discharge pulse detection technology, people Pulse variable parameters of a more detailed, parameter adjustment and further quantify the number of higher degree. In this case, the EDM pulse power supply circuit such as to continue to use discrete components and small and medium-scale integrated circuits as the basic original, obviously does not meet

today's power highly integrated, fast changing, good controllability of the design requirements.

2 Characteristics of CPLD devices

The first programmable logic device - PLD was produced in the 1970s, and it's output structure is programmable logic macrocell, because the design of hardware architecture was completed by the software, which like that workers designed the interior structure after the house completed, so its design is more flexible than pure software on digital circuits. But its structure is too simple so that they only can achieve smaller circuits. To make up for the flaw that PLD only can design small-scale circuit, in the middle of 1980s, the complex programmable logic device was invented– CPLD [4, 5].

With programming flexibility, high integration, design and development period is short, wide scope of application, development tools is advanced, low costs of design and manufacturing, the experience of the designers requirements low, standard products without testing, confidentiality, price moderate, etc, and it can realize large-scale circuit design, so the complex programmable logic device – CPLD is widely used in prototype of product design and production (In general under 10,000 pieces). Almost all the situation where small scale general digital circuits were applied can applied CPLD device. In recent years, because advanced integration process was Adopted, CPLD device was produced in quantity and its costs continue to drop. Integrated density, velocity, and has been greatly improved. And its integrated density, velocity, capability has been greatly improved. Because it has a lot of advantages, such as high reliability, excellent electromagnetic compatibility (EMC) and micro-power consumption, CPLD has been widely used in the field of numerical control. What is particularly important is that CPLD has the function of online programming (ISP) (according to different requirements, just a software re-programming, you can complete the online programming), which makes function update and system debugging more convenient and greatly shorten the product development cycle, also it is great convenience to design and modify.

3 EDM pulse power circuit structure

This pulse power takes CPLD and MOSFET as the core component. Through the programming on the CPLD, it can realize the steering impulse adjustment. This pulse takes the driving of circuit applied to the MOSFET as the power switch, and provides pulse power for the processing circuit. The power schematic is shown in Figure 1.

CPLD can construct digital logic integrated circuits for users' own needs, and it is suitable to be used to realize each kind of operation and combinatory logic. Furthermore, it can achieve large-scale circuit design for its many kinds of characteristics, such as programming flexibility, high integration, advanced develop kit, low design cost and so on. ALTERA's MAXII series chips are high speed and support for the global maximum input clock frequency up to 304 MHz. By using the

chip to carry on the pulse control signal disposition, it can output the disposition information for the external instrumentation, simultaneously may receive the superior information.

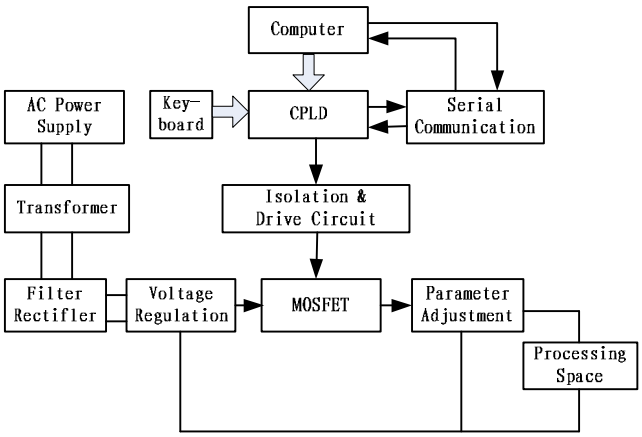

Fig. 1. Schematic diagram of pulse power

4 CPLD devices of control circuit for pulse power design

Pulses control program principle framework is shown in Figure 2. It set the required

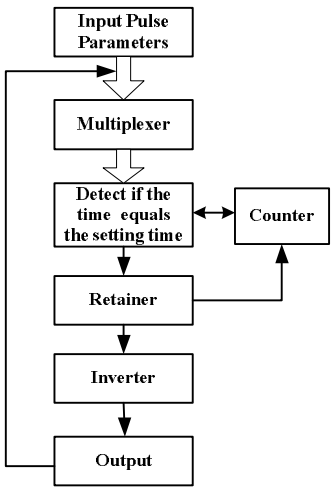

Fig. 2. Pulses control program principle framework

time parameters for pulse high and low, mainly through the multiplexer time-sharing operation to the next level. The multiplexer selection is carried out by the output

adjusting. When time parameters through the multiplexer, it immediately starts the counter to count, and loop checks whether the given parameters are equal. If they are equal, the program sends a corresponding pulse to the retainer, and triggers the inverter for inverting operation. Pulses are from the inverter output.

Pulses control program flow chart is shown in Figure 3. Pulse parameters on-time and off-time represent the pulse width and pulse interval and set by the DIP switch, according to the value of signal sel, put the values of on-time and off-time to variables time-count. If time-count is 0, then signal sel is negated, and sel takes counter-action in the next clock, at the same time take anti-variable temp, and the value assigns to the output signal out-value. If time-count is not 0, then enter the next statement. Every clock cycle, the variable Counter plus one, and compared with the variable time-count. The role of variable Counter is allocating time as a counter with the given pulse parameters. When Counter equals time-count, input signal sel is negated, and initialize the Counter, then take anti-signal temp to output values.

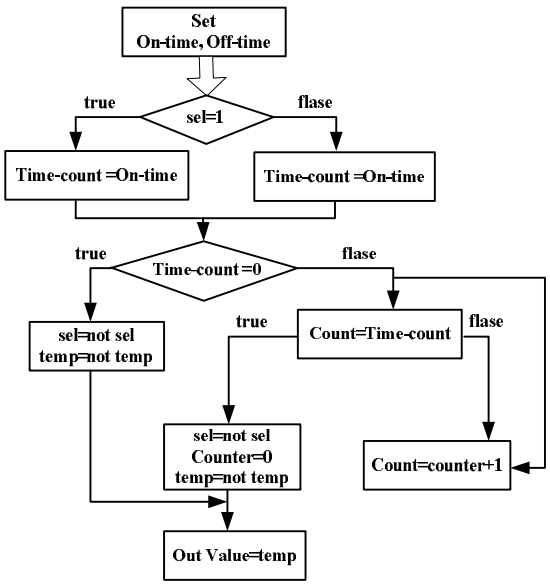

Fig. 3. Pulses control program flow chart

In the VHDL design, two common objects are signal and variable [6], signal is a means of date exchange in the design entity, using signal objects can connect design entity to form module, representative of a hardware circuit in the hardware connection, sometimes the signal will be integrated into register, while variable mainly stores temporary data locally, it is a local variable. Within a process, signal processing is delayed, namely only after the arrival of the next clock for signal processing, but the variable processing is real-time. Therefore, after entering the process, the signal of On-time and Off-time need to be converted to variable form. Variable of Time-Count judging and variable of Count computing are real-time .When Time-Count equals 0, that is, the high pulse or low pulse is a clock cycle, and the program directly jumps out from process. The minimum output pulse increased to a clock cycle by the pulse

entering output value .after using QUARTUSII simulation, waveform is shown in Figure 4.

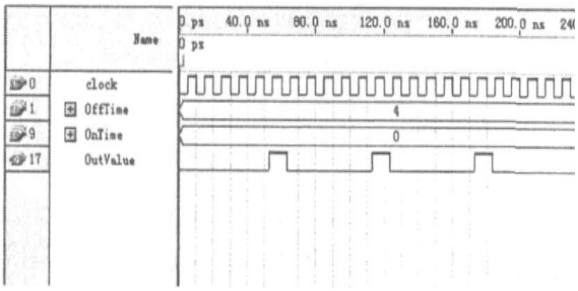

Fig. 4. Pulses width 10ns and inter-pulse 50ns simulation graph

CPLD uses the source crystal oscillator to provide clock pulses, taking into account the conduction ability of MOSFET .we choose 100M crystal which can provide minimum pulse period of 10ns

5 Conclusions

The designed control circuit has many advantages, such as stable performance, strong anti- interference ability, precise pulses, good scalability, fully embodies the characteristics of CPLD devices.

The CPLD devices applied to the design of EDM pulse power, improved the flexibility of circuit design, reduced PCB area, increased power system reliability, shortened product development cycle, and reduced design costs and application costs, it can meet the increasingly complex electronic processing equipment control circuit applications.

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