A DC-DC Step-Up μ-Power Converter for Energy Harvesting Applications, Using Maximum Power Point Tracking, Based on Fractional Open Circuit Voltage

Carlos Carvalho, Guilherme Lavareda, Nuno Paulino

A DC-DC Step-up μ-Power Converter for Energy Harvesting Applications, using Maximum Power Point Tracking, Based on Fractional Open Circuit Voltage

Carlos Carvalho[1], Guilherme Lavareda[2], Nuno Paulino[3]

[1] Instituto Superior de Engenharia de Lisboa (ISEL – ADEETC), Instituto Politécnico de Lisboa (IPL), Rua Conselheiro Emídio Navarro, nº1, 1949-014 Lisboa, Portugal, cfc@isel.ipl.pt

[2] Departamento de Ciências dos Materiais e UNINOVA/CTS, Faculdade de Ciências e Tecnologia, Universidade Nova de Lisboa, Campus FCT/UNL, 2829-516 Caparica, Portugal, gal@fct.unl.pt

[3] UNINOVA/CTS, Departamento de Engenharia Electrotécnica, Faculdade de Ciências e Tecnologia, Universidade Nova de Lisboa, Campus FCT/UNL, 2829-516 Caparica, Portugal, nunop@uninova.pt

Abstract. A DC-DC step-up micro power converter for solar energy harvesting applications is presented. The circuit is based on a switched-capacitor voltage tripler architecture with MOSFET capacitors, which results in an area approximately eight times smaller than using MiM capacitors for the 0.13μm CMOS technology. In order to compensate for the loss of efficiency, due to the larger parasitic capacitances, a charge reutilization scheme is employed. The circuit is self-clocked, using a phase controller designed specifically to work with an amorphous silicon solar cell, in order to obtain the maximum available power from the cell. This will be done by tracking its maximum power point (MPPT) using the fractional open circuit voltage method. Electrical simulations of the circuit, together with an equivalent electrical model of an amorphous silicon solar cell, show that the circuit can deliver a power of 1132 μW to the load, corresponding to a maximum efficiency of 66.81%.

Keywords: Electronics, CMOS circuits, Energy Harvesting, Power management circuits, Maximum Power Point Tracking, Amorphous Silicon Solar Cell.

1 Introduction

There is an emerging need to power applications in an autonomous fashion. This need results from the fact that it may not be practical to plug the device to the power grid, nor to use batteries, as they need to be replaced when their charge is depleted. A solution to this problem, that is being increasingly used, is to power the application by collecting the energy that exists in the surrounding environment; this

is known as energy harvesting, or energy scavenging, and has been growing in importance. By employing energy harvesting, circuits can virtually operate permanently. As such, there is no need to plug the circuit to the power grid, or to power it by using batteries.

Energy can be harvested from different sources: light (solar [1], [2] or artificial [3]), mechanical [2] (usually vibrations), thermal gradients [2], or electromagnetic [1]. Each of these energy sources has its own advantages and drawbacks, but they all share a common limitation, which is low energy density. This means that the available power for a small energy harvesting powered system will be limited. Amongst of all, ambient light has the highest energy density when compared to other possible ambient energy sources [1]. The power and the voltage produced by a solar cell vary with the connected load and with the amount of incident light. Thus, it is necessary to increase the voltage supplied by a single solar cell to an acceptable value by most circuits (at least, 1 V). So, it is necessary to use a step-up power converter circuit, which in this paper, is based on a switched-capacitor voltage tripler architecture, using 0.13μm CMOS technology MOSFET capacitors. This circuit uses an asynchronous state machine to produce a variable frequency clock, regulating the input voltage of the converter (output of the solar cell) to a nearly constant value, corresponding to the maximum power point (MPP). The objective is to dynamically adjust the working input voltage to the MPP voltage value. The output voltage value is maximized when this occurs. This step-up converter circuit tries to harvest as much energy as possible out of the solar cell using a maximum power point tracking (MPPT) approach. There are many MPPT approaches, varying with the availability of resources and the intended application [4]. Amongst these approaches, the Fractional Open Circuit Voltage (Fractional V_{OC}), is the one used in this work.

The research question associated to this work, is if it is possible to join an a-silicon solar cell to a voltage tripler and an MPPT method, and to get a reasonable efficiency performance. The hypothesis for such a combination is explored in the present paper.

2 Contribution to Sustainability

As the purpose of this system is based on energy harvesting, it can operationally contribute for environmental sustainability. The energy used to power the circuit and the energy that the converter provides, besides being non-polluting, it is also free. Moreover, by excluding the use of batteries, there is no need to dispose them of, avoiding additional pollution, nor the use of additional chemicals than those used to manufacture the circuit itself.

3 Novel Results, Contributing to Technological Innovation

The work described in this paper is a fundamental block of a self-powered system using energy harvesting, to be implemented in 0.13 μm CMOS technology. There are some innovative aspects in the present work, which include the use of cheaper

solar cells (made from amorphous silicon), the combination of NMOS and PMOS devices to implement a voltage step-up regulator and the use of a local supply module to power a phase generator. This local supply strategy allows for a more robust command over the switches in the main step-up converter section.

The ability of being self-powered is very important for electronic systems that are intended to monitor and gather information, in locations where it is difficult or even impractical, to obtain energy by normal methods. In such inaccessible places, an energy independent system, with low installation and operation costs, enhances the benefits of the energy harvesting facet, widening or even opening new possibilities of applications.

4 Electrical Model of the Amorphous Silicon Solar Cell

An a-Silicon photovoltaic cell was built by depositing amorphous silicon with a structure p/i/n on a glass previously covered with ITO (Indium Tin Oxide). The ITO was deposited using rf-PERTE (radio-frequency Plasma Enhanced Reactive Thermal Evaporation) and had a sheet resistance of 35 Ω/□. The active p-type, intrinsic and n-type layers were deposited using PECVD (Plasma Enhanced Chemical Vapor Deposition) and had a thickness of 150Å, 4500Å and 500Å respectively. The frontal aluminum electrode was deposited using thermal evaporation [5]. The solar cell was experimentally characterized and an equivalent electrical model, shown in Fig. 1-a), was obtained.

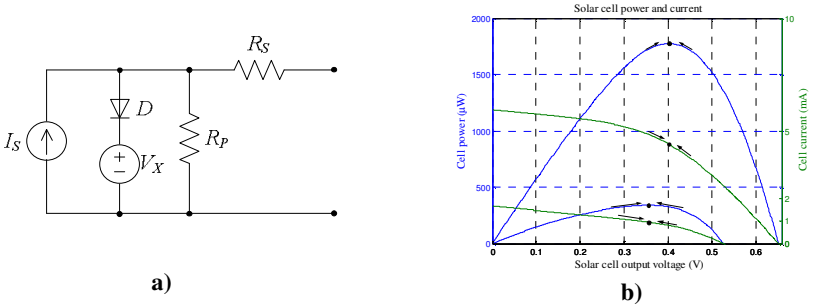


Fig. 1. a) Equivalent electrical circuit of the amorphous silicon solar cell and **b)** Power and current curves of the solar cell equivalent circuit model for maximum illumination and 30% of maximum illumination (higher and lower curves, respectively).

This solar cell has a short circuit current of about 5.9 mA, a maximum power of 1775 μW that occurs for a voltage of 403 mV (maximum power point) and an open circuit voltage of 652 mV. These data refer to a cell having an active area of about 1 cm^2, when irradiated according to AM1 (Air Mass 1) conditions (irradiance by the solar spectrum at the earth surface, having the Sun vertically located). The resulting power and current curves of the cell are depicted in Fig. 1-b).

Since the MPP voltage is small (around 400 mV) a SC voltage tripler circuit must be used in order to obtain an output voltage value around 1.1V. The impedance that this circuit presents to the solar cell must be adjusted in order for the solar cell voltage to become approximately equal to the MPP voltage.

5 Maximum Power Point Tracking, Based on Fractional Open Circuit Voltage

There are several methods available to track the maximum power point (MPP) of a solar cell [4], in order to achieve efficiencies as high as possible. Some of these methods can track the true MPP of the cell; however they typically require complex circuits or computational effort, namely the ability to perform multiplications. If some inaccuracy in the determination of the MPP is accepted, it is possible to use simpler methods that require less complex circuits. In this application where the total available power is very low, these simpler methods can be preferable. As such, the Fractional Open Circuit Voltage (Fractional V_{OC}) method was chosen, because it is a very simple and inexpensive (hardware wise) method. This method explores an intrinsic characteristic of cells: there is a proportionality factor between their open circuit voltage and the voltage at which the MPP occurs. This factor must be determined beforehand, by studying the solar cell behavior under several conditions of illumination and temperature. By performing a linear regression over the points plotted on the obtained graphs, the same way as in [6], one can determine the slope of these functions. By sweeping a range of temperatures that spanned from –55ºC to +125ºC, the ratio V_{MPP}/V_{OC} was around 0.84. By sweeping illumination, the ratio V_{MPP}/V_{OC} was around 0.76. Assuming that illumination has more importance, as it is more likely to vary, a value of 0.77 was selected for k, the fractional V_{OC} coefficient. This value agrees with the ones stated in [4].

A pilot solar cell that is in open circuit (unloaded), is used to measure the open circuit voltage. The optimum voltage of the loaded solar cell (MPP), is determined by multiplying the open circuit pilot voltage by k, using a resistive divider. This voltage is known as the fractional V_{OC}. Resistors must be high enough to preserve the open circuit assumption for the pilot cell. The pilot solar cell can be smaller than the main solar cell and it must have the same temperature and illumination as the main cell, in order for the fractional V_{OC} to accurately track the MPP voltage. The MPP tracking is implemented by adjusting the switching frequency of the SC voltage tripler. When the fractional V_{OC} is larger than the solar cell voltage this means that the impedance of the SC circuit is small and therefore it is necessary to decrease the switching frequency in order to increase the impedance, thus increasing the solar cell voltage. If the V_{OC} voltage is smaller than the solar cell voltage, it is necessary to increase the switching frequency in order to decrease the impedance of the SC circuit and therefore decrease the solar cell voltage. This process will result in a switching frequency value that allows the SC voltage tripler circuit to have an impedance value that causes the MPP voltage in the solar cell, as illustrated by the arrows in the graph depicted in Fig. 1-b).

6 Switched Capacitor Voltage Tripler Circuit with Charge Reusing

The circuit of the SC DC-DC converter is shown in Fig. 2. The principle of operation of this circuit is the same of the switched-capacitor voltage tripler [7]. During phase ϕ_1, the MOS capacitors of the upper half circuit, M_1 and M_3, are charged with the

input voltage value (v_{in}) and then, during phase ϕ_3, they are connect in series with the input voltage source.

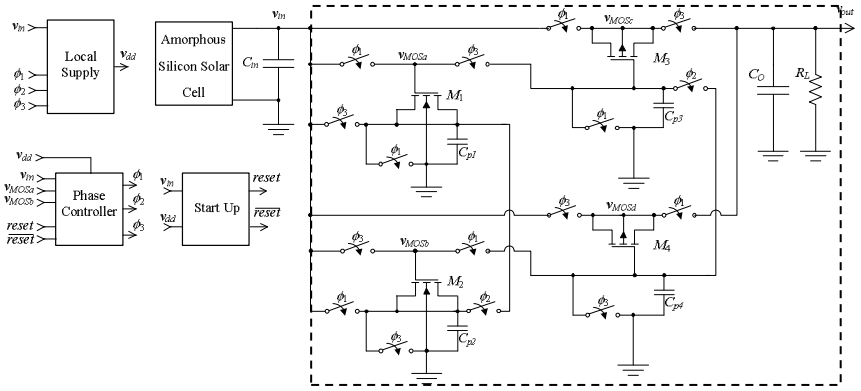


Fig. 2. Schematic of the SC voltage tripler circuit with charge re-utilization.

If there were no losses, this would result in an output voltage (v_{out}) approximately three times larger than the input voltage value. Although using MOS capacitors instead of MiM capacitors results in a significant reduction of the occupied area, there is also an increase in the parasitic capacitances of the bottom plate nodes, leading to a decrease in the efficiency of the circuit. In order to reduce the amount of charge lost in these parasitic capacitances, the circuit is split into two halves. The top half is composed by M_1 and M_3 and the bottom half is composed by M_2 and M_4. The bottom half works in the same way as the top half, with phase ϕ_1 changed with phase ϕ_3. During an intermediate phase (ϕ_2), the bottom plate nodes of both MOS capacitors of the upper and lower half-circuits are connected together, thus transferring half of the charge in one parasitic capacitance to the other, before the bottom nodes are shorted to ground. This reduces by half the amount of charge that is lost in the parasitic capacitance nodes. The clock phases are generated by the phase controller circuit that will be described next. The output voltage of the circuit depends on the value of the load resistance (R_L). This means that this voltage cannot be used to power the phase generator. Therefore, a smaller SC voltage tripler, controlled by the same clock, is used to create a local power supply. This circuit is a replica of the one inside the dashed rectangle in Fig. 2, but scaled to 3% of its area, as this ratio yielded the best results.

7 Phase Generation and Control

The three clock phases necessary for the operation of the SC voltage tripler circuit are generated by an ASM circuit that automatically adjusts the clock frequency in order to obtain the MPP voltage from the solar cell. This circuit is depicted next in Fig. 3. The operation of this circuit is similar to the one described in [8]. This circuit has four states that are determined by the output of four latches. These states correspond to the clock phases ϕ_1, ϕ_2, ϕ_3, and again ϕ_2. In order to change from one

state to the next, the *Set* signal of one latch is activated, changing the output of that latch from 0 to 1. This, in turn, activates the *Reset* signal of the previous latch, causing its output to change from 1 to 0, thus completing the state change.

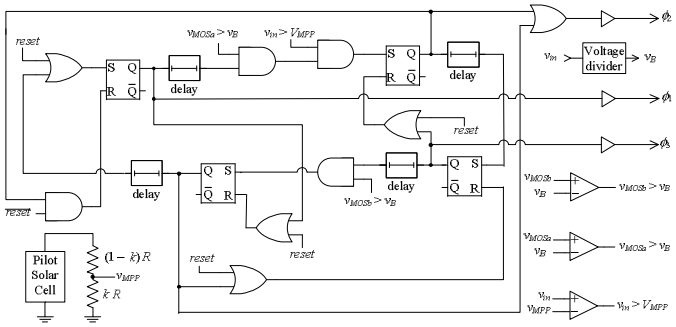


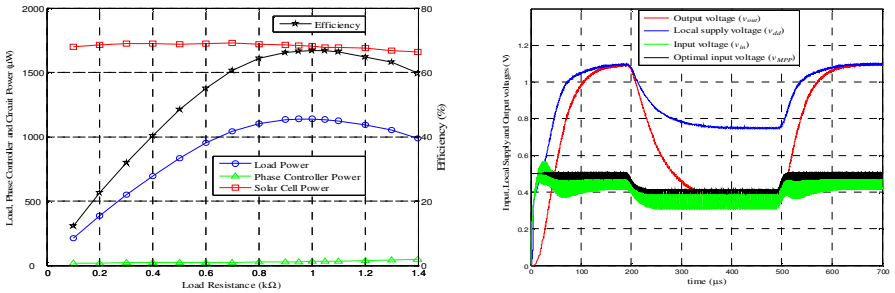
Fig. 3. Phase controller schematic.

A start-up circuit (described in [8]) generates a *reset* signal that guarantees that the first state is state1. The ASM is continually changing from one state to the next (and then from state4 to state1), in order to create the clock phases. The maximum frequency of operation is defined by the delay circuits (described in [8]) inserted between the output of each latch and the *Set* input of the next latch. The transitions between state, state2, state3 and state4 are delayed by comparators that guarantee that the MOS capacitors connected to the solar cell are charged to at least 95% of the input voltage (V_{MOSa}>v_B and V_{MOSb}>v_B). The duration of state1 (phase ϕ_1) is also dependent on the comparison between the solar cell voltage (v_{in}) and the fractional V_{OC}, obtained from the pilot solar cell (v_{MPP}). When the capacitors are connected to the solar cell (in the beginning of ϕ_1), the voltage v_{in} drops a little. The time it takes to recover to its previous value, and the fractional V_{OC}, depends on the temperature and illumination. Therefore the duration of the period corresponds to the frequency value that adjusts the input voltage to the MPP voltage value.

8 Simulation Results

This step-up converter was designed to work with an amorphous solar cell, with an area of about 1 cm^2, able to supply a maximum power of 1775 µW, at a MPP voltage of 403 mV. The efficiency and power values of the circuit for different load resistance values obtained through electrical simulations in Spectre, are shown in Fig. 4-a). This graph shows that when the load resistance is 1.05kΩ, the maximum efficiency of the circuit is 66.81%, for a power delivered to the load of 1132 µW and a solar cell power of 1694 µW. In this situation, v_{in} converged to 450 mV. This value does not match the optimal input voltage of 403 mV, because the Fractional V_{OC} method may not reach the true MPP voltage, as it depends upon k, which is an average value obtained from the studied situations taken beforehand. This problem is not very important since the power available from the cell does not change significantly around the MPP voltage. From a theoretical point of view, as stated in [7], the maximum achievable efficiency of an ideal converter with an input voltage of

450 mV and an output voltage of 1.090 V (which was the value of v_{out} in this situation) would be 80.74%.



a) **b)**

Fig. 4. a) Efficiency, input power, output power and phase controller circuit power as a function of the power delivered to load and **b)** Evolution of v_{in}, v_{dd}, v_{out} and v_{MPP}, during start-up and transient operation (lower illumination between 200 and 500μs).

In this situation, the phase generator circuit dissipates 32.47 μW. The frequency of the clock phase ϕ_1 in this load condition is 1.245 MHz. In order to determine how much is the efficiency penalty by using MOS transistors, instead of MiM capacitors, a simulation where the MOS transistors were replaced by MiM capacitors of the given technology was performed. In this case the maximum efficiency increased to 74.59%, which is not significant, given the die area tradeoff. The evolution of the input, local supply, output and optimal input voltages, during start-up (and transient operation), is shown in Fig. 4-b).

Electrical simulations showed that the system can converge, in order for the cell to provide the voltage at which the MPP is achieved. This system can start-up with loads starting as low as 100Ω. It is possible to have such a significant load connected to the output during start-up because the load of the local supply module is not very significant, allowing for the phase controlling signals to be correctly defined.

In order to check the robustness of the MPP tracker circuit when experiencing a sudden illumination change, Fig. 4-b) also shows how the circuit behaves under a irradiance-transient operation, when illuminated by 100% and 30% of the maximum value. It is seen that the circuit is able to track the optimal input voltage in both situations. Clock signal ϕ_1 decreases its frequency when a lower irradiance level is present, because the amount of available charge from the solar cell is also lower.

9 Conclusions

A step-up micro-power converter for solar energy harvesting applications was presented. The circuit is based on a switched-circuit voltage tripler architecture, with MOSFET capacitors of the 0.13 μm CMOS technology, which results in a total circuit area approximately eight times smaller than using MiM capacitors of the given technology. In order to compensate for the loss of efficiency due to the larger parasitic capacitances, a charge reutilization scheme was employed. The circuit uses a phase controller, designed specifically to work with an amorphous solar cell, in order

to track the MPP of the cell, using the fractional V_{OC} method. To implement this method, a previous study of the cell characteristics must be carried out, regarding illumination and temperature. The controller is powered by a local supply circuit to ensure that the phase signals that control the main switches are well defined. Electrical simulations of the circuit together with an equivalent electrical model of the amorphous solar cell, have shown that the circuit can deliver a power of 1132 μW to the load and a total circuit power dissipation of 1694 μW, corresponding to a maximum efficiency of 66.81%. This efficiency value is similar to the one obtained in [9], meaning that the hypothesis proposed in this paper is able to meet the requirements formulated in the research question. When using the MiM capacitors of the 0.13 μm CMOS technology, the increase of efficiency to 74.59% is not significant, considering the eight times less die area tradeoff. When the solar cell experiences irradiance variations, the phase controller circuit can effectively track the MPP, as it shifts from its previous value.

Acknowledgments. This work was supported by the Portuguese Foundation for Science and Technology (FCT/MCTES) (CTS multiannual funding) through the PIDDAC Program funds.

References

1. Chalasani, S.; Conrad, J.M., "A survey of energy harvesting sources for embedded systems," Southeastcon, 2008. IEEE , vol., no., pp.442-447, 3-6 April 2008.
2. Paradiso, J.A.; Starner, T., "Energy scavenging for mobile and wireless electronics," Pervasive Computing, IEEE , vol.4, no.1, pp. 18-27, Jan.-March 2005.
3. Hande, A.; Polk, T.; Walker, W.; Bhatia, D., "Indoor solar energy harvesting for sensor network router nodes," Microprocessors and Microsystems, Vol. 31, No. 6. (01 September 2007), pp. 420-432.
4. Esram, T.; Chapman, P.L., "Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques,", *IEEE Transactions on Energy Conversion*, vol.22, no.2, pp.439-449, June 2007
5. Amaral, A.; Lavareda, G.; Nunes de Carvalho, C.; Brogueira, P.; Gordo, P.M.; Subrahmanyam, V.S.; Lopes Gil, C.; Duarte Naia, V; de Lima, A. P., "Influence of the a-Si:H structural defects studied by positron annihilation on the solar cells characteristics", Thin Solid Films, vol. 403–404, pp. 539–542, 2002.
6. Brunelli, D.; Moser, C.; Thiele, L.; Benini, L., "Design of a Solar-Harvesting Circuit for Batteryless Embedded Systems," IEEE Transactions on Circuits and Systems – I: Regular Papers, vol.56, no.11, pp.2519-2528, November 2009
7. Zhu, G. & Ioinovici, A. (1996), Switched-capacitor power supplies: DC voltage ratio, efficiency, ripple, regulation, *in* 'Proc. IEEE International Symposium on Circuits and Systems ISCAS '96., 'Connecting the World", pp. 553-556.
8. Carvalho, Carlos; Paulino, Nuno; "A MOSFET only, step-up DC-DC micro power converter, for solar energy harvesting applications" *Mixed Design of Integrated Circuits and Systems (MIXDES), 2010 Proceedings of the 17th International Conference*, pp.499-504, 24-26 June 2010.
9. Hui Shao; Chi-Ying Tsui; Wing-Hung Ki, "The Design of a Micro Power Management System for Applications Using Photovoltaic Cells With the Maximum Output Power Control," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol.17, no.8, pp.1138-1142, Aug. 2009.