CMOS Fully Differential Feedforward-Regulated Folded Cascode Amplifier

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Abstract. A fully differential self-biased inverter-based folded cascode amplifier which uses the feedforward-regulated cascode principle is presented. A detailed small-signal analysis covering both the differential-mode and the common-mode paths of the amplifier is provided. Based on these theoretical results a design is given and transistor level simulations validate the theoretical study and also demonstrate the efficiency and usefulness of the proposed amplifier.

Keywords: fully differential amplifiers, feedforward-regulated cascode technique, self-biasing, inverter-based, CMOS analog integrated circuits.

1 Introduction

Amplifiers are essential building blocks used frequently to build feedback networks able to perform a variety of accurate functions, e.g. multiplication, addition, integration, inversion, etc. The accuracy of these operations is directly dependent on the amplifier's gain-bandwidth product (GBW) performance [1].

Dictated by the down scaling of the digital circuits, the CMOS technology evolved posing several obstacles to the analog circuits design in general and in particular to the amplifiers design. Some of these obstacles are low intrinsic gain (g_m/g_{ds}) of transistors, reduced supply voltages, high variability of devices, etc., which inevitably deteriorate the performance of the well-known amplifier topologies. To cope with this problem some existing amplifier topologies have been enhanced and novel topologies have been proposed, some recent examples are [2]-[4].

In this paper we propose a fully differential self-biased inverter-based folded cascode amplifier which uses the feedforward-regulated cascode principle firstly presented in [4]. First, the small-signal behavior of the topology is analyzed in detail. After, a design is outlined and transistor level simulations are presented to demonstrate the efficiency of the proposed new topology. Finally, the main conclusions are drawn.

2 Contribution to Sustainability

A new self-biased inverter-based transconductance amplifier topology using feedforwad-regulated cascode devices is presented. The combination of these features allows the topology to achieve an attractive figure of merit (FoM = GBW·C_L/Power), which is comparable or better to those of the best amplifiers up to date. This enhanced bandwidth to power dissipation efficiency is interesting for high speed and low power applications to be realized in deep-submicron CMOS technology nodes (≤ 0.13-μm).

3 Amplifier Description and Analysis

3.1 Circuit Description

The circuit of the proposed amplifier without common-mode (CM) feedback (CMFB) circuitry is shown in Fig. 1. The input stage is composed of transistors M_1, M_4, $M_{2a\text{-}b}$, and $M_{3a\text{-}b}$, where $M_{2a\text{-}b}$ and $M_{3a\text{-}b}$ are responsible for converting input voltage variations in incremental drain currents which are then "folded" to the output cascode devices. These currents are converted to incremental voltages in nodes $v_{D2a\text{-}b}$ and $v_{D3a\text{-}b}$, and these voltages are used to drive cascode transistors $M_{6a\text{-}b}$ and $M_{7a\text{-}b}$ in a feedforward fashion as proposed in [4]. For this reason the topology is named feedforward-regulated folded cascode. An interesting advantage of the feedforward-regulated cascode topology over the well-known feedback-regulated cascode one is the faster cascode regulation, which leads to a higher operation speed [4]. The inverter-based inputs of the amplifier effectively double the input g_m compared to single-transistor inputs, which can be used favorably in attaining high GBW.

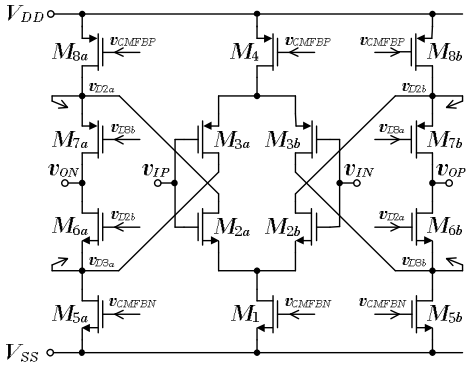

Fig. 1. Electrical schematic of the proposed amplifier (CMFB circuitry not shown).

The extra (self) biasing voltages v_{CMFBN} and v_{CMFBP}, which are also used to adjust the output CM voltage, are obtained from the circuit depicted in Fig. 2. This circuit performs two functions: 1) it averages the output voltage obtaining $v_{CMFB} = (v_{OP} + v_{ON})/2 \equiv v_{CMO}$; 2) in the sequence, it level-shifts this voltage down, resulting in v_{CMFBN}, and up, resulting in v_{CMFBP}. These voltage level-shifts are needed to bias transistors M_1, M_4, $M_{5a\text{-}b}$ and $M_{8a\text{-}b}$ in the saturation region without sacrificing considerably the output voltage swing. For example, assuming V_{DD} = 1.2 V, V_{SS} = 0

V, and V_{CMO} = 0.6 V, the $|V_{DS}|$ (drain-source voltage) of the aforesaid transistors should be greater than 0.3 V to saturate these transistors in a technology with a $|V_{TH}| \approx 0.3$ V (threshold voltage). As a result, 50 % of the rail-to-rail voltage is consumed, which is not desirable. Regarding the averaging circuit, the value of the resistors should be sufficiently large in order not to lower the output impedance, and hence the gain. Unfortunately, large resistor values mean large silicon area, and, if this is prohibitive, other CMFB circuitry, depending on the application, can be used (e.g., switched-capacitor CMFB, differential difference amplifier CMFB, etc.). It is important to remark that besides the rail voltages (V_{DD} and V_{SS}) no additional biasing voltages are required, i.e., the amplifier is completely self-biased. This feature precludes the use of an explicit biasing circuit, saving power consumption and silicon area.

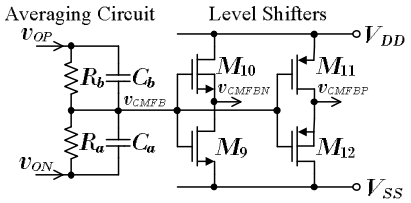

Fig. 2. Electrical schematic of the CMFB circuitry.

3.2 Circuit Analysis

The small-signal differential-mode (DM) analysis is carried out with the equivalent half-circuit shown in Fig. 3 (a). Here C_L represents an output capacitive load. The small-signal model used for all MOS transistors is illustrated in Fig. 3 (b).

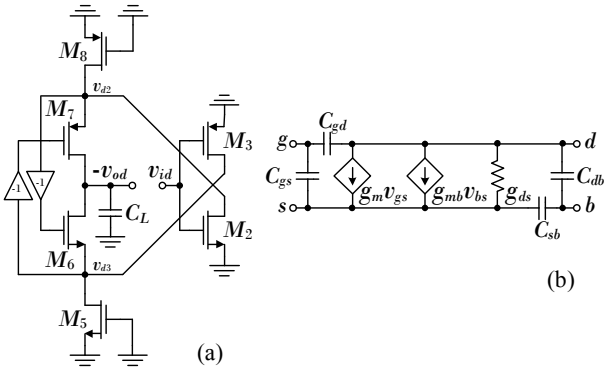

Fig. 3. Small-signal DM half-circuit of the amplifier (a) and MOS transistor model (b).

By considering a "perfect" symmetry, that is, the small-signal parameters of transistors M_2, M_5, and M_6 identical to those of M_3, M_8, and M_7, respectively, the following input-output transfer function results:

$$\frac{V_{od}}{V_{id}} = \frac{2(sC_{gd2} - g_{m2})(sC_{gd6} - g_{eq1})}{C_{eq1}C_{eq2}s^2 + [C_{eq1}(g_{eq1} + g_{ds2} + g_{ds5}) + 2g_{ds6}(C_{eq2} + C_{gd6})]s + 2g_{ds6}(g_{ds2} + g_{ds5})} \quad (1)$$

where $g_{eq1} = 2g_{m6} + g_{mb6} + g_{ds6}$, $C_{eq1} = C_L + 2C_{gd6} + 2C_{db6}$, and $C_{eq2} = C_{gd2} + C_{db2} + C_{gd5} + C_{db5} + 2C_{gs6} + C_{sb6}$. It is important to mention that, besides the two poles and two zeros present in (1), a pole-zero doublet occurs between the dominant and nondominant poles. With the symmetry assumption, this doublet is perfectly canceled out. If we consider the dominant pole angular frequency ω_d much lower than that of the nondominant pole ω_{nd}, expressions for these poles can be derived from (1) as follows [5]:

$$\omega_d = \frac{2g_{ds6}(g_{ds2}+g_{ds5})}{C_{eq1}(g_{eq1}+g_{ds2}+g_{ds5})+2g_{ds6}(C_{eq2}+C_{gd6})} \approx \frac{2g_{ds6}(g_{ds2}+g_{ds5})}{C_{eq1}(g_{eq1}+g_{ds2}+g_{ds5})} \tag{2}$$

and

$$\omega_{nd} = \frac{C_{eq1}(g_{eq1}+g_{ds2}+g_{ds5})+2g_{ds6}(C_{eq2}+C_{gd6})}{C_{eq1}C_{eq2}} \approx \frac{g_{eq1}+g_{ds2}+g_{ds5}}{C_{eq2}} \ . \tag{3}$$

The low-frequency (DC) gain is given by:

$$A_{dc} = \left(1+\frac{2g_{m6}}{g_{ds6}}+\frac{g_{mb6}}{g_{ds6}}\right)\left(\frac{g_{m2}}{g_{ds2}+g_{ds5}}\right) \ . \tag{4}$$

It is important to note that bulk-source transconductances g_{mb} of transistors $M_{6a\text{-}b}$ and $M_{7a\text{-}b}$ increase the gain. Therefore, it is recommended not to eliminate the body-effect of these transistors, even though this is possible in most modern CMOS technologies. Also from (1) we see the transfer function has two right-half plane zeros. In practice, these zeros are at relatively high frequencies and can be neglected. The maximum GBW for this amplifier, considering a phase margin of about 65°, i.e. the nondominant pole located at a frequency twice the GBW [1], is $\omega_{nd}/(2*2\pi)$ hertz.

We now analyze the small-signal common-mode behavior. For this purpose, we consider the equivalent circuit shown in Fig. 4, where it is assumed ideal averaging circuit as well ideal level shifters. One important requisite for the CM path is to have sufficient bandwidth (generally equal or greater than that of the DM path [6]) and good phase margin to not deteriorate the DM performance. It is also desirable a moderate DC gain to stabilize the output CM voltage with some accuracy.

By visual inspection, we see that the overall transfer function (V_{cmo}/V_{cmfb}) of the circuit in Fig. 4 is of fifth order, since it has five signal nodes, excluding the input. It is now clear why, for simplicity, we made ideal both the averaging circuit and the level shifters (otherwise the transfer function would be of seventh order and hardly manageable). Also, if desirable, the influence of these circuits can be included a posteriori. Considering symmetrical devices, i.e., transistors M_1, M_2, M_5, and M_6 identical to M_4, M_3, M_8, and M_7, respectively, two perfectly matched doublets arise and the system reduces to "third" order. In this case the transfer function is given by:

$$\frac{V_{cmo}}{V_{cmfb}} \approx \frac{\begin{array}{c}2(2C_{gd6}s+g_{eq2})\{2C_{gd5}C_{eq3}s^2+[(C_{gd1}+2C_{gd5})g_{eq1}+2(C_{gd5}g_{ds1}-g_{m5}C_{eq3})]s \\ -2g_{m5}(g_{eq1}+g_{ds1})-g_{m1}g_{eq1}\}\end{array}}{\begin{array}{c}C_{eq1}C_{eq2}C_{eq3}s^3+[(g_{eq2}+2g_{ds2}+2g_{ds5})C_{eq3}+(g_{eq1}+g_{ds1})C_{eq2}]C_{eq1}s^2 \\ +(g_{eq2}+2g_{ds5})(g_{eq1}+g_{ds1})C_{eq1}s+8g_{ds6}[g_{ds5}(g_{eq1}+g_{ds1})+g_{ds1}g_{ds2}]\end{array}} \ , \tag{5}$$

where $g_{eq1} = 2(g_{m2} + g_{mb2} + g_{ds2})$, $g_{eq2} = 2(g_{mb6} + g_{ds6})$, $C_{eq1} = 2C_L + 4C_{db6}$, $C_{eq2} = 2(C_{gd2} + C_{db2} + C_{gd5} + C_{db5} + C_{gd6} + C_{sb6})$, and $C_{eq3} = C_{gd1} + C_{db1} + 2(C_{gs2} + C_{sb2})$. This transfer function is approximated because the sum of products terms multiplying the complex frequency "*s*" powers in the denominator are somewhat simplified; however, each term has a simplification error no greater than 1 % for typical parameter values.

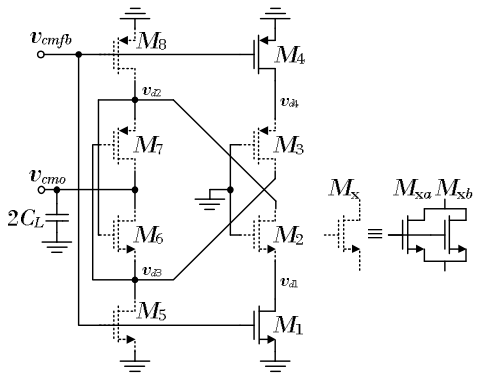

Fig. 4. Small-signal CM equivalent circuit considering ideal averaging circuit and level shifters.

Considering a dominant-pole behavior, i.e. the frequency of the first pole much lower than the remaining ones, the dominant pole can be derived from (5) as:

$$\omega_{d,cm} = \frac{8g_{ds6}[g_{ds5}(g_{eq1} + g_{ds1}) + g_{ds1}g_{ds2}]}{(g_{eq2} + 2g_{ds5})(g_{eq1} + g_{ds1})C_{eq1}} \approx \frac{8g_{ds6}g_{ds5}}{(g_{eq2} + 2g_{ds5})C_{eq1}} \quad . \tag{6}$$

Since the nondominant (second) pole is not far away from the third pole, it can not be derived using an approach similar to that used for the dominant one. Therefore, a different approach [7] is used to approximate this pole (with an error lower than 10 %) resulting in:

$$\omega_{nd,cm} = \frac{1.6(g_{eq2} + 2g_{ds5})(g_{eq1} + g_{ds1})}{(g_{eq2} + 2g_{ds2} + 2g_{ds5})C_{eq3} + (g_{eq1} + g_{ds1})C_{eq2}} - \frac{0.045[(g_{eq2} + 2g_{ds2} + 2g_{ds5})C_{eq3} + (g_{eq1} + g_{ds1})C_{eq2}]}{C_{eq2}C_{eq3}}. \tag{7}$$

Similar to the DM path, this nondominant pole will dictate the maximum CM GBW for a given stability (phase margin). Hence, expressions (3) and (7) play a crucial role in the analysis and design of the proposed amplifier. The CM DC gain is straightforward derived from (5) and is given by:

$$A_{dc,cm} = \frac{-g_{eq2}[2g_{m5}(g_{eq1} + g_{ds1}) + g_{m1}g_{eq1}]}{4g_{ds6}[g_{ds5}(g_{eq1} + g_{ds1}) + g_{ds1}g_{ds2}]} \quad . \tag{8}$$

The CM transfer function (equation (5)) also has three zeros; however, these zeros are at relatively high frequencies and can be ignored in practice.

4 Amplifier Design

The accuracy of the feedback networks (settling error, gain accuracy, bandwidth, etc.) where amplifiers are usually used is directly related with the amplifier's loop gain, which in turn at a particular frequency is a function of the GBW; therefore, the greater the GBW can be designed, the better system performances can be obtained [1]. As a result, in a basic view the design (sizing) problem of an amplifier is to achieve the maximum GBW possible with the minimum average power dissipation. In practice, however, other requirements (e.g., output swing, input-referred noise, distortion, etc.) have to be considered simultaneously resulting in a very challenging problem. To deal with this complexity and be able to obtain the most efficient solution (sizing), it is a common procedure to use a circuit optimizer.

Alternatively to the automated/optimized sizing, a manual and interactive equation-based approach can be followed. In order to come up with a tractable design problem, only the most important requirements are considered by the designer and the remaining ones are achieved with some design rules of thumb, which generally mean over-sizing the circuit. Although this approach generally precludes the optimum solution, we follow it here to gain more insight into the amplifier operation and also to validate the usefulness of the relatively simple expressions derived in the analysis section.

Throughout the previous section we conveniently considered symmetrical devices. Unfortunately, the PMOS and NMOS transistors are not symmetrical. At a simplified view, they differ mostly in the effective mobility (in the technology used in this work the mobility ratio of the NMOS/PMOS transistors (α_{np}) is roughly four times). To compensate this lower PMOS performance, the aspect ratio (W/L) of the PMOS transistors is usually α_{np} times greater than that of the NMOS counterparts. With this constraint, both device types have the same g_m (for a given drain current I_D), and this is also good to improve the noise performance of the amplifier [1]. However, the price to pay for wider PMOS transistors is greater parasitic capacitances. Another important constraint is to use channel lengths two or more times greater than the minimum channel length (L_{min}) allowed by the technology. Doing so short-channel phenomena are highly attenuated, but also the devices are slowed down.

Table 1. Active devices sizing and biasing ($V_{OV} \equiv V_{GS} - V_{TH}$).

Devices	*W/L* [µm/µm]	I_D [µA]	V_{OV} [mV]	V_{DS}/V_{DSsat} [V/V]	g_m [mS]	g_{mb} [µS]	g_{ds} [µS]	C_{gs} [fF]	C_{gd} [fF]	C_{sb} [fF]	C_{db} [fF]
M_1	32/0.24	344	79	2.14	5.30	679	212	54	9	17	15
$M_{2a\text{-}b}$	24/0.24	172	42	7.66	3.10	341	71	37	7	11	8
$M_{3a\text{-}b}$	96/0.24	-177	-75	5.02	2.90	522	69	155	28	68	57
M_4	128/0.24	-354	-106	1.65	4.93	996	212	226	38	101	94
$M_{5a\text{-}b}$	24/0.24	285	79	4.44	4.36	554	114	41	7	13	10
$M_{6a\text{-}b}$	16/0.24	108	52	1.58	1.88	184	121	25	5	6	6
$M_{7a\text{-}b}$	64/0.24	-108	-73	2.53	1.79	305	49	103	19	42	40
$M_{8a\text{-}b}$	96/0.24	-280	-108	2.57	3.90	788	108	169	28	76	67
M_9	0.18/0.72	8	383	1.12	0.03	4	3	1	0.1	0.1	0.1
M_{10}	24/0.18	8	-111	18.07	0.20	26	6	8	7	13	8
M_{11}	1.20/0.72	-8	-335	1.32	0.04	8	1	7	0.4	1	1
M_{12}	67/0.18	-8	71	16.97	0.19	38	7	26	21	54	38

Following the previous constraints and the set of equations derived in the analysis section, the amplifier is sized targeting the highest GBW while providing a moderate DM DC gain (> 55 dB) and an average current consumption of about 1 mA. The sizing result is summarized in Table 1 (the passive elements sizing is: C_L = 4 pF, $C_{a\text{-}b}$ = 0.5 pF, and $R_{a\text{-}b}$ = 500 kΩ). It is worth to note that only transistors M_{10} and M_{12} are not saturated in strong or moderate inversion, and, except for the parasitic capacitances, the transistors small-signal parameters are approximately symmetrical.

5 Simulation Results

In this section some electrical simulations are presented for the amplifier sizing shown in Table 1, which is done in a standard 0.13-µm high-speed 1.2 V CMOS technology (L_{min} = 0.12 µm) from a pure foundry player. Only standard-V_{TH} devices are used. For all simulations a load capacitance of 4 pF is employed. The DM frequency response is depicted in Fig. 5. The amplifier achieves a GBW of 197 MHz with a phase margin of about 83°, and a DC gain of about 55 dB while dissipating 1.12 mW from a 1.2 V supply. This results in a FoM of 704 MHz·pF/mW, which compares favorably with other up to date amplifiers [8].

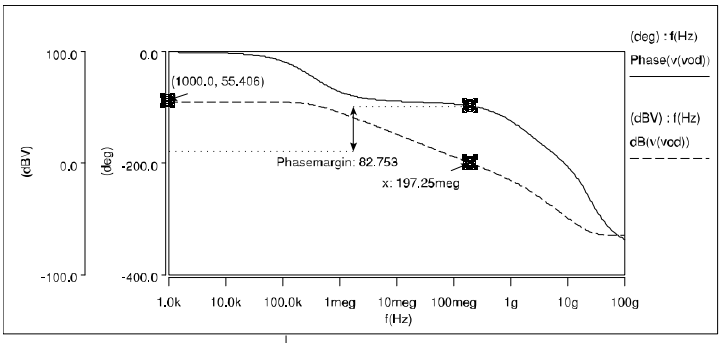

Fig. 5. Differential-mode frequency response.

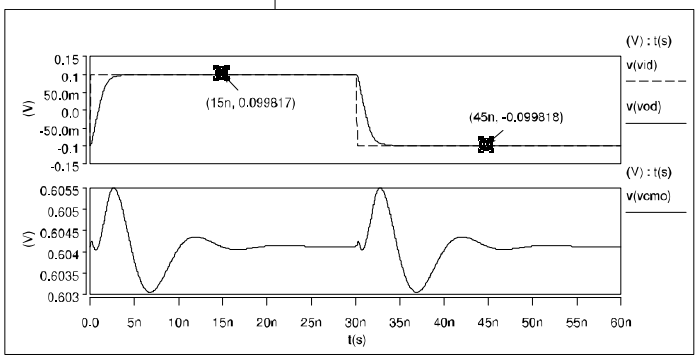

Fig. 6. 0.2 Vp-p,diff step response (top) and output CM voltage settling (bottom).

The step response of the amplifier in unity-gain feedback configuration for a step of 0.2 $V_{p\text{-}p,diff}$ is shown in Fig. 6 (top), where the settling final values are clearly

indicated. Also in this figure is shown the output CM voltage settling, which indicates a good CM behavior. The amplifier settles to within the 0.01 % error band about the final values in less than 7.1 ns (exactly 6.96 ns for the positive step and 7.06 ns for the negative one).

6 Conclusions

In this work we proposed a fully differential self-biased inverter-based folded cascode amplifier which uses the feedforward-regulated cascode technique. The amplifier achieves a DM GBW of 197 MHz with a capacitive load of 4 pF while dissipating an average power of only 1.12 mW from a 1.2 V supply. Configured as a unity-gain follower, and with the same load, the amplifier settles to within an error of 0.01 % in less than 7.1 ns for 0.2 $V_{p\text{-}p,diff}$ positive and negative steps. These results show the suitability of the proposed amplifier for high speed and low power applications designed in standard deep-submicron CMOS technologies.

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