Computer Architecture Development: From the BESM-6 Computer to Supercomputers

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Abstract. This work outlines the architecture and main features of the BESM-6 computer and data processing system AS-6. It also discusses the development of the "Electronika SS BIS-1" supercomputer system as well as the principle results of the research on multi-architecture (heterogeneous) supercomputer systems.

Keywords: Supercomputer architecture, heterogeneous multicomputer systems, pipelined vector processors, multi-architecture supercomputer systems, scalable heterogeneous chip multiprocessors

1. Introduction

The BESM-6 computer became the milestone of domestic computer development in the USSR. The chief designer of BESM-6 was academician S.A. Lebedev; the vice-chief designer was academician V.A. Melnikov. This computer was oriented towards the solution of large-scale scientific and engineering problems. This fact was the major influence on the architecture, the logical design, and the construction of the machine.

The logical circuits were based on diode gates and transistor current switch amplifiers with a floating power supply. Due to the original construction with short wires between modules, it achieved a very high clock frequency of 10 MHertz. It used a pipeline on clock frequency in control and arithmetic units. The interleaving of banks of the main memory and non-addressed buffer memory with associative search maintained the proper speed of access to the memory. In fact, this design was similar to the cache memory of the IBM System 360 Model 85, which was introduced two years later. The BESM-6 computer had a simple and effective one-address instruction set, a floating-point arithmetic unit and registers for address modification. For multi-programming, it used paged virtual addressing, a processor interruption system, a privileged instruction set, and a multi-user operational system. There were seven selector channels for magnetic drum, disk and tape memory, and multiplexer channel for input-output devices based on CPU multiprogramming. The original design methodology had two features: a formula description of logics and a table system with a table for each module describing all its wire connections [4].

2. Developments

The beginning of the production was 1967. The BESM-6 computer set two records: the duration of production of fifteen years and the duration of use for more than twenty years. The impact of this computer on many generations of engineers and programmers was based mainly on the fruitful ideas of its original design.

The next major development produced under the leadership of chief designer V.A. Melnikov was the AS-6 data processing system. The installation and maintenance of the BESM-6 at the computer centers that processed large volumes of data from many abonents, in particular from the Space Flight Control Center, served as a stimulus for the AS-6 system development. A weak point in the BESM-6 design was the small number of external devices available for use and the low throughput of the input-output channels. At the first stage the main task was the design of the interface unit (in Russian Аппаратура Сопряжения - АС-6) between the BESM-6 machine and AS-6 machine with the capability of attaching a large number of telephone and telegraph channels, channels for telemetric data, and also increasing the number of peripheral devices. However, after experimental work with at the first stage it became clear that the system must contain more powerful means of processing data; most of all, it must be a scalable system with the ability of attaching additional computers and devices. In the end, the task was the design of multicomputer system with an advanced means for system reconfiguration.

3. The AS-6 System

The fundamental ideas were the creation of application-specific subsystems and devices, and a unification of channels for the whole system. Beside the BESM-6 the system included an AS-6 central processing unit, a peripheral computer PM-6 consisting of a peripheral multichannel processor, a multichannel exchange unit (channeler), additional units of main memory, magnetic disks controllers, and a telemetric controller. They connected all these components by a unified first-level channel.

Since 1973, the AS-6 system was in use for experimental purposes. At the same time its development was continued. In 1975, the system was in use during works on the joint Soviet-American “Apollo–Soyuz” mission. The complete system was ready in 1979.

In the AS-6 system design, they realized for the first time new ideas that became the basis for supercomputer development and research on advanced high-performance computer architecture. To begin, it is necessary to highlight the following features:

- The AS-6 was a heterogeneous multicomputer system;
- The AS-6 central processing unit was problem-orientated for the tasks of complex objects control and effective translation;
- The PM-6 peripheral computer was function-specific for input-output control;
- The system used several specially designed unifying channels.

4. The BESM-10 and the Electronika

During the period of development and operation of the system, it became obvious that new architectural ideas and old electronic technology were not corresponding one to the other. In 1973, they worked out the BESM-10 system. They planned to develop the advanced computer system on high-speed ECL LSI chips. The Ministry of Radio Industry of the USSR did not support this project.

Further development in this direction under the leadership of academician V.A. Melnikov was the creation of the "Electronika SS BIS-1" supercomputer system. The aim of this development was to increase the performance of the new computer by two orders of magnitude. This led to the development of a new technology and appropriate architecture [5].

It was planned on the first stage of design that the system would include the following problem-oriented subsystems: a main computer with a pipelined vector processor, a matrix computer, and a logical data processing machine. In addition to this, they planned the development of the following function-specific subsystems: a peripheral computer, an external solid-state memory controller, a magnetic disk controller, control computers, and front-end computers. Due to the shortage of resources, they decided to postpone the development of the matrix, logical and peripheral machines.

The two choices of architecture for the main computer came under review; namely, the AS-6 central processor as enhanced in BESM-10 project and the pipelined vector processor. The second one was more appropriate due to much higher performance and better utilization of synchronous pipelines. The feature of external solid-state memory was the development of intellectual controller intended for the realization of different access methods for the main computer and for joining up two vector machines in a single platform. The peak performance of two-processor system achieved 500 MFLOPS. The software included operational systems of main and front-end computers, programming systems for macro assembler, and the Fortran 77, Pascal, and C programming languages [6].

In 1991, they tested the "Electronika SS BIS-1" system. Four sets of system hardware were delivered to customers. In the same year, they developed the "Electronika SS BIS-2" multiprocessor system. The planned peak performance was 10 GFLOPS. Beside multiprocessor main machines, the system has included monitor machines for task preparation and system control as well as massively parallel subsystems. However, in 1993, they made the decision to discontinue all work on this effort.

5. Reflections

The experience gained during the development of these systems became the basis for the research on heterogeneous supercomputer systems. They showed that the most effective system was one with subsystems oriented toward different forms of parallelism, that is, those corresponding to different forms of parallelism of parts belonging to the very large problems. The processing of large data sets is connected with data level parallelism. This form of parallelism is used most effectively in vector

processors. Another form of parallelism is parallelism of tasks, which is present in problems with great number of independent or weakly coupled subtasks. In this case, the best choice is a multiprocessing subsystem.

At the first stage of research, they developed the concept of heterogeneous supercomputer systems. In particular, they proposed to integrate in a single platform a vector uniprocessor and a multiprocessor, both having the access to the common memory [7]. The whole system could have several such integrated platforms based on large system memory [1].

The next stage of research concerned the analysis of advanced ULSI technologies with more than one billion transistors on a chip. They developed the original architecture of a scalable multi-pipelined vector processor. This processor had many parallel pipelined branches each having a chain of simple vector processor with several functional units and a local memory. A program having complex vector operations achieved the best results. The performance of such scalable processor was up to 1024 floating-point operations per cycle [8].

In accordance with these concepts, the research project of a multi-architecture supercomputer system had been developed [9]. The system consisted of a computing subsystem, monitor-simulating subsystem, system memory and external subsystem. The computing subsystem includes a vector multiprocessor, a scalar multiprocessor, and a monitor computer. The productivity of this system can be very high, up to 90% of its peak performance. The performance depends on the level of technology and it could reach up to 10 PFLOPS.

6. Conclusion

The comparison of this project with foreign researches and developments shows that in theoretical and conceptual sense it is ahead of published results [10]. On March 20 of 2006, Cray Inc. announced plans to develop supercomputers that will take the concept of heterogeneous computing to an entirely new level by integrating a range of processing technologies into a single platform. The second phase will result in a fully integrated multi-architecture system [3]. The same concepts were published in 1995 [7]. The term “multi-architecture” was proposed in 2003 [9].

The design of the cell chip by Sony, IBM, and Toshiba began in 2001. Cell is a heterogeneous chip multiprocessor that consists of an IBM 64-bit Power Architecture™ core, augmented with eight specialized co-processors based on a novel single-instruction multiple data [2]. In a paper published in 1998 [8], one reads the following:

> “The chains and parallel branches of the modules provide high performance due to their topology with the shortest links between functional units. In a maximum configuration, the uniprocessor might have up to 1024 modules and attain up to 4 thousands floating-point operations per cycle or 4 TFLOPS”.

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