# A Multistep Extrapolated S-Parameter Model for Arbitrary On-Chip Interconnect Structures

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**Abstract.** Accurate high-frequency interconnect models are needed for the precise estimation of signal delays, crosstalk, and energy losses in complex on-chip communication structures, such as hierarchical bus architectures and networks-on-chip. In this chapter we introduce a computationally-efficient wide-bandwidth characterization method based on an incremental extrapolation of S-parameters for arbitrary interconnect structures. Our method defines a systematic set of *a priori* parameter extractions and performs on-demand multistep extrapolations for interconnect segments with specified wire length, widths, spacings, metal layer, and neighboring routing information. Experimental evaluations show a maximum absolute error of less than $2{\cdot}10^{-2}$ (magnitude) and 7 degrees (angle) between our model and an industry-standard full-wave field simulator for a 90-nm CMOS process. We consistently enforce the passivity of the admittance matrices for each set of measured or generated parameters to eliminate the possible errors introduced during parameter measurements and extrapolation. Circuit-level simulations with the extrapolated model show a maximum signal delay error of less than 12.5% across multiple metal layers and wire configurations.

## 1 Introduction

At gigahertz frequencies, bus data and clock signals in integrated circuits are entering the microwave-specific range and the global on-chip interconnects become a more and more critical bottleneck in the global system performance [3, 14]. Moreover, numerous vias, crossing lines, and dielectric discontinuities, as well as a high wire packing density, are common attributes of state-of-the-art CMOS processes, but constitute nevertheless a frequent cause of crosstalk and reflections [5]. In addition, important signal quality drops generated through skin effects and dielectric losses augment with the frequency and cannot be ignored anymore in the present interconnect wires. In this respect, an increasingly high percentage of the final circuit performance becomes dictated by the interconnects [3], although devices and, recently, device parameter variability continue

to influence a significant performance amount. Thus, with increasingly high integration scales, the electrical performance of interconnects must be accurately characterized, modeled, and seamlessly integrated into IC design flows.

There are two common approaches in the analysis, measurement, and description of interconnect structures, namely in the time domain (using e.g. time-domain reflectometry or eye diagrams) and in the frequency domain (employing e.g. S-parameters) [14]. Although the two approaches may embed the same information in different forms, for practical circuit modeling purposes there are other factors, such as simulator support or the amount of computation overhead vs. accuracy, which decide which method becomes more appropriate. Furthermore, the analysis of on-chip interconnects is significantly burdened by challenging factors like high losses, scaled aspect ratios, increased number of wires, and strong non-uniformities in the dielectric stack [11], which contribute to the difficulty of employing standard measurement and simulation techniques.

In order to enable the accurate characterization of such parasitic effects within a practical workflow, designers need efficient performance estimation models at lower abstraction levels, which are capable to describe arbitrary interconnect structures [5] and are developed to support an integration with industry standard simulation frameworks. For instance, signal integrity analyses in digital communication structures operating at gigahertz frequencies [9] require the interconnect models to be valid over very wide frequency ranges.

### 1.1 Interconnect Modeling Challenges

The parasitic effects which affect the densely-packed interconnect wires, such as dielectric and substrate-induced dispersion, skin effects, and proximity effects, are strongly dependent on frequency [21] and need to be carefully considered by the interconnect models. Further, the evaluation of self and mutual impedances requires finding the current return paths for each individual wire, which are also frequency-dependent [15]. In addition, the actual return paths are difficult to estimate in interconnects, since there is no ground plane between the metal layers. Finally, the rapidly-switching signals exhibit very narrow rise and fall times and therefore contain significant spectral components within wide frequency ranges.

Interconnect models have traditionally evolved from simple, lumped capacitance, through lumped and distributed RC, until the state-of-the-art transmission-line distributed RLCG chains. Lumped and distributed RC models neglect inductive effects and fail to model lossy interconnect lines with propagation delays comparable or larger than the signal rise time [16]. Inductively and capacitively coupled, distributed RLCG models are today generally preferred [4, 13, 21], as they provide a good tradeoff between accuracy and model complexity. Within a distributed RLCG representation, the wires are divided into cascaded segments of circuit elements, extracted to reflect the interconnect response up to the desired significant frequency. These models are designed to enclose high-frequency effects, they achieve a perfect circuit-level compatibility with simulators, and are fast to simulate. On the other hand, they rely on coupled mutual inductances

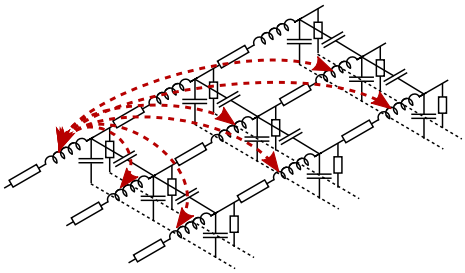

**Fig. 1.** Complexity of mutually-coupled inductances in distributed RLCG models.

between all the segments from all chains, as illustrated in Fig. 1 for only one inductance of a single chain segment. As a consequence, the modeling complexity increases exponentially with the number of cascaded segments and it becomes extremely hard to compute the value of each mutually coupled inductance pair.

Field solvers are commonly employed for computing accurate capacitance values [17], and for resistance and inductance [12] extractions. Nevertheless, for fast estimations of arbitrary interconnect structures needed in the early design stages, analytic expressions have been developed for capacitance [25] and self inductance [23] computation. On the other hand, mutual inductance values can only be estimated for two parallel running lines of equal wire length [19], hence they are restricted to a small number of cases. Field solver extractions of wire parameters, while being very accurate, are not applicable for real-time estimations, due to the time overhead and complex structural setup they imply. Moreover, the extracted models exhibit a decreasing accuracy with frequency increase and their maximum frequency of validity is specified in terms of the acceptable error [16]. In addition, distributed RLCG models rely on the quasi-TEM (transverse electric and magnetic) propagation of electromagnetic waves in transmission lines [4], which does not account for radiation losses and steep discontinuities (vertical vias, wire segment bends) [21] and assumes that the cross-sectional wire dimensions are much smaller than the wavelength at the maximum frequency of interest. In such cases, more precise electromagnetic analyses might be required.

Full-wave characterization methods [21] are ideal for accurate wide frequency-range modeling purposes, as they rely on a direct discretization of Maxwell's equations and find a numerical solutions at every frequency. Such methods include differential-based approaches, such as either frequency-domain finite element solvers [8] or time-domain finite difference solvers [7], and integral-based techniques, such as the method of moments [18] and the partial element equivalent circuits (PEEC) [21, 22]. The complexity implied by the discretization and numerical solving of Maxwell's equations in differential or integral form is requiring however a substantial computational overhead [21]. Hence, while holding the highest accuracy, these methods are not directly applicable for interconnect synthesis applications, unless a method exists to extract fast characterizations of arbitrary interconnect segments.

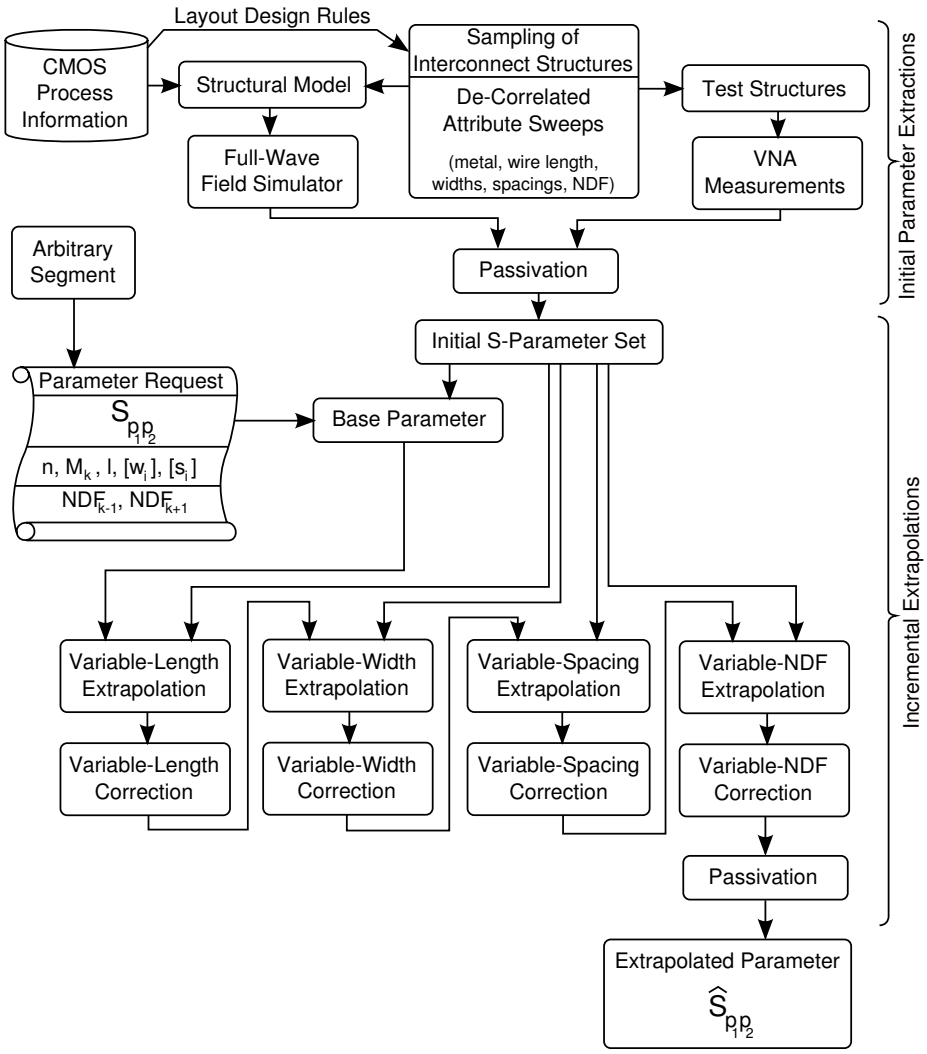


**Fig. 2.** Overview of the extrapolated S-parameter modeling workflow.

### 1.2 Multistep Extrapolated S-Parameter Model

As discussed in Sec. 1.1, there are two main directions in the high-frequency interconnect modeling: first, the full-wave numerical methods, with high accuracy but restricted by their large computation time, and second, the transmission-line distributed RLCG circuit models, with a good accuracy over the frequency range, but with a very complex tracking of the mutual inductive couplings between the distributed segments. We propose here a third approach with limited complexity and exhibiting a modeling performance close to the precision of a

field simulator. Our method consists of an incremental extrapolation technique for generating a set of S-parameters for an arbitrary interconnect segment in a given CMOS process, which relies on a predefined set of measured parameters obtained either with a vector network analyzer (VNA), or with a field simulator and a structural model of the silicon environment. The resulting model of the interconnect segment is an n-port with its associated S-parameter matrix.

As illustrated in Fig. 2, we start with an initial set of extracted parameters, which samples the entire range of possible interconnect structures, as seen from a designer's point of view, in a predetermined way. This initial set explores variations in the metal layer, wire number, wire length, as well as individual wire widths, wire spacings, and neighboring routing configurations in the adjacent metal layers. To describe various routings in the neighboring layers, we employ a neighboring density factor (NDF), as explained in Sec. 3.1. Within this process, the parameters are extracted for a wide frequency range which extends up to the bandwidth required by the target application. Furthermore, the extracted set can be obtained either from direct measurements on a test chip, or using an accurate field simulator and a multi-layered representation of the substrate, metal, and dielectric environment for the target technology. In both cases, measurement or computational errors are likely to affect the parameter values, threatening the stability of the interconnect model. We employ therefore a passivity enforcement criterion in our modeling flow, requiring the real part of the admittance-parameter matrix to be positive definite [24].

The initial set of parameters is then used as basis for an incremental suite of extrapolations, applied on the individual wire attributes, such as length, width, spacing, metal layer, and neighboring routing information. The individual extrapolation for each wire attribute is possible since the initial extraction of the base parameters is designed to minimize the correlation between the attributes. Furthermore, the inclusion of common design practices, such as orthogonal routing in neighboring metal layers and shielding of bus segments with $V_{DD}$ and ground ($GND$), as well as the layout design rules for a specified process, limit the complexity of the initial extraction procedure to a polynomial $O\left(N^2\right)$ for a maximum of $N$ minimum-width wires between the power grid shielding lines.

Several n-port parameter sets are available for representing the frequency behavior of interconnect segments, including impedance (Z), admittance (Y), and scattering (S) parameters. In Fig. 3 we have plotted the magnitude of a Z, Y, and S parameter for a 100-µm wire in a 90 nm technology (metal 5). The plot shows that the Z and Y parameters vary across several orders of magnitude within the considered frequency range, whereas the S parameter value remains between 0.8 and 1. If we consider the extrapolation of parameters across the entire frequency range, then the amount of variation of each parameter within this range will directly affect the extrapolation performance. As a result of this observation, we have chosen the S-parameter representation for our modeling methodology, since it exhibits the least amount of variations across the frequencies of interest.

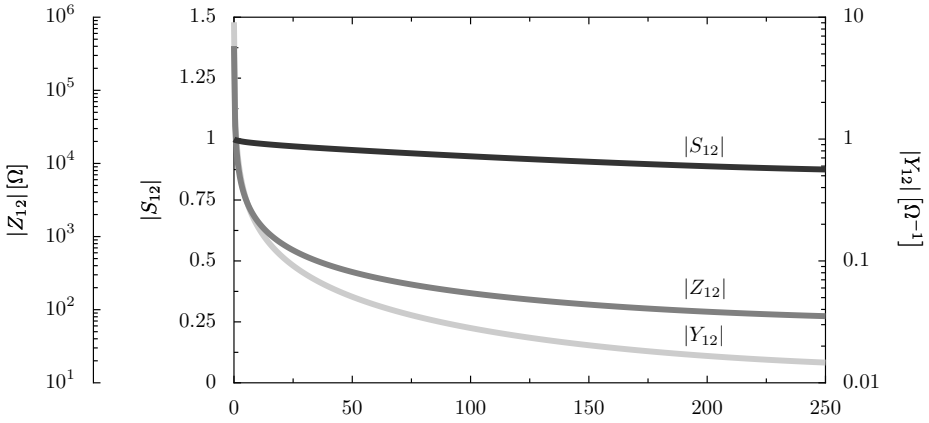


**Fig. 3.** Magnitude plot of the $Z_{12}$, $Y_{12}$, and $S_{12}$ parameters for a single-wire segment.

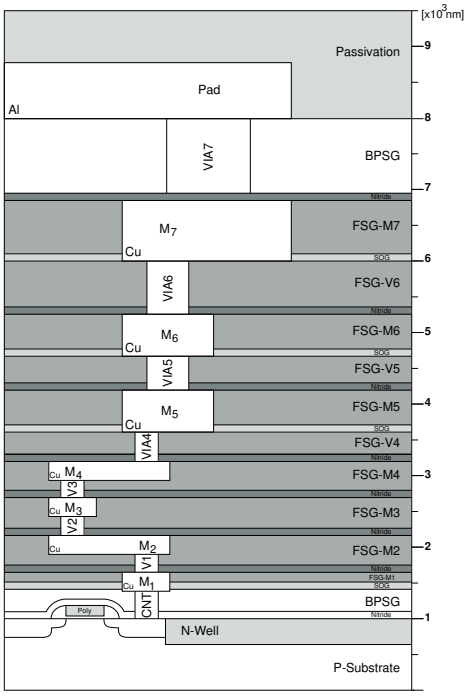


**Fig. 4.** Cross-section through the structural model of the CMOS process.

## 2 Parameter Extraction Framework

Our incremental extrapolation method relies on an initial set of S-parameters, which can be obtained either from direct VNA measurements, or with a field

solver. In this work we use an industry-standard 3D full-wave finite element method-based field simulator [1] to extract the base parameters from an interconnect structural model representing the target technology. Fig. 4 depicts a cross-section through the simulated 7-metal-layer (4-2-1) structure for the 90-nm, 1.0-V digital CMOS process employed within this work. The structure includes a total of 7 copper metal layers within a fluorosilicate glass (FSG) dielectric, separated by spin-on-glass (SOG) etch stop layers, silicon nitride dielectric diffusion barriers, and borophosphosilicate glass (BPSG), and finally bounded by a p-type doped silicon substrate at the bottom and an aluminum-pad grid on the top. This stacked material structure models effectively the complex dielectric environment and the inter-wire couplings present in tightly-integrated CMOS digital circuits.

For each metal layer, all the wire structures required for the subsequent extrapolations have been simulated across a frequency range from DC up to the maximum significant frequency. We have selected the maximum frequency for employing the model in SPICE simulations as:

$$F_{max} = F_{knee} \cdot N_{steps} \approx \frac{0.5}{t_{rise_{min}}} \cdot 5 \tag{1}$$

where $F_{knee}$ denotes the knee frequency and $N_{steps}$ is the number of required time steps per rise time ($t_{rise}$) during a SPICE transient simulation. A number of 5 steps together with a rounded upper bound for the knee frequency have been chosen for increased frequency validity. As a consequence, for an arbitrary minimum rise time of e.g. 10 ps, a maximum frequency of 250 GHz is obtained.

The extracted S-matrices usually contain generalized parameters, which are normalized to the impedances of each port. Since the port impedance depends on the attached load or driver, it's more practical to have all the parameters normalized to a single known impedance value. For convenience, the results have been normalized to the standard specific impedance of 50 Ω. In many cases, the solution of the solver would consider only the dominant mode. If higher-order modes are present in the structure, they should also be included. In such a case, a multi-mode analysis can be performed and the propagation constant $\gamma = \alpha + j\beta$ can be inspected for each mode. Nevertheless, each additional mode at a port adds an additional set of S-parameters. In our case however, the results show that a multi-mode analysis is not necessary, and the coupled lines can be accurately modeled with one mode per terminal.

## 3 Multistep Extrapolation Method

### 3.1 Extraction of the Initial Parameter Set

The target of our extrapolation procedure is to compute a requested parameter $S_{p_1 p_2}$ from the available set of extracted results, given the following specifications: the requested frequency $f_k$, the requested ports $p_1$ and $p_2$, and the structural details of the interconnect segment, such as the metal layer $M_k$, the wire

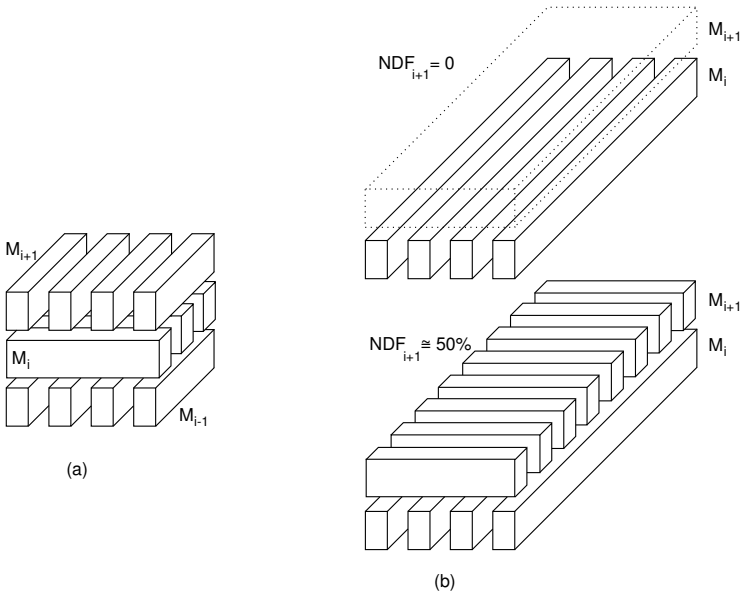


**Fig. 5.** (a) Orthogonal routing directions in adjacent metal layers. (b) NDF values of 0, respectively 50%.

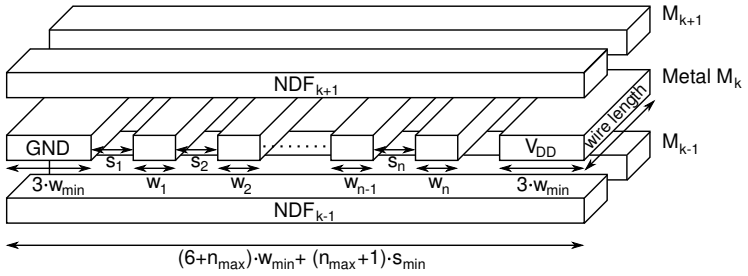


**Fig. 6.** Structural model of an $n$-wire interconnect segment.

length $l$, the set of wire widths $[w_i]$, the set of wire spacings $[s_i]$, and the neighboring routing configurations. In order to extrapolate the requested parameter values, we must have an initial set of extracted S-parameters for every metal layer $M_1, \ldots, M_N$, a variable number of wires, variable wire lengths, variable wire widths, variable wire spacings, and variable routings in the neighboring metal layers.

To keep the problem tractable, we need to make a series of simplifying assumptions, which actually reflect common best practices in the design of state-of-the-art high-density digital signal processors. First, the number of parallel running wires is limited to $n_{max}$ by introducing a power grid consisting of $V_{DD}$ and $GND$ shielding lines, in order to ensure a controlled low-impedance cur-

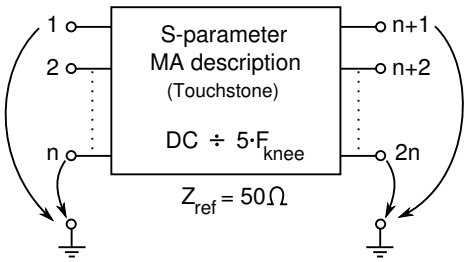


**Fig. 7.** Associated n-port model for an $n$-wire segment.

rent return path and to limit the inductive-coupling effects [13, 20]. In our case, we assume a maximum of six minimum-width signal wires between every two shielding lines. Finally, we assume that the routing in neighboring metal layers occurs only in orthogonal directions, to further minimize the inductive coupling, as shown in Fig. 5(a).

The influence of routed wires in the neighboring layers is considered by introducing a *neighboring density factor* (NDF). We further model the existence of routed wires in the adjacent metal layers by considering a density factor between 100% (i.e. a metal plane or a very thick wire which covers 100% of the considered segment) and 0% (i.e. no routing in the neighboring layer, as illustrated in Fig. 5(b) for e.g. 0 and 50%. Accordingly, we define an NDF value for each side of the metal, except for the lowest and the highest metal layers, which have only one neighbor. For instance, a segment placed on metal layer $M_k$ has an NDF corresponding to the neighbors in $M_{k+1}$ given by:

$$NDF_{k+1} = \frac{1}{l_k} \sum_{j=1}^{n_{k+1}} w_j \tag{2}$$

where $n_{k+1}$ is the number of wires, including shielding lines, which cross the segment, $w_j$ is the width of each wire, and $l_k$ is the length of the segment under consideration.

The structural model of an $n$-wire interconnect segment routed on a given metal layer $M_k$ is depicted in Fig. 6. All wires within the segment have the same length $l$, but individual widths $w_i$ and spacings $s_i$. Additionally, interconnects with distinct wire lengths can be modeled by concatenating several n-port segments [4]. The associated n-port model of the segment is shown in Fig. 7.

A complete base of initial parameters for the subsequent extrapolation must cover all metal layers and all numbers of wires in a segment, from 1 to $n_{max}$. As stated before, the number of parallel-running wires is restricted by the presence of a shielding grid, thus the distance between two subsequent $GND$ and $V_{DD}$ lines allows for the routing of maximum $n_{max}$ minimum-width, minimum-spacing wires. Furthermore, the minimum wire width $w_{min}$ and wire spacing $s_{min}$ are dictated by the layout design rules for each metal layer.

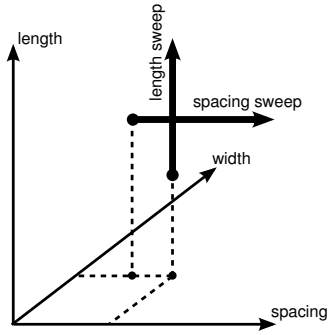


**Fig. 8.** Orthogonal sweeps of the wire attributes, illustrated here for length and spacing (NDF axis not shown).

Since the model applies an incremental sequence of extrapolations for each individual wire characteristic, the initial extracted set must be chosen in such a way, as to minimize the correlation between wire attributes. More specifically, we can describe the sequence of extrapolations for a requested $S_{p_1p_2}$ as:

$$\hat{S}_{p_1p_2} = \sum_{a_i \in \{a_1, a_2, \dots\}} extrap\left(\hat{S}_i^{p_1p_2}, F_{s_i}\right) \tag{3}$$

where $\hat{S}_{p_1p_2}$ is the extrapolated parameter value, $a_1, a_2, \dots$ are the individual wire attributes, $\hat{S}_i^{p_1p_2}$ is the extrapolated contribution of wire attribute $a_i$ to the final parameter value, and $F_{s_i}$ is the sweep function for wire attribute $a_i$. In order to apply the extrapolations individually on each attribute and sum the contributions, the sweep functions $F_{s_i}$ must be orthogonal, i.e. they must not introduce correlations between the attributes during the sweeps.

We can achieve orthogonality between the attribute sweeps if we vary only one attribute at a time, while keeping the other attributes constant. In the attribute space, such sweeps would correspond to orthogonal lines, parallel to each of the attribute axes, as exemplified in Fig. 8 for wire length and spacing sweeps. An additional orthogonal NDF axis can not be displayed in Fig. 8, however it only adds a fourth dimension to the attribute space.

It is to be noted, that the individual wire attributes are not completely independent one from each other. For instance, the assumption of having a fixed power grid introduces a relatively strong dependence between wire width and spacing. Specifically, we cannot vary the width of a wire without affecting also the spacing to its neighbors. This generates a residual correlation between the attribute sweeps which must be taken into account and corrected afterwards. A controlled weighting of the incremental attribute correction steps is performed during the subsequent extrapolations, which are described in Sec. 3.2.

Given these observations, we exploit the orthogonality of the parameter sweeps to the maximum, by sweeping each individual wire attribute while keeping the other attributes at a neutral value (i.e. the minimum, or the average

```
ExtractInitialSet()
 1  for  each metal layer M_k
 2  do for n ← 1 to n_max
 3     do /* Length Sweep */
 4        NDF_{k-1} ← NDF_{k+1} ← 0;
 5        for i ← 1 to n
 6        do w_i ← w_min;
 7           s_i ← ((n_max − n)/(n+1)) w_min + ((n_max + 1)/(n+1)) s_min;
 8        for l ← l_min (M_k) to l_max (M_k)
 9        do Extract-S-Parameters();
10
11        /* Width Sweep */
12        l ← l_mean (M_k);
13        for i ← 1 to n
14        do for w_sweep ← w_min to (n_max − n)(w_min + s_min) + w_min
15           do w_i ← w_sweep;
16              s_i ← ((n_max − n + 1)(w_min + s_min) + s_min − w_sweep)/2;
17              for j ← 1 to n, j ≠ i
18              do w_j ← w_min;
19                 s_j ← s_min;
20              if i < n then s_{i+1} ← ((n_max − n + 1)(w_min + s_min) + s_min − w_sweep)/2;
21              Extract-S-Parameters();
22
23        /* Spacing Sweep */
24        for i ← 1 to n
25        do w_i = w_min;
26        for i ← n downto 1
27        do for s_sweep ← s_min to (n_max − n)(w_min + s_min) + s_min
28           do s_i ← s_sweep;
29              for j ← 1 to n, j ≠ i
30              do s_j ← s_min;
31              if i < n then s_{i+1} ← (n_max − n)(w_min + s_min) + 2s_min − s_sweep;
32              Extract-S-Parameters();
33
34        /* NDF Sweep */
35        for i ← 1 to n
36        do w_i ← w_min;
37           s_i ← ((n_max − n)/(n+1)) w_min + ((n_max + 1)/(n+1)) s_min;
38        for NDF_{k-1} ← NDF_min to NDF_max
39        do for NDF_{k+1} ← NDF_min to NDF_max
40           do Extract-S-Parameters();
```

Listing 1: Extraction of the base parameter set.

value, depending on the attribute). The algorithm applied for the extraction of the base parameter set is given in Listing 1. First, the length of the segment

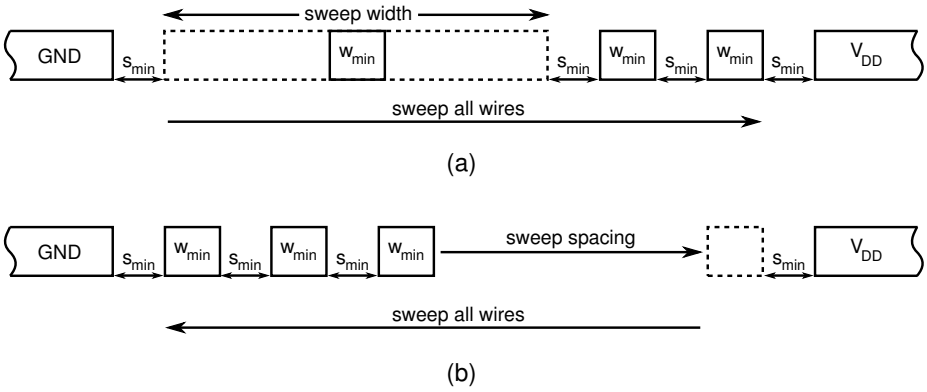


**Fig. 9.** Variable-width (a) and variable-spacing (b) sweeps during the initial parameter extraction.

is varied across the relevant domain for metal layer $M_k$, i.e. from $l_{min}(M_k)$ to $l_{max}(M_k)$, with all the wires set to the minimum width and equally-spaced between the bounding power grid. From this first set of simulations we collect parameter sets which reflect only changes in wire length, while the influence of wire width and spacing is minimized. Next, the length is kept constant at an average value for the given metal layer ($l_{mean}(M_k)$) and the width of each wire is varied from $w_{min}$ up to the maximum allowed by the minimum spacing to its neighbors, with all the other wires kept to the minimum width and spacing. While doing this, the varying wire is placed exactly in the middle of the distance between its two direct neighbors. This approach minimizes the influence of wire length and spacing on the results obtained from the variable-width sweeps. An illustration of the variable-width sweep procedure is shown in Fig. 9(a). After that, a variable-spacing sweep is performed sequentially for every wire, as illustrated in Fig. 9(b), with all the wires kept at minimum width. Again, the influence of wire length and width on the results is minimized. During all the previous sweeps, the NDF of both upper and lower metal layers was set to zero, to avoid any influence of neighboring routed wires on these first results. Finally, the NDF sweeps add the information related to the presence of wires routed in the neighboring layers. During the sweeps, the density factors are varied from a minimum value $NDF_{min}$, which corresponds to either 0 (i.e. no routed wire), or to the value computed from the presence of only the $GND$ and $V_{DD}$ lines, depending on the position of the metal layer. The maximum value $NDF_{max}$ corresponds to the maximum routing density present in the adjacent layer, including the power lines and maximum-width thick wires covering all the length of the segment. An illustration of such a maximum NDF case is shown in Fig. 10, where a single wire extends to the maximum width allowed by the fixed power grid. The Extract-S-Parameters() call designates the extraction of the S-parameter matrices for the given segment in a frequency sweep from 0 (DC) up to $F_{max}$ with a step dictated by the application requirements.

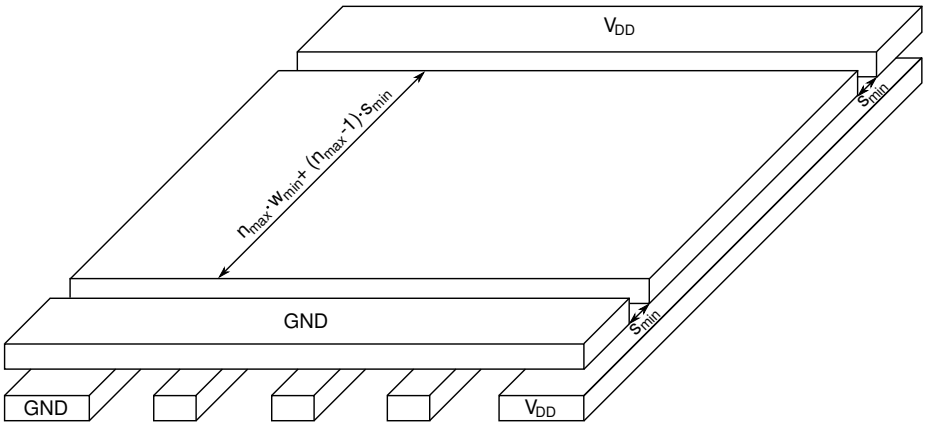


**Fig. 10.** Maximum NDF in the upper metal layer, with power grid and maximum-width signal line.

### 3.2 Incremental Extrapolation

The input for the extrapolation procedure consists of the following:

- The request for computing a parameter $S_{p_1p_2}$ for a multi-wire interconnect segment, described by its length, metal layer, individual wire widths and spacings, as well as the NDF information for the adjacent metal layers.
- An initial set of extracted base parameters for the target CMOS process, built as described in Sec. 3.1.

The result of the extrapolation method is the computed value $S_{p_1p_2}$ for the specified segment, at all frequencies from DC to $F_{max}$ (with the same step as the input data), written in the standard Touchstone magnitude-angle (MA) format.

First, the initial set of extracted parameters is parsed in a search for a base parameter for the extrapolation. This base parameter must be the closest-matching value for the requested parameter, i.e. a parameter describing an interconnect segment with the closest attributes to the requested one. To do this, a *matching rank* is first evaluated and the parameter with the highest matching rank will be afterwards selected. Considering a requested parameter $S_{p_1p_2}$, the factors which contribute to the matching rank and their respective weight are as follows:

- The wire length, which contributes to the wire resistance, coupling capacitance, and coupling inductance, thus having a high weight.
- The widths of the primary wires (connected to the ports $p_1$ or $p_2$), which contribute mainly to the wire resistance and coupling capacitance, having a high weight.
- The spacings of the primary wires, which mainly affect the coupling capacitance, with a medium weight.
- The widths of the secondary wires (not attached to the requested ports $p_1$ and $p_2$), which mainly influence the coupling inductance, with a relatively low weight.

– The spacings of the secondary wires, with a relatively low weight.
– The NDF, which affects only the coupling capacitance, hence with a relatively low weight.

The matching rank of an extracted parameter is computed as the sum of the individual weights for the structural details that match with the requested segment. If a closest-matching parameter is found, then it is used further as the base parameter for the extrapolation. If no structural attributes can be matched with any of the already-extracted results, then the base parameter must be extrapolated from e.g. the variable-length set. Concretely, if the wire length for the requested parameter $S_{p_1p_2}$ is $l_r$, then the extrapolated base parameter is computed as:

$$\begin{aligned} M_b^{p_1p_2} &= \text{extrap}\left([l_i], \left[M_{l_i}^{p_1p_2}\right], l_r, \text{'method'}\right) \\ A_b^{p_1p_2} &= \text{extrap}\left([l_i], \left[A_{l_i}^{p_1p_2}\right], l_r, \text{'method'}\right) \end{aligned} \tag{4}$$

where $M_b^{p_1p_2}$ and $A_b^{p_1p_2}$ are the magnitude, respectively angle, of the base parameter for the extrapolation of $S_{p_1p_2}$, $[l_i]$ represents the set of wire lengths available in the initial extracted set, while $M_{l_i}^{p_1p_2}$ and $A_{l_i}^{p_1p_2}$ are the magnitude, respectively angle, of $S_{p_1p_2}$ for the segment with wire length $l_i$ from the initial extracted set. The keyword 'method' designates the desired extrapolation function, which can be based either on linear interpolation, piece-wise cubic hermite polynomials, cubic interpolation, or cubic spline interpolation with smooth derivatives, to name only a few. The results shown in this work have been obtained with a cubic spline interpolation method, which proved to offer the best precision.

The base parameter represents the very first approximation of the requested $S_{p_1p_2}$ value. Because in the most cases the structural attributes of the requested segment do not coincide with the attributes related to the base parameter, a set of incremental corrections for each structural element must be further applied as explained in the following. Let's first assume that the wire length related to the base parameter is $l_b$. We extrapolate two parameter values from the length-sweep results, one for $l_b$ and one for the requested wire length $l_r$:

$$\begin{aligned} M_{l_b}^{p_1p_2} &= \text{extrap}\left([l_i], \left[M_{l_i}^{p_1p_2}\right], l_b, \text{'method'}\right) \\ M_{l_r}^{p_1p_2} &= \text{extrap}\left([l_i], \left[M_{l_i}^{p_1p_2}\right], l_r, \text{'method'}\right) \end{aligned} \tag{5}$$

The corresponding angle values $A_{l_b}^{p_1p_2}$ and $A_{l_r}^{p_1p_2}$ are computed in a similar way:

$$\begin{aligned} A_{l_b}^{p_1p_2} &= \text{extrap}\left([l_i], \left[A_{l_i}^{p_1p_2}\right], l_b, \text{'method'}\right) \\ A_{l_r}^{p_1p_2} &= \text{extrap}\left([l_i], \left[A_{l_i}^{p_1p_2}\right], l_r, \text{'method'}\right) \end{aligned} \tag{6}$$

Next, two variable-length *correction terms* $\Delta_l M^{p_1p_2}$, respectively $\Delta_l A^{p_1p_2}$ are computed as the following differences:

$$\begin{aligned} \Delta_l M^{p_1p_2} &= M_{l_r}^{p_1p_2} - M_{l_b}^{p_1p_2} \\ \Delta_l A^{p_1p_2} &= A_{l_r}^{p_1p_2} - A_{l_b}^{p_1p_2} \end{aligned} \tag{7}$$

and the *variable-length correction* is applied to the base parameter as follows:

$$\begin{aligned} M_b^{p_1p_2} &= M_b^{p_1p_2} + w_c \cdot \Delta_l M^{p_1p_2} \\ A_b^{p_1p_2} &= A_b^{p_1p_2} + w_c \cdot \Delta_l A^{p_1p_2} \end{aligned} \tag{8}$$

where $w_c$ is a correction weighting factor for the parameter inter-correlations and is therefore data-dependent.

Further, to take into account the influence of wire width and spacing, for each wire in the segment the following parameter values are extrapolated:

$$\begin{aligned} M_{w_{b,i}}^{p_1p_2} &= \text{extrap}\left([w_{j,i}], \left[M_{w_{j,i}}^{p_1p_2}\right], w_{b,i}, \text{'method'}\right) \\ M_{w_{r,i}}^{p_1p_2} &= \text{extrap}\left([w_{j,i}], \left[M_{w_{j,i}}^{p_1p_2}\right], w_{r,i}, \text{'method'}\right) \end{aligned} \tag{9}$$

$$\begin{aligned} M_{s_{b,i}}^{p_1p_2} &= \text{extrap}\left([s_{j,i}], \left[M_{s_{j,i}}^{p_1p_2}\right], s_{b,i}, \text{'method'}\right) \\ M_{s_{r,i}}^{p_1p_2} &= \text{extrap}\left([s_{j,i}], \left[M_{s_{j,i}}^{p_1p_2}\right], s_{r,i}, \text{'method'}\right) \end{aligned} \tag{10}$$

where $w_{b,i}$ and $w_{r,i}$ represent the width of wire $i$ (with $i$ varying from 1 to $n$) for the base and the requested parameter, respectively, while $s_{b,i}$ and $s_{r,i}$ are the corresponding spacing values. The sets $[w_{j,i}]$ and $[s_{j,i}]$ contain the width and spacing arrays employed in the sweeps from Sec. 3.1 (see Listing 1 lines 14, respectively 28). In addition, the angle components $A_{w_{b,i}}^{p_1p_2}$, $A_{w_{r,i}}^{p_1p_2}$, $A_{s_{b,i}}^{p_1p_2}$, and $A_{s_{r,i}}^{p_1p_2}$ are obtained in a similar way.

After computing the correction terms $\Delta_{w_i} M^{p_1p_2}$, $\Delta_{w_i} A^{p_1p_2}$, $\Delta_{s_i} M^{p_1p_2}$, and $\Delta_{s_i} A^{p_1p_2}$ as the corresponding differences from the previously-extrapolated values, we apply the *variable-width* and *variable-spacing corrections*:

$$\begin{aligned} M_b^{p_1p_2} &= M_b^{p_1p_2} + w_c \sum_{i=1}^{n} \left(\Delta_{w_i} M^{p_1p_2} + \Delta_{s_i} M^{p_1p_2}\right) \\ A_b^{p_1p_2} &= A_b^{p_1p_2} + w_c \sum_{i=1}^{n} \left(\Delta_{w_i} A^{p_1p_2} + \Delta_{s_i} A^{p_1p_2}\right) \end{aligned} \tag{11}$$

Finally, the *variable-NDF correction* is computed and applied:

$$\begin{aligned} M_b^{p_1p_2} &= M_b^{p_1p_2} + w_c \cdot \Delta_{NDF} M^{p_1p_2} \\ A_b^{p_1p_2} &= A_b^{p_1p_2} + w_c \cdot \Delta_{NDF} A^{p_1p_2} \end{aligned} \tag{12}$$

where the correction terms $\Delta_{NDF} M^{p_1p_2}$ and $\Delta_{NDF} A^{p_1p_2}$ represent the differences between the extrapolated parameters for the base NDF and for the requested NDF values.

The correction steps applied to the base parameter are incremental and the influences of various wire attributes on the S-parameters are treated as independent. Although minimized, a non-zero residual correlation still exists between the individual influences, especially in the case of wire width variation, which has a significant influence on the spacing, see e.g. Fig. 9(a). Thus, a correction weighting factor $w_c < 1$ is employed, which accounts for the residual correlation and prevents therefore an overscaling of the final corrected value. A further correction of the extrapolated parameters is provided in Sec. 3.3.

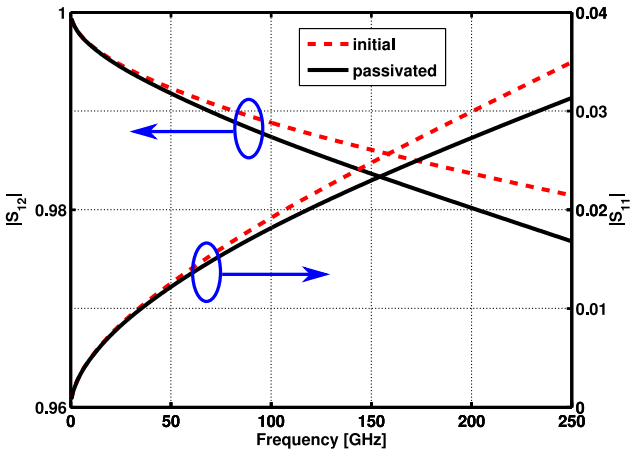


**Fig. 11.** Passivation example for a single-wire interconnect segment (metal 1, $l = 10\,\mu\text{m}$, $w = 400\,\text{nm}$, $s = 810\,\text{nm}$).

### 3.3 Passivity Enforcement

Both measured and extrapolated S-parameters must exhibit a passive behavior, i.e. the interconnect model must dissipate active power, as opposed to generate it, at any value of the input voltage and at any frequency. We employ here a passivation enforcement criterion based on the correction of the eigenvalues of the admittance matrix [6]. First, the Y-parameter matrix can be computed from the S-parameter matrix as follows [10]:

$$\mathbf{Y} = \mathbf{G}_{ref}^{-1} \cdot \mathbf{Z}_{ref}^{-1} \cdot (\mathbf{S} + \mathbf{E})^{-1} \cdot (\mathbf{E} - \mathbf{S}) \cdot \mathbf{G}_{ref} \tag{13}$$

where, in our case, $\mathbf{Z}_{ref} = Z_{ref} \cdot \mathbf{E}$ is the reference impedance matrix, $\mathbf{G}_{ref} = \frac{1}{\sqrt{|Z_{ref}|}} \cdot \mathbf{E}$ is the reference conductance matrix, and $\mathbf{E}$ is the identity matrix. The passivity criterion requires the real part of the $\mathbf{Y}$ matrix to be positive definite [6], i.e. the eigenvalues of $Re\{\mathbf{Y}\}$ to be all positive. This relatively simple technique ensures both the passivity and the stability of the model. A more detailed discussion on passivity and stability conditions can be found in [24].

We set the negative eigenvalues of $Re\{\mathbf{Y}\}$ to zero as in [9], then we recompute the real part as:

$$Re\{\mathbf{Y}\} = \mathbf{V} \cdot \mathbf{D}_{corr} \cdot \mathbf{V}^{-1} \tag{14}$$

where $\mathbf{V}$ contains the eigenvectors of $Re\{\mathbf{Y}\}$ and $\mathbf{D}_{corr}$ is a diagonal matrix with the corrected eigenvalues. The S-parameter matrix is recomposed from the corrected admittance matrix as:

$$\mathbf{S} = \mathbf{G}_{ref} \cdot (\mathbf{E} - \mathbf{Z}_{ref} \cdot \mathbf{Y}) \cdot (\mathbf{E} + \mathbf{Z}_{ref} \cdot \mathbf{Y})^{-1} \cdot \mathbf{G}_{ref}^{-1} \tag{15}$$

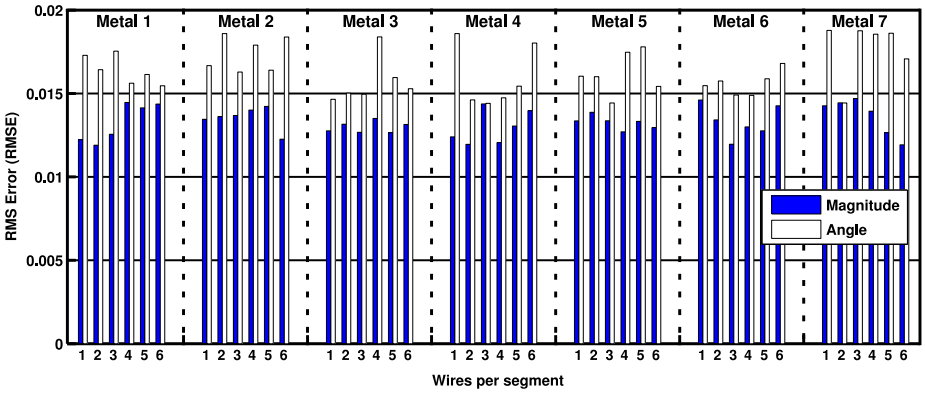


**Fig. 12.** RMS error between extrapolated and extracted results for the entire range of tested interconnect segments.

Fig. 11 shows two extracted S-parameters before and after the passivation, for a 10-µm single-wire interconnect segment placed on the $M_1$ layer. We observe that the passivity correction becomes more substantial as the frequency increases, which shows that measurement and numerical computation errors increase with frequency.

## 4 Experimental Validation

In order to assess the overall precision of the extrapolation method we have tested a wide range of interconnect segments in the 90-nm technology, with up to six wires per segment and varying from metal 1 up to metal 7. In every case, the evaluation has been performed on a "difficult", non-standard segment configuration, with each wire having an individual width and spacing, randomly assigned with a uniform distribution between the minimum and maximum values allowed by the design rules.

We computed the RMS error (RMSE) between the extrapolated parameters and the parameters obtained with the field simulator, from all the $(2n)^2$ S-parameters of each segment as:

$$RMSE = \sqrt{\frac{1}{N_f \cdot 4n^2} \sum_{i,j=1}^{2n} \sum_{f_k}^{N_f} \left( \hat{S}_{ij}^{f_k} - S_{ij}^{f_k} \right)^2} \tag{16}$$

where $\hat{S}_{ij}$ and $S_{ij}$ represent the extrapolated, respectively the extracted parameter values, and $f_k$ is the frequency index, indicating the steps from DC up to the maximum frequency of interest. The results for all the investigated configurations are summarized in Fig. 12, where the angle values have been normalized to 360°. The maximum absolute errors were $1.8{\cdot}10^{-2}$ in magnitude and 6.8 degrees in angle. The main causes for the exhibited deviations are given by:

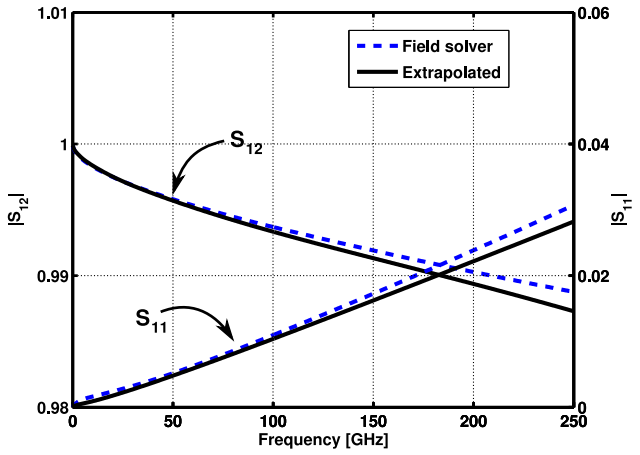


**Fig. 13.** Magnitude of extrapolated and extracted parameters for a single-wire interconnect segment.

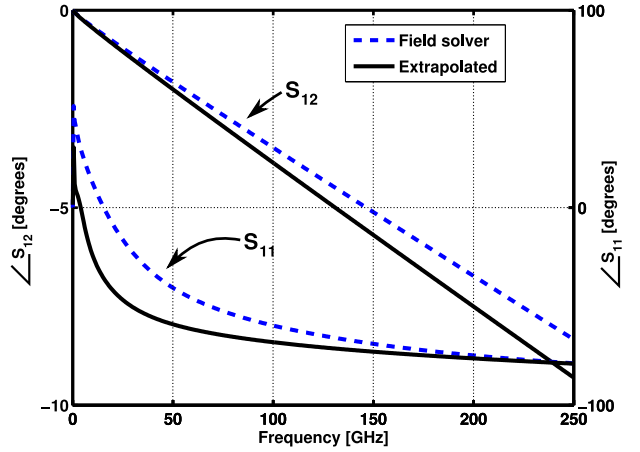


**Fig. 14.** Angle values for the extrapolated and extracted parameters of a single-wire segment.

- The residual correlations between the wire attributes, especially width and spacing.
- The non-optimal passivity correction [6, 24].
- The precision of the extrapolation method, which is limited by the number of samples available in the initial set.

| Wire | Length | Width | Spacing | $NDF_3$ | $NDF_5$ |
|---|---|---|---|---|---|
| 1 | 2.5 mm | 140 nm | 200 nm | 70% | 25% |
| 2 | | 300 nm | 290 nm | | |
| 3 | | 300 nm | 295 nm | | |

**Table 1.** Wire attributes for a three-wire $M_4$-segment.

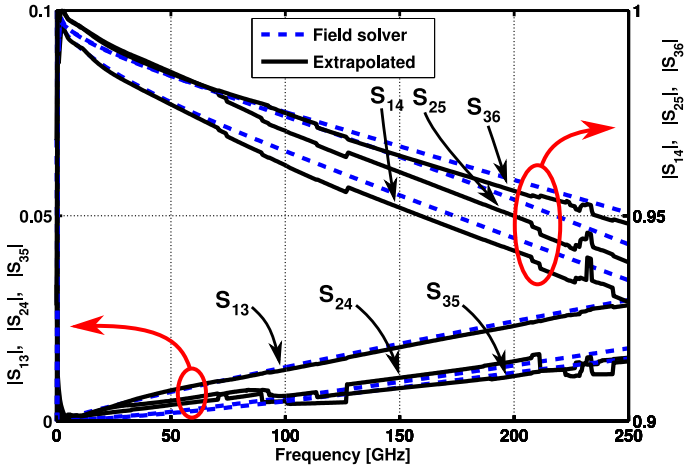


**Fig. 15.** Magnitude plot of six S-parameters for a three-wire $M_4$-segment.

A more detailed example is shown in Fig. 13 and 14 for a single-wire $M_1$-segment with $l$ =10 µm, $w$ = 580 nm, $s$ = 420 nm, and NDF = 35%. The plots show the values for $S_{11}$ and $S_{12}$, while the other two parameters, $S_{22}$ and $S_{21}$, are virtually identical with $S_{11}$, respectively $S_{12}$ due to the inherent symmetry of the wire. From Fig. 13, one can see that $|S_{12}|$, which reflects the power wave transmission from port 2 to port 1, reaches a maximum of 1 at DC and starts to drop relatively fast as the frequency increases into the multi-GHz range. This behavior shows the rate of losses in signal power with the frequency increase, for a direct transmission across the line from port 2 to port 1, and points out the expected signal integrity issues which influence the interconnect at high frequencies. The level of signal reflections at port 1 is shown by the plot of $|S_{11}|$, which indicates that reflections are essentially zero at DC, but increase with the frequency. Again, the expected signal reflections within the wire are here illustrated and quantified. The extrapolated model is overall in a good agreement with the directly-extracted parameter data.

A further example is depicted in Fig. 15 for a three-wire segment in metal 4, with the attributes presented in Tab. 1. Only six parameters have been selected for the plot from the complete set of 36, in order to maintain a reasonable

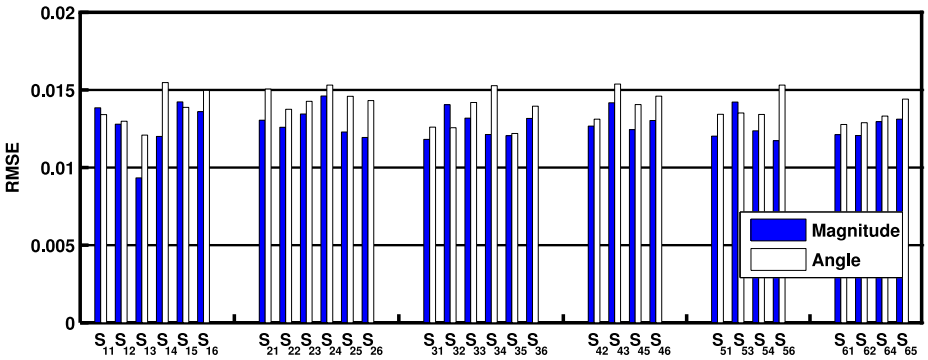


**Fig. 16.** RMS errors between extrapolated and directly-extracted parameters (three-wire $M_4$-segment).

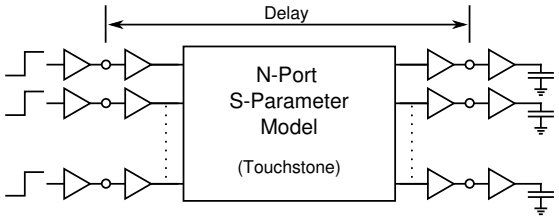


**Fig. 17.** Circuit employed for the transient simulations.

amount of visible detail. $S_{14}$, $S_{25}$, and $S_{36}$ represent the direct signal transfer along the three wires, and show substantial losses at the maximum frequency of interest. $S_{13}$, $S_{24}$, and $S_{35}$ reflect the crosstalk between wires 3 and 1, 1 and 2, respectively 2 and 3. Here we see that the crosstalk also increases significantly with the frequency. Thus, we can clearly observe that a wide-frequency interconnect model is extremely important to quantify the amount of performance losses at very high switching speeds. Beyond these observations, we can also notice a very good agreement between the extrapolated model and the directly-extracted parameters. In order to obtain a more detailed quantitative evaluation of the modeling performance we have computed the RMS error for every parameter across the investigated frequency range. The results are displayed in Fig. 16 where we omitted the parameters which are identical due to the wire symmetry, i.e. $S_{44}$ with $S_{11}$, $S_{41}$ with $S_{14}$, $S_{55}$ with $S_{22}$, $S_{52}$ with $S_{25}$ etc. The measured errors are in line with our previous evaluations from Fig. 12.

Next, we have tested the extrapolated S-parameter models within transient circuit-level simulations. For this purpose we used a SPICE-level simulator which supports the direct modeling of n-port elements using S, Y, or Z-parameter descriptions [2]. Within our modeling framework, the extrapolated S-parameters are saved as standard Touchstone files which are directly supported by the simu-

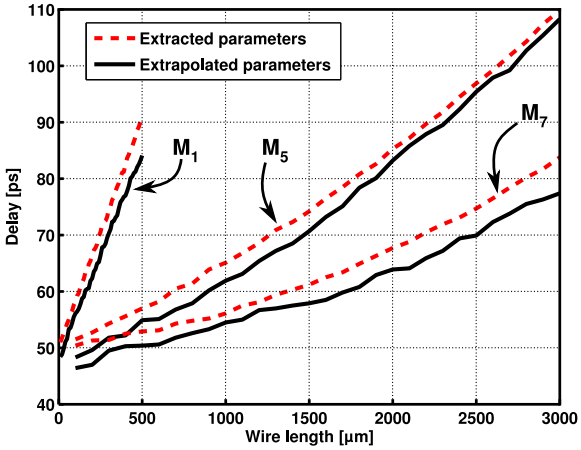


**Fig. 18.** Signal propagation delays from three-wire interconnect segments placed on three metal layers.

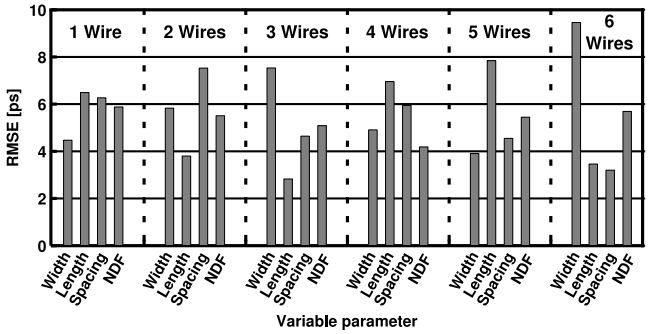


**Fig. 19.** Delay RMSE for the transient simulations of interconnect segments on metal 5.

lator. The circuit configuration employed for the tests is shown in Fig. 17, where each wire of the interconnect model is driven and terminated independently.

We have measured the signal delay across each wire with both quiet and switching neighboring lines and we compared the results obtained using our extrapolated S-parameters and the parameters extracted with the field solver. A detailed view of the results is shown in Fig. 18 for three-wire interconnect segments of various lengths placed on $M_1$, $M_5$, and $M_7$, in each case with one neighbor switching at the same time in opposite direction. To better quantify the differences we have measured the RMS and relative errors for every series of simulations. First, we have measured the RMS errors on each metal layer, for each number of wires per segment, and for each sweep of the wire attributes.

| | | Number of wires per segment | | | | | |
|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 |
| Metal layer | 1 | 4.28% | 7.37% | 7.77% | 10.01% | 10.47% | 11.88% |
| | 2 | 5.04% | 6.69% | 8.19% | 10.39% | 10.24% | 11.46% |
| | 3 | 5.46% | 5.56% | 6.94% | 8.28% | 9.51% | 11.50% |
| | 4 | 6.93% | 5.34% | 7.78% | 8.83% | 9.94% | 11.74% |
| | 5 | 6.79% | 7.32% | 6.21% | 9.32% | 10.39% | 10.51% |
| | 6 | 6.37% | 5.78% | 7.41% | 8.60% | 11.27% | **12.21%** |
| | 7 | 5.56% | 7.18% | 8.38% | 8.97% | 9.29% | 11.14% |

**Table 2.** Maximum relative delay error across all considered metal layers and wires per segment.

A detailed plot of the RMS errors in the case of metal 5 is depicted in Fig. 19. Each RMSE value is computed across the parameter sweep range, across the investigated frequency range, and across all S-parameters.

After computing the RMSE values we have evaluated the maximum relative delay error obtained across all metal layers and numbers of wires per segment. For each metal layer and for each wire number we have varied individually the segment length, wire widths, wire spacings, and the NDF, and we evaluated the maximum error as:

$$\varepsilon_r^{max} = \max\left\{ \max_{l_i}\left\{\left|\frac{\hat{\delta}_{l_i}-\delta_{l_i}}{\delta_{l_i}}\right|\right\}, \max_{w_{j,i}}\left\{\left|\frac{\hat{\delta}_{w_{j,i}}-\delta_{w_{j,i}}}{\delta_{w_{j,i}}}\right|\right\}, \max_{s_{j,i}}\left\{\left|\frac{\hat{\delta}_{s_{j,i}}-\delta_{s_{j,i}}}{\delta_{s_{j,i}}}\right|\right\}, \max_{NDF_i}\left\{\left|\frac{\hat{\delta}_{NDF_i}-\delta_{NDF_i}}{\delta_{NDF_i}}\right|\right\}\right\} \tag{17}$$

where $\hat{\delta}$ is the delay measured with the extrapolated model and $\delta$ is the delay obtained using the directly-extracted parameters. It is to be noted that the attribute variations during these tests have been selected in such a way that they do not include the same values found in the initial set, for a better evaluation of the extrapolation performance. Wire length has been varied between 1 and 500 µm for the local layers ($M_1$ to $M_4$), between 100 µm and 5 mm for intermediate layers ($M_5$ and $M_6$) and from 3 mm to 5 cm for the global layer ($M_7$). Wire width and spacing have been varied from the minimum design rule for each metal layer up to the maximum allowed by the shielding grid and the number of wires between two successive power lines (see Listing 1 lines 14 and 28). Additionally, the minimum NDF was always zero, while the maximum NDF varied between 85% and 100% depending on the wire length (see Fig. 10).

The evaluated maximum relative errors are shown in Tab. 2. The maximum error generally increases with the number of wires per segment, since the total number of S-parameters increases quadratically with the number of wires. As it can be seen, our method achieved during the tests a maximum delay error of 12.21% for six-wire segments placed on the $6^{\text{th}}$ metal layer.

## 5 Conclusions

Technology-accurate wide-bandwidth interconnect models are needed for the precise estimation of signal delays, crosstalk, and energy losses across the complex on-chip communication structures. Traditional transmission-line distributed models offer a good accuracy at the expense of limited frequency validity and complex mutual inductance extractions, therefore they always imply a tradeoff between precision and computational efficiency. On the other hand, full-wave interconnect analyses provide a high accuracy at all frequencies, but require extensive numerical computations which can not be performed in real time. In addition, the amount of possible wire configurations across various lengths, widths, spacings, and metal layers increases exponentially the complexity of the modeling problem.

This chapter has introduced a computationally-efficient wide-bandwidth characterization method for arbitrary interconnect structures, which is based on the incremental extrapolation of S-parameters. The method defines a set of *a priori* parameter extractions, designed to reflect the particularities of a given manufacturing process. This initial set of parameters can be extracted with high precision within an independent time frame prior to the application, and represents a data base for the subsequent computations. Further, it has been shown how the initial set can be extracted by means of a full-wave field simulator and a structural model reflecting the technological process. It has also been shown that the complexity of covering the large set of possible wire attributes can be substantially reduced by minimizing the correlations between the segments employed in the initial set. A further measure to limit the complexity is to consider a fixed power grid and orthogonal routing directions. Moreover, the presence of wire segments in the neighboring metal layers has been modeled by introducing a density factor which indicates the amount of coupling capacity between the metal layers. Next, an incremental extrapolation procedure is performed in real time for every parameter request, which includes a search for a best-matching base parameter and a suite of extrapolated corrections applied for every wire attribute. A passivation enforcement criterion has been also described, which ensures that the obtained model is stable and exhibits a passive behavior.

The model has been tested across all metal layers and up to six wires per segment and the results have been compared with an industry-standard field simulator. The results show a good agreement with the directly-extracted parameters and lie within $2{\cdot}10^{-2}$ and 7 degrees for magnitude and angle values, respectively. Another suite of extensive tests has been performed in the time domain, within circuit-level simulations. The results summarized in Tab. 2 show a maximum error of less than 12.5%.

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