Wearable ECG SoC for Wireless Body Area Networks: Implementation with Fuzzy Decision Making Chip

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Abstract. The work aims to present an ultra-low power Electrocardiogram (ECG) on a chip with an integrated Fuzzy Decision Making (FDM) chip for Wireless Body Sensor Networks (WBSN) applications. The developed device is portable, wearable, long battery life, and small in size. The device comprises two designed chips, ECG System-on-Chip and Fuzzy Decision Maker chip. The ECG on-chip contains an analog front end circuit and a 12-bit SAR ADC for signal conditioning, a QRS detector, and relevant control circuitry and interfaces for processing. The analog ECG front-end circuits precisely measure and digitize the raw ECG signal. The QRS complex with a sampling frequency of 256 Hz is extracted after filtering. The extracted QRS details are sent to the decision maker chip, where abnormalities/anomalies in patient's health are detected and an alert signal is sent to the patient via wireless communication protocol. The patient's ECG data is wirelessly transmitted to a PC, using ZigBee or a mobile phone. The chip is prototyped and employed in a standard 0.35µm CMOS process. The operating voltage of Static RAM and digital circuits and analog core circuits are 3.3 Volts and 1 Volt, respectively. The total area of the device is about $6cm^2$ and consumes about 8.5µW. Small size and low power consumption show the effectiveness of the proposed design, suitable for wireless wearable ECG monitoring devices.

1. Introduction

According to World Health Organization (WHO), cardiovascular and modern human behavior-related diseases are the major cause of mortality worldwide. These types of cardiovascular related-diseases, like Cardiac arrhythmias, Atrial fibrillation, and Coronary heart diseases, can be monitored and controlled with continuous personal healthcare supervision [1-2]. Electrocardiogram (ECG) embodies the cardiovascular condition, therefore, is considered one of the most important human physiological signals. In applying measurement of physiological signals for continuous monitoring, patients usually cannot carry a bulky instrument, which restricts their mobility and makes them uncomfortable, with so many electrodes and cables attached to their bodies. Therefore, there is growing demand for a compact wearable ECG acquisition system [2]. Wearable monitoring devices can record physiological variables, like

ECG, blood pressure, etc. for several hours and store them in the memory for future use. The stored ECG data can then be utilized by clinicians or cardiologists for further diagnosis.

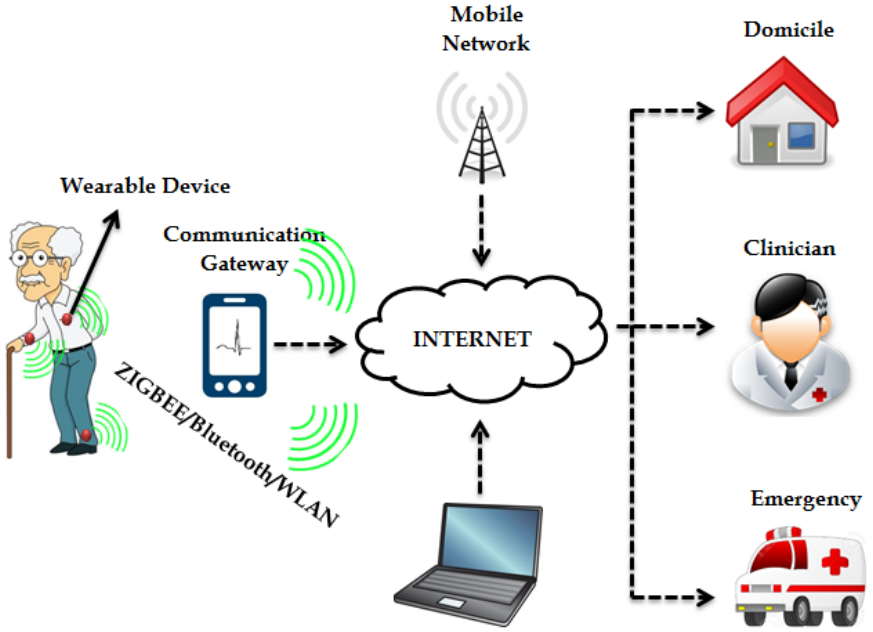


Fig. 1. Graphical Illustration of wearable health care monitoring

The graphical embodiment of a wearable system for continuous remote monitoring is illustrated in Fig.1. Wearable sensors/electrodes (deployment in accordance with the clinical application) collect the physiological signals for monitoring the patient's health status. These wearable sensors continuously monitor vital signs, like heart rate and blood pressure, when the patient with chronic heart disease is undergoing clinical involvement. Wearable devices are also applied in home-based rehabilitation interventions for continuous personal health monitoring. Wireless protocols can be integrated with wearable systems to facilitate long-term health monitoring for patients diagnosed with cardiac diseases. The wireless communication is relied upon and used to transmit the physiological data continuously to a central place (an access point or a mobile) and to remote central (server or emergency centre) via internet. In emergency situations, an alarm/alert signal can be transmitted to the remote emergency centre for facilitating medical assistance to patients. Family members or clinicians are also alarmed when the patient is in an emergency condition through the technology and enabled to monitor the patient's medical status continuously. Even though there are advantages of wearable devices, many future challenges should be addressed. This

primarily requires the support of innovative sensor technologies, especially Wireless Body Sensor Networks (WBSN), formed with various wearable biomedical sensors. Since the constraints on battery life and form factor are crucial, these sensors have a very stringent power requirement. To aid low cost, ultra-low power design is essential for developing wearable devices. In terms of cost, size, and performance, System-on-Chip (SoC) implementation is an attractive option.

In this chapter, the development and deployment of the wearable ECG SoC monitoring system are studied, regarding key technology perspective. The following sections present the prior art and essential components of wearable devices, System overview, Proposed ECG SoC, and Fuzzy Decision Maker Chip. Concluding remarks, observations, and future reservations are discussed in the final section.

2. Prior Art

Wireless Body Area Network (WBAN) is the fundamental component of a wireless ECG monitoring system. WBAN allows the integration of various other components, like intelligent systems, miniaturized components, low-power sensor nodes, etc. Therefore, the combination of SoC concepts, wearable technology, Wireless Sensor Network (WSN), and research in artificial intelligence produce novel approaches, resulting in better health care services. System-on-a-chip (SoC) is a felicitous option for device development because of its small size, low power consumption, and lower cost features. Developing SoC for Wireless Body Area Network applications intends to carry healthcare monitoring closer from clinical intervention to domiciles. It allows physiological signal monitoring to be conducted more regularly than limiting it to hospitals or clinics. WBSN is foreseen as the next generation health care monitoring platform, as it is considered a reliable, low-cost high-patient-safety health care monitoring system. In recent years, the development of ECG SoC for WSBN applications has attracted much attention [2,14]. A wearable monitoring system is proposed in [3] to monitor various physiological variables, such as ECG, blood pressure, and temperature. Also, the Global Positioning System (GPS) co-ordinates of patient or wearer with the acquired variables are transmitted wirelessly to a remote station.

Targeting patients with chronic high-risk heart/respiratory diseases, a wrist worn wearable medical monitoring and alert system (AMON) monitors physiological variables. For terrestrial and space applications, physiological parameters of the astronauts in space should be monitored continuously. To address the mentioned problem, a wearable system, called ‘Life Guard’, is proposed [4] to monitor the health status of astronauts. The deployment of a biopatch with integrated low-power SoC prototype is proposed by Yang et al. [5] to facilitate features, such as a three-stage front-end signal conditioning circuit, 8-bit successive-approximation-register (SAR) ADC, and a digital core. An integrated wireless ECG SoC for WBSN applications is proposed in [6], which comprises a two-channel ECG front-end, an 8-bit SAR-ADC, a simple micro-

controller, a SRAM memory, and RF-transceivers. Many ECG SoCs implementations for WBSN applications employ a microcontroller or microprocessor to establish the remote gateway [7,14]. In worst cases, there is a need for an artificial intelligence approach, integrated with wearable ECG SoC, when abnormal ECG episodes are to be detected instantly. This solution addresses diseases, like cardiac arrhythmia or silent myocardial ischemia, to be easily identified for clinical treatment. This increases the need for low cost and easy to use wearable wireless ECG sensors with integrated decision making to alert personnel. The following sections narrate about an ultra-low power ECG on Chip with integrated CMOS Fuzzy Decision Making Chip that addresses the issues in existing solutions.

3. Wearable ECG System: With Decision Making

3.1 System Overview

The proposed health care architecture includes two parts: (a) Main unit and (b) Remote unit, as shown in Fig.2. The Main unit contains wearable textile electrodes, designed ECG front-end chip, FDM chip, a controller, and a ZigBee transceiver. The remote unit (personal gateway) can be a mobile phone or a personal computer with an USB interface. The main unit records the ECG from wearable textile electrodes and wirelessly transfers the data to a remote unit. The designed ECG acquisition chip for low power use is described in the next sub-section. The ECG acquisition chip comprises: (1) specially designed textile electrodes for acquiring the ECG; (2) a miniature printed circuit board with ECG front end circuits; (3) Analog to Digital Conversion unit; (4) QRS Detection; and (4) System control unit. The ECG data is buffered, using low power microcontroller internal memory to minimize power consumption before wirelessly sending it to the remote unit. The main unit also performs the other tasks, such as system initialization, data buffering, and scheduling wireless communication. The Fuzzy Decision Making (FDM) chip (3×3 fuzzy controller; nine rules are accessible) takes decisions when necessary. Depending on applications, control voltages set on IC pins change the rules of fuzzy inference. The study of the Fuzzy chip is explained in detail in subsequent sections. ZigBee protocol is chosen as a wireless communication protocol (TI CC2420) to provide reasonable power consumption and adequate data rate. The prototype uses a low power TI MSP430 microcontroller for data management, wireless ZigBee baseband, and routing management. The prototype model is designed for patients, regarding comfort and ease of use, thus, not affecting regular activities of patients. In addition, the entire unit is sealed within a smart textile shirt. So, the patient can wear and remove it easily.

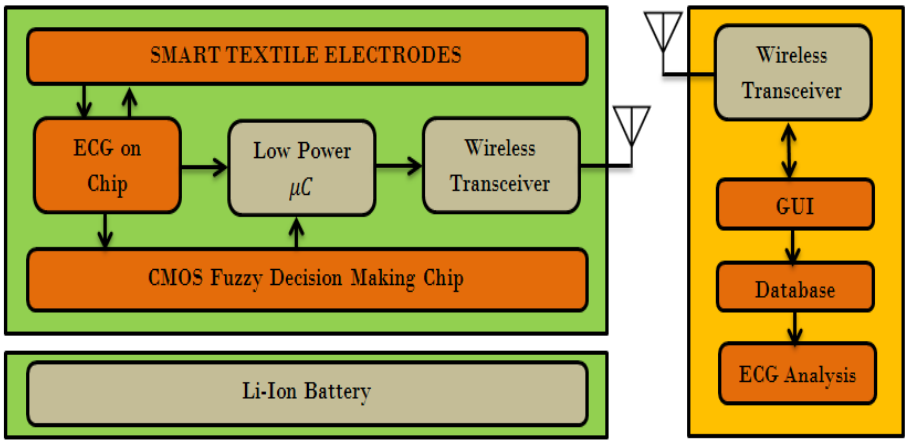


Fig. 2. Block diagram of proposed healthcare architecture

For various medical applications, the acquired physiological variables should be analyzed continuously. The remote unit (personal gateway) can be a mobile phone or a personal computer with an USB interface. The important functions of the remote unit are receiving the data wirelessly, database management, ECG analysis, graphical user interface (GUI) interface, and customization. To avoid signal interference from other wireless devices, the remote unit has specific authentication to process the received data. In addition, there are several options in the GUI interface for customization.

3.2 ECG on Chip

A. ECG Analog Front-end Amplifier

The ECG front-end amplifier is mainly responsible for noise suppression, signal conditioning, and amplification, which comprises two phases as shown in Fig.3, namely, low noise AFG with band pass function and a programmable gain amplifier (PGA) to amplify the acquired ECG signals (from textile electrodes), with amplitude in a few millivolts, adopting a flip-over-capacitor technique. The Low noise amplifier not only acts as a preamplifier, but also acts as a band pass filter function with bandwidth between 0.3 and 100 Hertz. In the AFG design, two switches (S1 and S2) are integrated to settle down quicker when power is applied, due to the large resistance by the pseudo-resistors. The speeding up of the AFG is done by a reset signal with an appropriate switch during startup of the system.

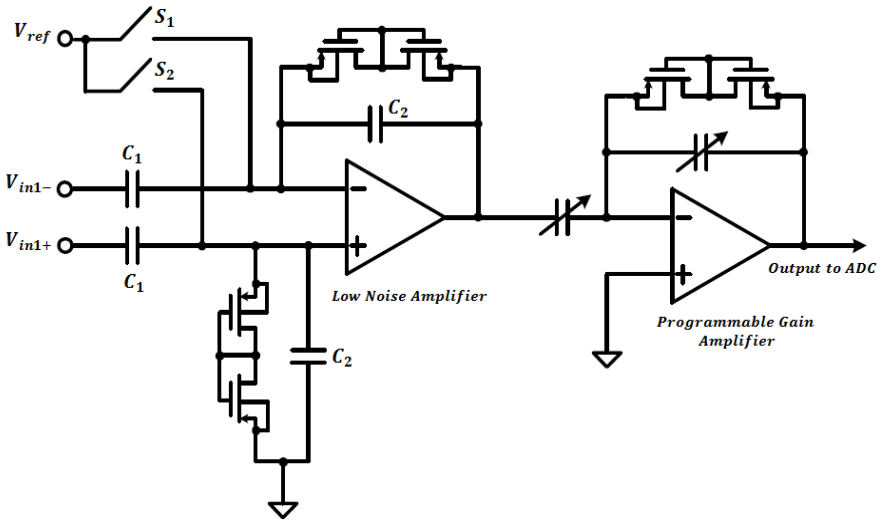


Fig. 3. Typical circuit diagram of ECG Front-end low noise amplifier

B. Analog to Digital Converter (ADC)

Successive Approximation Register (SAR) ADC is chosen for this WBSN application because of its moderate accuracy and low power overhead. Fig. 4 depicts the architecture of the SAR ADC, adopted from literature. The analog ECG output is driven directly by the preceding buffer stage, without the need of an additional hold amplifier, sampled through a bootstrapped switch and held in the capacitive 12 bit DAC, and is then used by open-loop Sample/Hold. The reason for open-loop Sample/Hold is to obtain low power, low cost, fast settling, and less offset error. The obtained analog ECG data are being compared with a reference (REF) and then level-shifted by the DAC. The fixed reference REF helps to compensate the dynamic offset error at the comparator. An on-chip crystal oscillator is used to drive the logic and timing sequence for achieving low power consumption and low jitter. The resultant digital codes are passed to a System Control Unit (SCU) after level conversion and to QRS complex detector for data processing.

C. Heart Rate Calculation and QRS Detection

The morphological filter [8] is adopted to reduce the noise artifacts present in the ECG data and to detect\estimate the QRS complex details and R-R intervals. The filter comprises a pair of Opening and Closing operations, using dilation and erosion operators, which suppress peaks and valleys. The flowchart for QRS complex detection is illustrated in Fig.5. The impacts of wandering baseline drift are eradicated by subtracting the mean result of operations (opening and closing) with the original input. The ECG samples are loaded serially into the shift register and then added/subtracted (for dilation/erosion respectively) with the structure element $g(x)$ [8].

The results are compared continuously, using a comparator tree to find the minimum/maximum (for dilation/erosion respectively). A moving average filter (serial structured) is used to reduce the impulse noises and smooth the filtered signal. The received signals are continuously compared against the adaptive threshold and monitored to detect the R-peaks. The current threshold is updated regularly when a new R-peak is identified. By counting the number of clocks between R peaks using a binary counter, R-R interval is measured. The Heart Rate (HR) variable is also calculated by simply counting the number of R-peaks in the last sixty seconds. A parallel-to-serial converter is integrated with the wearable system for transmitting the HR variable through the SPI interface.

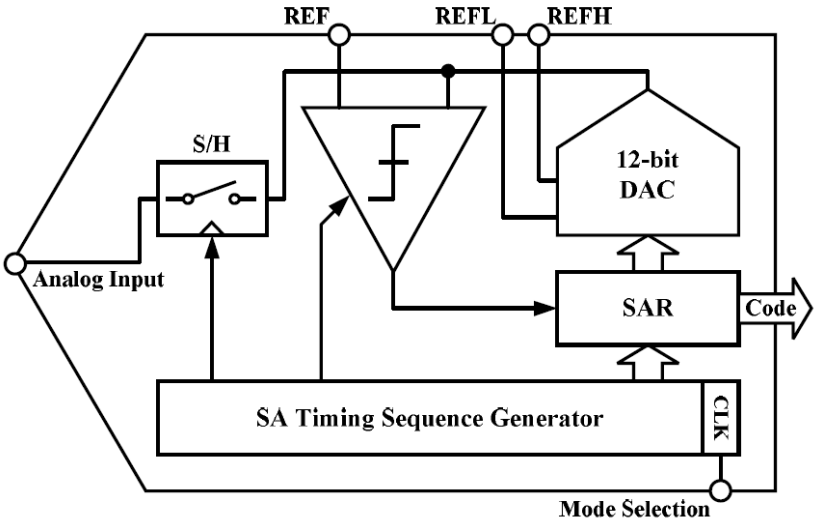


Fig. 4. Schematic Architecture of Successive Approximation ADC

D. System Control Unit and SPI Interface

System Control Unit (SCU) is solely responsible for generating the interface control signals, based on the host or main controller commands for all the blocks in ECG on-chip. Data framing, CPU interrupt handling, etc. are done by the SCU system, based on control signals, which are generated by state machine. In-order to interface the chip with various host CPUs, the System Control Unit uses an asynchronous FIFO with 8 Kb buffers. Data from the ADC and QRS block is continuously written into the FIFO at the sampling frequency of 256Hz. Based on the FIFO status, FIFO write/read controllers generate many status signals, which are “full”, “nearly full”, “empty”, and “nearly empty.” A microcontroller is employed externally to communicate with the proposed wearable device via a duplex SPI communication interface. The data link transmits QRS complex codes and ECG details with the internal FIFO status flags.

The control vector from external microcontroller is delivered to the internal control registers by the command link.

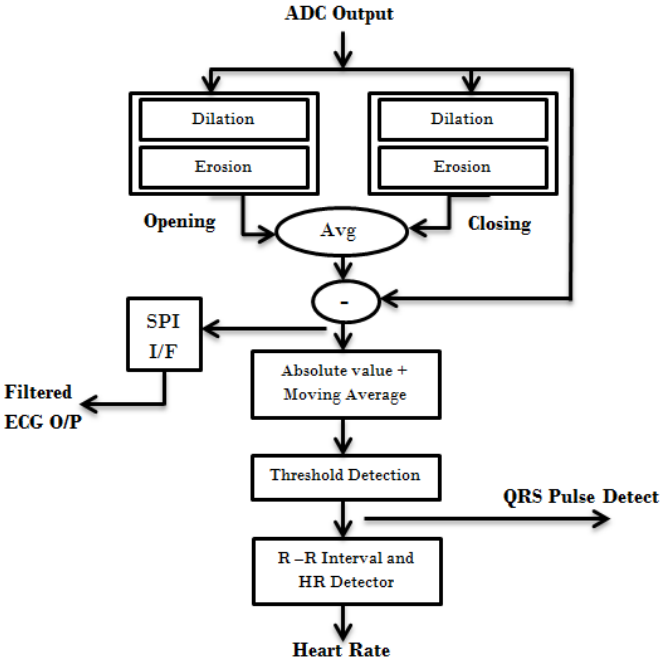


Fig. 5. Flow process for QRS Detection and HRV Calculation

3.3 Fuzzy Decision Making Chip: Concepts, Design and Implementation

In real world worst-case scenarios, there is a need for an artificial intelligence approach, integrated with a wearable ECG SoC, for detecting abnormal ECG episodes instantly. Especially, diseases like cardiac arrhythmia or silent myocardial ischemia should be identified immediately to alert the clinicians/family members for assistance. Therefore, a Fuzzy Classifier chip meets the critical requirements of medical applications: no delay in response, reliable, high-safety, and low cost. The functional blocks of the FDM chip are detailed in the following sections. It comprises three parts: fuzzifier, inference engine, and defuzzifier. In the fuzzifier, input variables (non-fuzzy) are mapped to the input membership functions. The inference engine handles fuzzy inference, depending on the inference method. Finally, the defuzzifier is used to convert the fuzzy output values from inference engine to non-fuzzy values.

Fuzzy Interface. The implemented architecture is a two-input one-output fuzzy supervisor. Each input has three trapezoidal membership functions or linguistic terms abbreviated as L (Low), M (Medium), and H (High), while the output variable is characterized by singletons. The parameters used for determining membership functions (V_{r+},V_{r-},V_{c+},V_{c-}) are calibrated by voltages applied on FDM IC pins. Since input membership functions have three parts, architecture is a 3×3 fuzzy controller, and nine rules are accessible. Depending on various applications, Control voltages set on IC pins can change these rules. The controller architecture in Fig. 6 is constructed with CMOS components, such as Membership function generator (MFG), MIN circuits and a defuzzifier (D blocks) circuit. A ramp function generation circuit is used for MFG. In fuzzy interface, three basic circuits are used: a ramp generator (RG) circuit [8], a minimum circuit, and a fuzzy complementary circuit. The membership functions for input and output variables of a controller are built, using two ramp functions. In Fig. 7, a form of trapezoidal membership function, using a ramp function and its parameters, is depicted.

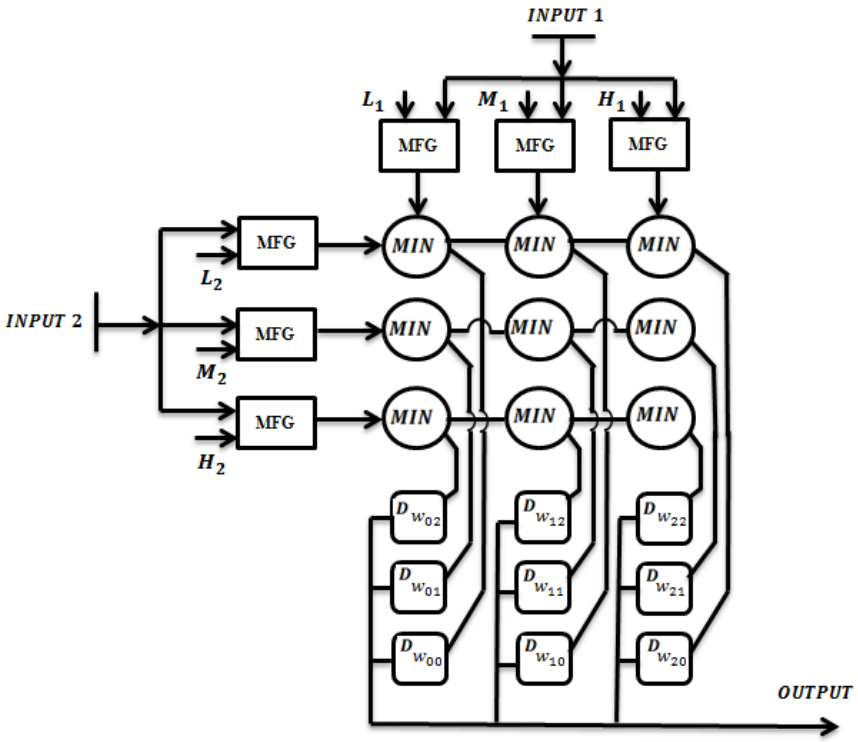


Fig. 6. Block diagram of Fuzzy Classifier

The membership functions are generated for input and output variables of a fuzzy decision supervisor. It shows that two ramp functions are necessary to build a membership function. The triangular membership function is a special case of trapezoidal membership function, when c and d coincide. The slope of the ramp functions and position of the membership functions must be tunable. Changing the parameters, a, b, c, and d allow the construction of different membership functions.

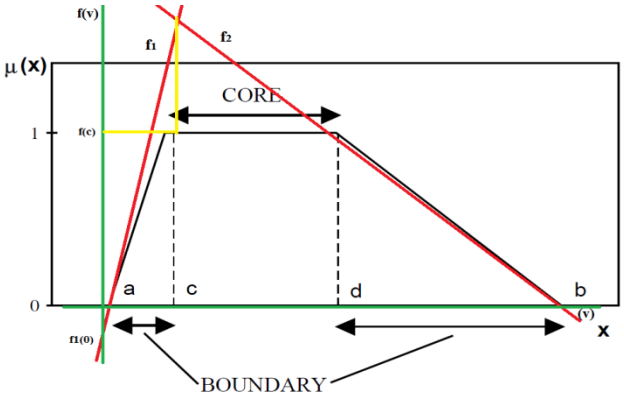
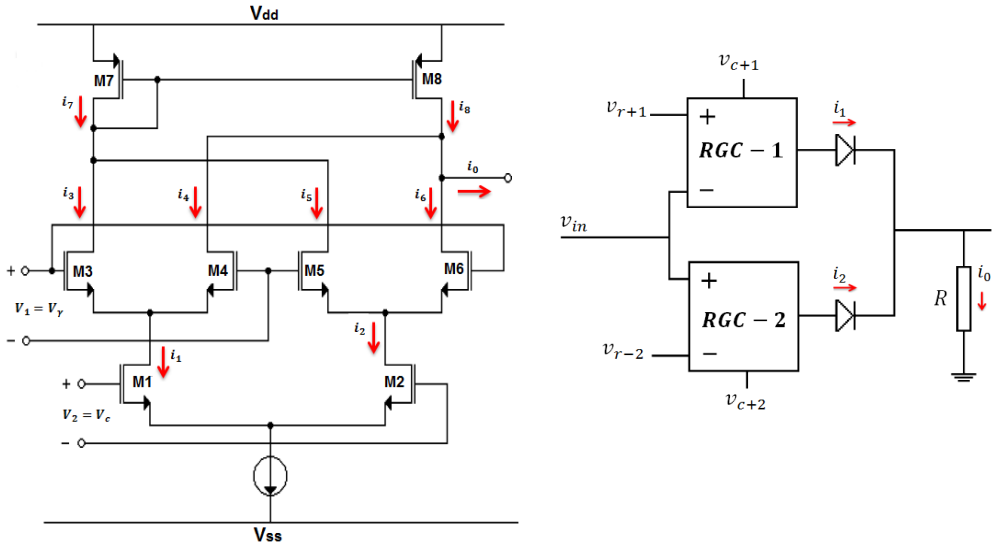


Fig. 7. Trapezoidal membership function and its parameters



(a) **(b)**

Fig. 8. Schematic of (a) Ramp generator circuit and b) CMFG

Fig. 8a shows the ramp generator circuit for membership function generation. It is assumed that all fuzzy sets are normalized. $\text{Supremum}_x(x) = 1$. In RG circuit, the output current i_0 is a function of v_1 and v_2. Considering I_{ss} fixed, and M3, M4, M5, and M6 are matched,

$$i_0 = i_3 + i_5 - (i_4 + i_6) = g_{m3}\frac{v_r}{2} - g_{m5}\frac{v_r}{2}\left(-g_{m4}\frac{v_r}{2} + g_{m6}\frac{v_r}{2}\right)$$
$$= \frac{v_r}{2}\left(\frac{I_1}{v_{gso3} - v_t} - \frac{I_2}{v_{gso5} - v_t} + \frac{I_1}{v_{gso4} - v_t} - \frac{I_2}{v_{gso5} - v_t}\right)$$
$$= \frac{v_r}{2}\left(\frac{2I_1}{v_{gso3} - v_t} - \frac{2I_2}{v_{gso5} - v_t}\right),$$

Where, all $v_{gso}'s$ are gate to source voltages in quiescent point, and also

$$I_1 = \frac{I_{ss}\frac{v_c}{2}}{v_{gso1} - v_t}, \quad I_2 = \frac{-I_{ss}\frac{v_c}{2}}{v_{gso2} - v_t}$$

Using previous equations, assuming M1 and M2 are also matched, then

$$i_0 = \frac{I_{ss}}{v_{gso1} - v_t}\left(\frac{1}{v_{gso3} - v_t} + \frac{1}{v_{gso5} - v_t}\right)v_r v_c$$

Assuming v_c is set to be a constant value, hence $v_{gso1} - v_t$ is constant. Also, changes of $v_{gso3} - v_t$ and $v_{gso5} - v_t$ are in opposite directions. So $\left(\frac{1}{v_{gso3} - v_t} + \frac{1}{v_{gso5} - v_t}\right)$ is approximately constant.

Therefore, $i_0 = kv_1v_2$

Where,

$$k = \frac{I_{ss}}{v_{gso1} - v_t}\left(\frac{1}{v_{gso3} - v_t} + \frac{1}{v_{gso5} - v_t}\right)$$

The RG circuit can generate both a positive and negative slope ramp function. Suppose $v_{c-} = 0, v_{c+}$ and v_{r-} are constant, then

$$i_0 = k(v_{r+} - v_{r-})(v_+) = kv_{c+}v_{r-} - kv_{c+}v_{r-} = mv_{r+} - n$$

Where,

$$m = kv_{c+}, \quad n = kv_{c+}v_{r-}$$

Thus, a positive slope ramp is generated.

Similarly, if $v_{c+} = 0$, and let v_{c-}, v_{r-} be constant, then

$$i_0 = k(v_{r+} - v_{r-})(-v_{c-}) = -kv_{c-}v_{r+} + kv_{c-}v_{r-} = -mv_{r+} - n$$

Where,

$$m = kv_{c-}, \quad n = kv_{c-}v_{r-}$$

Therefore, by changing $v_{r+}, v_{r-}$and v_c, different ramp functions are generated. It is evident that the output voltage of RG circuit

$$v_0 = R_{out}i_{out}$$

Where R_{out} is output resistance.

Two ramp functions f_1 and f_2 with positive and negative slopes, respectively, are shown in Fig.7. Assuming RG circuit has generated these functions, f_1 and f_2 can be equated as below

$$f_1 = m_1 v - n_1$$
$$f_2 = n_2 - m_2 v$$

To construct a tunable membership function,

$$f_1(0) = -n_1 = -k v_{r1-} v_{c1+}$$
$$f_2(0) = n_1 = k v_{r2-} v_{c2-}$$
$$a = v|_{f_1=0} = \frac{n_1}{m_1} = \frac{k v_{r1-} v_{c1+}}{k v_{c1+}} = v_{r1-},$$
$$b = v|_{f_2=0} = \frac{n_2}{m_2} = \frac{k v_{r2-} v_{c2+}}{k v_{c2+}} = v_{r2-},$$

When $f_1 = f_2$, can be written as $m_1 c - n_1 = -n_2 + m_2 c$
Therefore,

$$c = \frac{n_1 - n_2}{m_1 - m_2} = \frac{v_{r1-} v_{c1+} - v_{r2-} v_{c2-}}{v_{c1+} - v_{c2-}}$$

With this value for c,

$$f(c) = f_1(c)$$
$$= f_2(c) = \frac{k v_{c1+} v_{c2-}}{v_{c1+} - v_{c2-}} (v_{r1-} - v_{r2-})$$

To construct a fuzzifier with desirable capabilities, Set $v_{r1-} = v_{r2-}$. A reverse triangular in the positive region of vertical axis will be formed as shown in fig.7. By clipping this triangular area with a constant value E, a controllable membership function can be obtained.

In this case,

$$a = v|_{f_2=E} = \frac{n_2 - E}{m_2} = v_{r2-} - \frac{E}{k v_{c2-}},$$
$$b = v|_{f_1=E} = \frac{E - n_1}{m_1} = \frac{E}{k v_{c1+}} - v_{r1-},$$

Varying v_{c1} and v_{c2} results in a change in a and b. For $v_{r1} = v_{r2}$, it will also be variable. The position of the membership function can be changed. Note that a trapezoidal membership function is obtained when $v_{c+} > v_{c-}$ and in this case, $c = v_{c-}$ and $d = v_{c+}$. Considering these points, it is necessary that c and d are selected equal to v_{r1} and v_{r2}, respectively, and then by changing v_{c1} and v_{c2}, a and b are determined. Diodes are used to eliminate the extra parts of membership function. Since two ramp functions are needed, two RG circuits are used for each membership function. The typical circuit diagram of complementary membership function generator (CMFG) is shown in Fig.8b and adapted from [8]. Considering the output voltage $v_{0ut} = R i_o$
Where,

$$i_0 = \begin{cases} i_1 = k(v_{1+} - v_{in})v_{c1+};\ v_{r1+} f v_{in} \\ i_2 = k(v_{in} - v_{r2-})v_{c2-};\ v_{r2-} p v_{in} \end{cases}$$

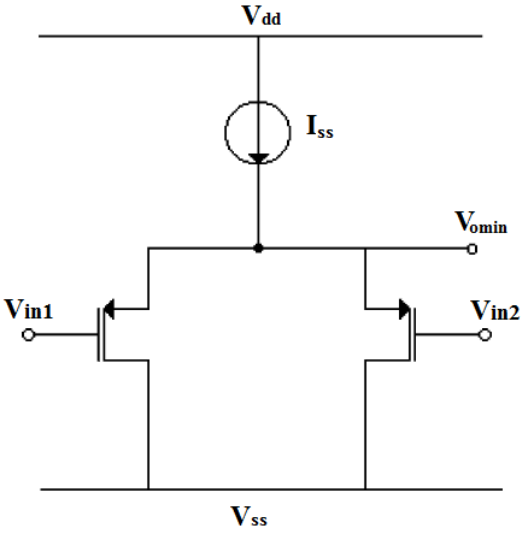


Fig. 9. Schematic representation of Minimum Circuit

Minimum circuits can be used to clip the extra curves and then reverse it by a fuzzy complementary circuit (FCC). Fig.10. illustrates the circuit diagram of a fuzzy complementary circuit. In FCC, the two inputs are connected to the gates of the transistors. A multi-input minimum circuit with over two transistors is needed in applications, such as three-input fuzzy controllers. As illustrated in Fig.9, the output voltage $v_{o(min)}$ always takes the smaller value of two inputs $v_{in1}$and $v_{in2}$with a positive offset voltage v_{offset}.

$$v_{o(min)} = \min(v_{in1}, v_{in2}) + v_{offset}$$

This result $v_{o(min)}$ specifies that the offset voltage is about 1 Volt. To compensate the offset voltage, v_{off} a negative level shifter circuit is necessary. The Negative shift is achieved by a fuzzy complement circuit with a reference voltage of E. The complementary membership function must be converted to an ordinary membership function, achieved by a fuzzy complementary circuit of two g_m circuits.

From Fig.10, assuming the reference voltage E = 0,

$$v_{comp} = R_i = R(i_1 + i_2) = R\left(-g_m v_{in} - g_m v_{comp}\right)$$

Therefore, this is opposite to the input voltage. The complement of the membership function is $E \neq 0$,

$$v_{comp} = E - v_{in}\ if\ \ Rg_m \gg 1$$

Note that, in the final fuzzifier structure, E must be set to compensate offset voltage, associated with the minimum circuit. The attenuation is due to the limited gain of Rg_mthat is equal to $-Rg_m$=$1 + Rg_m$. This attenuation is the same in each one of the

fuzzifiers used in the controller, and the error due to attenuation does not affect fuzzy processing considerably. If the input signal has a negative DC value, then E must be chosen to be greater than the Supremum value by $|V_{dc}|$.

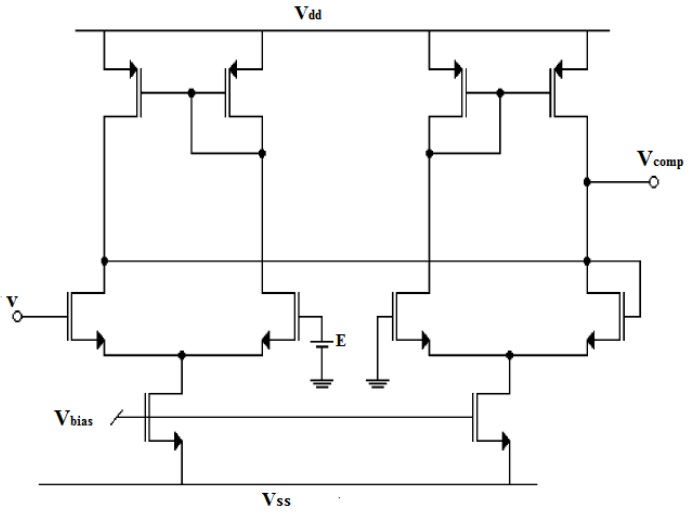


Fig. 10. Schematic diagram of Fuzzy Complementary Circuit

Inference Engine. With Mamdani's inference technique, the inference engine is accomplished by a set of intersection and union operations [10,12]. The Min- Product inference method is chosen for inferencing in which a minimum of two inputs can be specified. Nine two-input minimum circuits in the inference engine are needed. Therefore, the controller has two inputs with three membership functions. The Min blocks [10] and their synthesis in the complete controller structure will do the inferencing.

Defuzzification. A novel defuzzifier is used [8,10] in which the center of the area is calculated without employing a division circuit. Therefore, it occupies a small chip area. The main idea is based on parallel conductances g_n, stating implicitly that the output voltage of the defuzzifier circuit is the average value of the inputs. The contribution of each input to the output is weighted by the conductance g_i that is a controllable variable. The below equation provides a non-fuzzy or defuzzifier output.

$$V_{defuzz} = \frac{g_1 V_1 + g_2 V_2 + \cdots + g_n V_n}{g_1 + g_2 \ldots\ldots + g_n}$$

MOS transistor is used as a controllable g-element in this work. Offset voltage v_t in a MOS transistor must be cancelled to control g_{ds} by v_{gs} $(g_{ds} = kv_{gs})$ linearly.

$$g_{ds} = k(v_{gs} - v_t); k = \frac{1}{2}\mu c_{ox}\frac{W}{L}$$

Level shifter circuit (LSC) is used to compensate offset voltage [8]. The complete schematic diagram of defuzzifier is depicted in Fig.11.

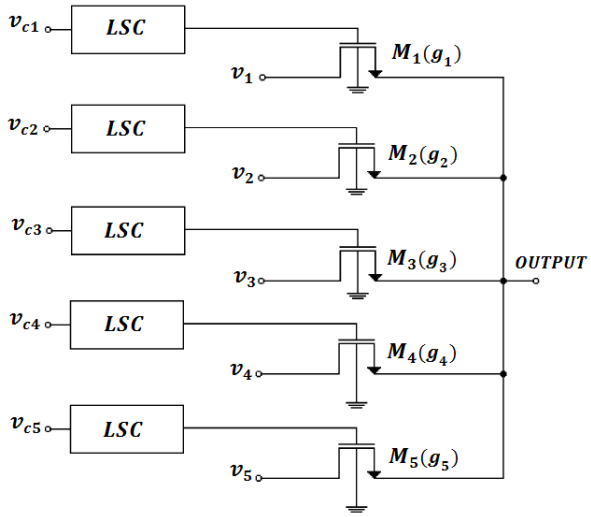


Fig. 11. Schematic Illustration of Defuzzifier

4. Results and Discussion

The wearable ECG sensor node system fits perfectly on a shirt. The main unit provides a versatile framework for incorporating sensing, monitoring, and information processing devices. The designed wearable device can be deployed in a variety of applications, such as public safety, health monitoring, and sports. The vital signal monitoring functionality of the smart shirt is tested in real time. The inference performance test is done, based on physical activity under various conditions. The abnormal ECG signal is measured and stored in the fuzzy inference engine. The fuzzy decision making rules are framed in such a way that, when an abnormal ECG signal is detected, an alert signal is sent promptly to the remote gateway via microcontroller. A wearable smart shirt transfers the physiological ECG signals over a wireless sensor network at the test. The following sections depict the important results of the proposed system.

4.1 ECG Acquisition

To ensure comfort, the clothing is designed from a knitted conductive textile fabric for reducing flammability. Rectangles of electrically conductive textile fabric in knitted design were stitched on the position of the pectoral muscles [13]. The conductive textile fabric is realized from a blended yarn of the composite containing silver nanoparticles, which provide electrical conductivity of the yarn and the resultant knitted fabric. The content of silver nanoparticles provides corrosion resistance of textile electrodes, antibacterial and anti-allergic properties, and mechanical and electrical stability when exposed to sweat. The design of blended conductive textile fabric, made from conductive yarn, enables traditional maintenance of T-shirts (washing, ironing) and long-term stability of surface conductivity of the electrodes with a high number of wash cycles. The designed conductive textile fabrics are circular in shape, with dimensions 5 × 5 cm. Fig.12 shows the wearable electrodes, which comprise a conductive fabric electrode pair and the wearable sensor node system placed on the wearer's chest placement. To provide a sufficient potential difference, the electrodes are positioned 100 mm apart. The ECG measurements are obtained through wearable textile electrodes (Zero Resistance, 100% Silver fiber for conductive part), and the acquired ECG signals are processed, using other modules in this health architecture for decision making.

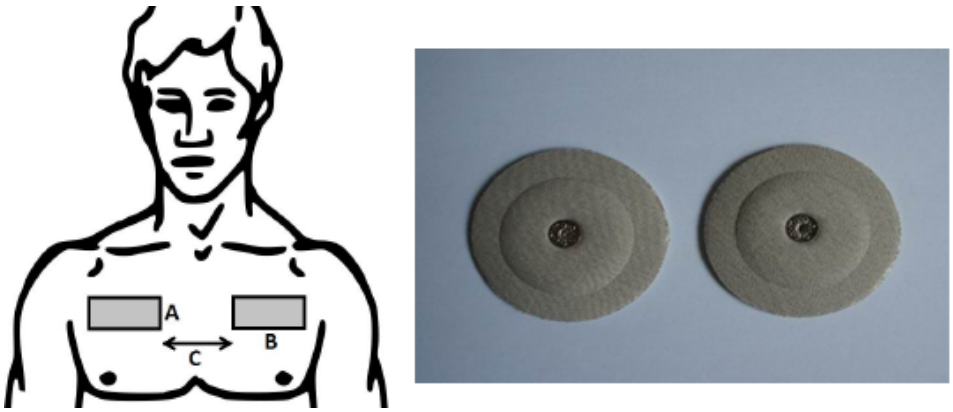


Fig. 12. Placement of wearable textile electrodes

4.2 Fuzzy Decision Making

In the FDM module, the Heart rate variability (HRV) is computed from the time series R-R intervals (R-peak to R-peak), converted into a uniformly sampled time-spaced sequence. As the physiological condition (wakefulness state, sleep state, etc.) of a patient changes, the power spectral density (PSD) of heart rate differs. The low-to-high (L/H) frequency ratio is considered an effective assessment and indicator of

such change, because it reflects the balancing action of the sympathetic and parasympathetic nervous-system branches. Power Spectral Density of HR variations is calculated, and the three frequency bands, such as Very low frequencies (VLF: 0-0.04 Hz), Low frequencies (LF: 0.04-0.15 Hz), and High frequencies (HF: 0.15-0.5 Hz), have been utilized. The features extracted from HRV and PSD are used to feed the fuzzy logic engine that computes epoch-by-epoch (30 or 60 seconds per period) inferences. The fuzzy inference rules are based on the observed details of normal and abnormal ECG signals. The inputs of FDM chip are details of QRS complex and PSD results. The ranges of membership functions are tunable by changing the voltages of FDM IC pins, which is done by the developer via microcontroller.

The FDM chip provides the index values (i.e., defuzzified output in the range of 0 - 2), which is sent to the microcontroller. Hence, there are output states, such as normal, sleep onset/fatigue, and abnormal, decoded by microcontroller unit. A set of meaningful rules has been framed. The following are the strongest:

IF HR Variability is Low **AND** LF/HF ratio is Medium
THEN the Output signal is SLEEP_ ONSET

IF HR Variability is High **AND** LF/HF ratio is High
THEN the Output signal is NOR_WAKE

IF HR Variability is Low **AND** LF/HF ratio is Low
THEN the Output signal is DROWSY

Fig. 13 shows the major difference between normal and abnormal ECG signals, noting that an abnormal ECG data has an elevated T wave.

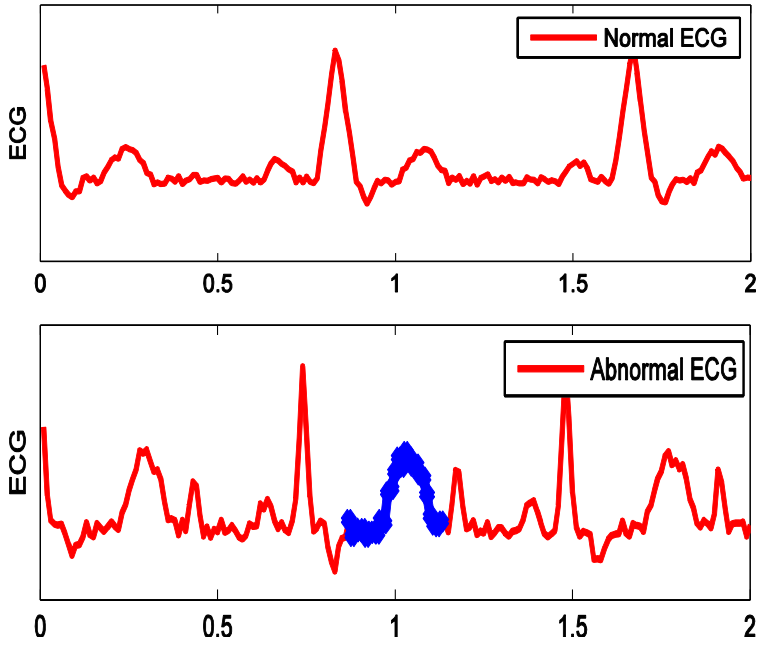


Fig. 13. Measured sample ECG data for Inference Engine

4.2 Performance Evaluation

The status is continuously sent to the remote unit every 2 minutes or preset time in the controller. The results of the experiments, as shown in Table 1, confirmed our hypothesis that human health status can be predicted by the FDM module through extracted ECG features. Detection succeeds, based on ECG signal captured from the wearable textile electrodes. When the signal is sensed, the system detects the status, and if abnormal, an alert signal is transmitted. Measurement accuracy of Fuzzy based ECG classification confirms to be robust enough to perform over 95% successful early detections. Therefore, the proposed system can make decisions, based on the acquired ECG data.

Table 1. Performance Evaluation of Fuzzy Decision Making in the proposed system

Rule-Check	Clinical datasets			
	Number of data sets used for testing	Number of data sets correctly classified	Number of data sets wrongly classified	Accuracy (%)
Drowsiness	21	19	2	90
Sleep Onset	19	18	1	94

Normal	23	23	0	100
Rule-Check	Simulated datasets			
	Number of data sets used for testing	Number of data sets correctly classified	Number of data sets wrongly classified	Accuracy (%)
Drowsiness	89	82	7	92
Sleep Onset	102	98	4	96
Normal	213	213	0	100

Fig.14 depicts the designed graphical user interface for the proposed architecture. Timing of the early detection capability of each system is also evaluated during the tests.

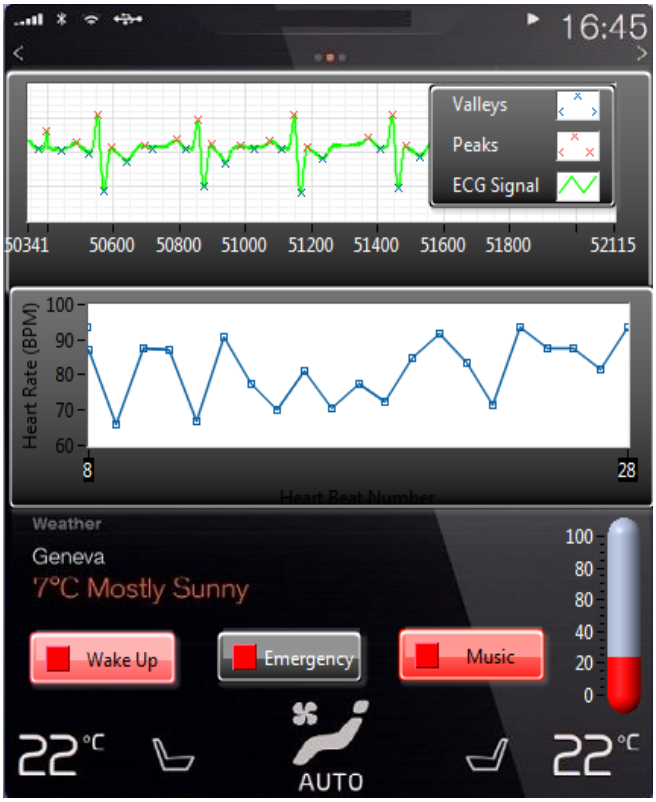


Fig.14. Designed Graphical User Interface for testing and measurements

5. Concluding remarks

A wireless ECG on a chip with an integrated Fuzzy Decision making system is proposed for real-time ECG health monitoring. The proposed wearable device is small, user-friendly, has a long battery life, and is capable of wirelessly transmitting ECG data continuously to a remote station for detailed diagnosis. The FDM chip is integrated with ECG on Chip to take the decisions for alerting the patients when necessary. The designed FDM responds immediately when anomalies are found in ECG data. The proposed device has already been tested with a reference high-quality measurement system for verification of accuracy and showed that the accuracy of the proposed device is good enough, and the variation in key ECG parameters obtained from the proposed device and the reference device is acceptable for clinical usage.

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6. References

1. C.Y. Chen, C.L.Chang,C.W.Chang, S.C.T. Lai, F. Chien, H.Y. Huang, J.C. Chiou, C.H. Luo. A Low-Power Bio-Potential Acquisition System with Flexible PDMS Dry Electrodes for Portable Ubiquitous Healthcare Applications. *Sensors, 13*: 3077–3091, 2013.
2. Manikandan Pandiyan, Geetha Mani, Jovitha Jerome, Natarajan Sivaraman. Integrating wearable low power CMOS ECG acquisition SoC with decision making system for WSBN applications. *2015 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, 154-158, 5-7 Oct. 2015.
3. P.S. Pandian et al. Wearable multi-parameter remote physiological monitoring system, *Med. Eng. Phys.,* 30 (4): 466–477, 2007.
4. U. Anliker, J.A. Ward, P. Lukowicz, et.al. AMON: a wearable multi parameter medical monitoring and alert system. *IEEE Trans. Inf. Technol. Biomed*, 8 (4): 1–11, 2004.
5. G. Yang, L. Xie, M. Mantysalo, J. Chen, H. Tenhunen, and L. R. Zheng. Bio-patch design and implementation based on a low-power system-on-chip and paper-based inkjet printing technology. *IEEE Trans. Inf.Technol. Biomed*, 16(6): 1043–1050, 2012.
6. M. Khayatzadeh, X. Zhang, J. Tan, W. S. Liew, and Y. Lian. A 0.7-V 17.4-μW3-lead wireless ECG SoC. *IEEE Trans. Biomed. Circuits Syst.*, 7(5): 583–592, Oct. 2013.
7. N. Halin, M. Junnila, P. Loula, and P. Aarnio. The Life Shirt system for wireless patient monitoring in the operating room. *J. Telemed. Telecare,* 11: 41–43, 2005
8. Hamed Peyravi, Abdollah Khoei, Khayrollah Hadidi. Design of an analog CMOS fuzzy logic controller chip. *Fuzzy Sets and Systems*, 132: 245 – 260, 2002.
9. SS Lobodzinski, MM Laks. New devices for very long-term ECG monitoring. *Cardiol J.,* 19(2): 210–4, 2012.

10. Manikandan Pandiyan, Geetha Mani. Embedded low power analog CMOS Fuzzy Logic Controller chip for industrial applications. *2015 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC),* 43-48, 5-7 Oct. 2015
11. N Van Helleputte, JM Tomasik, W Galjan, A Mora-Sanchez, D Schroeder, Krautschneider WH, R Puers. A flexible system-on-chip (SoC) for biomedical signal acquisition and processing. *Sens Actuators A*, 142(1):361–368, 2008.
12. P Manikandan, M Geetha and Jovitha Jerome. Weighted fuzzy fault tolerant model predictive control. *IEEE International Conference on Fuzzy Systems (FUZZ-IEEE)*, 83-90, IEEE, 2014.
13. L Vojtch, R Bortel, M Neruda and M Kozak. Wearable Textile Electrodes for ECG Measurement. *Advances in Electrical and Electronic Engineering*, 11(5): 410-414, 2013.
14. G Lopez, V Custodio, J I Moreno and Lobin. E-textile and wireless-sensor-network-based platform for healthcare monitoring in future hospital environments. *IEEE Transactions on Information Technology in Biomedicine*, 14(6):1446-1458, 2010.