Design Methodology for an All CMOS Bandgap Voltage Reference Circuit

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Abstract. The Internet of Thing (IoT) has given rise to the integration of smart systems in the industrial, healthcare, and social environments. These smart systems are often implemented by system-on-chip (SoC) solutions that require power management units, sensors, signal processors, and wireless interfaces. Hence, an independent voltage reference circuit is crucial for obtaining accurate measurements from the sensors and for the proper operation of the SoC. Making, bandgap circuits indispensable in these types of applications. Typically, bandgap circuits are implemented using bipolar transistors to generate two voltages with opposite temperature coefficients (Complementary To Absolute Temperature – CTAT; Proportional do Absolute Temperature - PTAT) which are added resulting in a temperature independent voltage reference. The disadvantage of using bipolar devices is that the power supply voltage must be larger than the ON base-emitter voltage, resulting in voltages larger than 0.7 V. The low power demands of IoT and of technology scaling, have forced lower values for the power supply voltage and thus new bandgap circuits using only CMOS transistors have gathered increased interest. In these, the MOS transistors operate in the weak inversion region where its current has an exponential relation with its gate-to-source voltage, as in the bipolar devices. Making it possible to generate both the PTAT and the CTAT voltages and thus produce a temperature independent voltage reference. This paper describes a design methodology of an all CMOS bandgap voltage reference circuit, in which one of the transistors works in the moderate region and the other in the weak inversion, to achieve the lowest possible voltage variation with temperature. The circuit produces a voltage reference of 0.45 V from a minimum power supply voltage of 0.6 V, with a total variation of 1.54 mV, over a temperature range of -40 to 100 ºC, resulting in a temperature coefficient of 24 ppm/ºC, and a power supply rejection ratio (PSRR) of -40 dB.

Keywords: Low-voltage CMOS Bandgap Voltage Reference, Analog Design Methodology, Weak Inversion Operation.

1 Introduction

Reference voltage generators are required in almost any Internet of Thing (IoT) System on Chip (SoC). To ensure the proper behavior of these systems, these reference voltages should be stable, independently of variations in: environment temperature, supply voltage, and fabrication process. The bandgap reference (BGR) is the most commonly voltage reference generator used [1]. Typically, a bandgap produces a constant reference voltage by summing two temperature dependent voltages – one Proportional to Absolute Temperature (PTAT) and the other Complementary to Absolute Temperature (CTAT). Most of the bandgaps uses the V_{BE} of a bipolar transistor to generate both CTAT and PTAT voltages [1][2][3]. However, due to the technology scaling and the need to reduce power consumption, the supply voltage has been greatly reduced. At supply voltages bellow 1 V, bipolar transistors are not suitable since they need a minimum V_{BE} value of 0.7 V to be turned ON. Therefore, to keep pace with this decrease in the power supply several all CMOS bandgap reference voltage circuits have been proposed [4][5][6][7][8]. In these new topologies, the PTAT and CTAT voltages are generated by using a MOS transistor in the weak inversion (or subthreshold region). In this region the transistor current depends exponentially on the gate-to-source voltage (V_{gs}), similar to the bipolar transistor. This paper describes a complete design methodology and simulation test of an all CMOS bandgap, in order to achieve the best performance.

2 Relationship to Smart Systems

The smart systems together with IoT play an important role on the new generation of information technology and it is predicted to have a major impact in the human life in the near future. This relatively recent technology aims to enable things to be connected anytime, anywhere, with anything and anyone ideally using any path/network or service. Such systems must be small, low power, and durable, hence they are often implemented by SoC solutions, that contain power management units, sensors, signal processors, and wireless transceivers. All this circuits and sensor require constant reference voltages so that they can work properly and obtain accurate and precise measurements. Moreover, since smart systems can be placed in any kind of environment, these reference voltages must be stable and robust even in harsh environments where the temperature variation can be high.

3 Proposed Circuit and Design Methodology

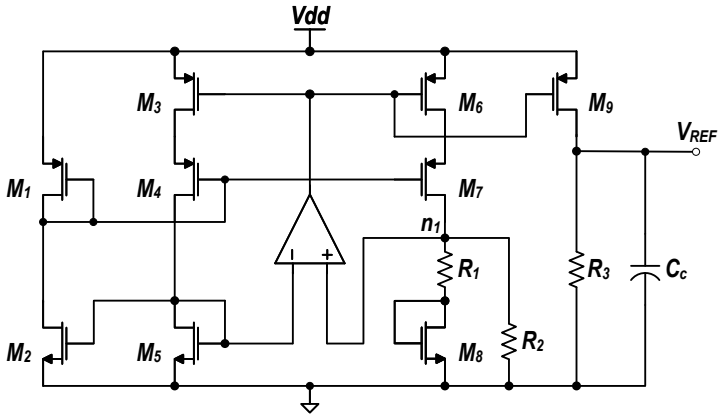

Fig. 1 Simplified schematic of the proposed Bandgap circuit.

Fig. 1 shows the simplified schematic of the all CMOS bandgap voltage reference circuit [5], where the operational amplifier was implemented using a simple two stage miller compensated amplifier. The diode connected transistors $M_{5,8}$ operate in the weak inversion region where their current varies exponentially with $V_{gs_{5,8}}$. Thus, $V_{gs_{5,8}}$ is given by (1) where I_{D0} is the technology current, n is the substrate value, V_T is the thermal voltage, L and W are the transistor length and width, and V_{th} is the threshold voltage. For the 130 nm CMOS technology the value of I_{D_0} and n for an NMOS transistor were determined by simulation and are 0.9 μA, and 1.17, respectively.

$$V_{gs} = n\,V_T\,\ln\left(\frac{I_D\,L}{I_{D_0}\,W}\right) + V_{th} \tag{1}$$

The transistors $M_{5,8}$ along with the resistances $R_{1,2}$ are responsible for the generation of a PTAT and CTAT current. The values of these currents can be derived by applying KCL to node n_1 (2), where it is assumed that the amplifier gain is high so that $V^- = V^+$, and that the current I_D is equal in all the four branches of the circuit and so it can be derived through Ohm's law (3).

$$\frac{V_{gs_5} - V_{gs_8}}{R_1} + \frac{V_{gs_5}}{R_2} - I_D = 0 \tag{2}$$

$$I_D = \frac{V_{REF}}{R_3} \tag{3}$$

Considering $L_5 = L_8 = L,\ V_{th5} = V_{th8}, I_{D_{0_5}} = I_{D_{0_8}} = I_{D_0}, n_5 = n_8 = n,\ I_{D_5} \approx I_{D_8} \approx I_D$ and $W_5 = K\,W_8$, then $V_{gs_5} - V_{gs_8}$ from (2) can be replaced by (1), resulting in

$$V_{gs_5} - V_{gs_8} = n_5\, V_T \ln\left(\frac{I_{D_5}\, L_5}{I_{D_{0_5}}\, W_5}\right) + V_{th_5} - n_8\, V_T \ln\left(\frac{I_{D_8}\, L_8}{I_{D_{0_8}}\, W_8}\right) - V_{th_8} =$$

$$= n\, V_T \ln\left(\frac{\frac{I_{D_5}\, L_5}{I_{D_{0_5}}\, W_5}}{\frac{I_{D_8}\, L_8}{I_{D_{0_8}}\, W_8}}\right) = n\, V_T \ln\left(\frac{\frac{I_D\, L}{I_{D_0}\, W_5}}{\frac{I_D\, L}{I_{D_0}\, K\, W_5}}\right) = n\, V_T \ln(K) \tag{4}$$

Replacing (4) and (3) in (2) results

$$\frac{n\, V_T \ln(K)}{R_1} + \frac{V_{gs_5}}{R_2} - \frac{V_{REF}}{R_3} = 0 \leftrightarrow$$

$$\leftrightarrow \frac{V_{REF}}{R_3} = \frac{n\, V_T \ln(K)}{R_1} + \frac{V_{gs_5}}{R_2} \leftrightarrow V_{REF} = \frac{R_3}{R_2}\left(V_{gs_5} + \frac{R_2}{R_1}\, n\, V_T \ln(K)\right) \tag{5}$$

Hence, the variation of V_{REF} over the temperature T is given by

$$\frac{\partial V_{REF}}{\partial T} = \frac{R_3}{R_2}\left(\frac{\partial V_{gs_5}}{\partial T} + \frac{R_2}{R_1}\, n\, \ln(K)\frac{\partial V_T}{\partial T}\right) = \frac{R_3}{R_2}\left(\frac{\partial V_{gs_5}}{\partial T} + M\frac{\partial V_T}{\partial T}\right) \tag{6}$$

where $M = \frac{R_2}{R1} n \ln(K)$. In order for V_{REF} to be constant its derivative must be equal to zero,

$$\frac{R_3}{R_2}\left(\frac{\partial V_{gs_5}}{\partial T} + M\frac{\partial V_T}{\partial T}\right) = 0 \leftrightarrow M = \left|\frac{\frac{\partial V_{gs_5}}{\partial T}}{\frac{\partial V_T}{\partial T}}\right| = \left|\frac{634.5\times10^{-6}}{86.3\times10^{-6}}\right| = 7.35 \tag{7}$$

where $\partial V_T/\partial T = k/q = 86.3\ \mu\text{V/°C}$, in which k is the Boltzmann constant ($k = 1.38\times10^{-23}$ J/K) and q is the elementary charge ($q = 1.60\times10^{-19}$C). By simulating a NMOS diode connected transistor biased by a current (Fig. 2). source it possible to determine the V_{gs} variation with temperature (Fig. 3). The current was set to 500 nA and $L = 10$ µm, the temperature was swept from -40 to 100 ºC for different W values (1 µm, 5 µm, 10 µm, and 20 µm). As expected from (1) as W decreases V_{gs} increases. Also, V_{gs} decreases with the increase in the temperature, i.e. it has a negative temperature coefficient like the bipolar transistors. For the chosen current and L values, and knowing that $V_{th} = 0.220$ V (extracted by simulation), then W must be higher than 5 μm to be in the moderate region ($V_{gs} \approx V_{th}$) or weak inversion ($V_{gs} < V_{th}$) using even higher W values. Table 1 shows the slope, i.e. $\partial V_{gs}/\partial T$, for each W value from Fig. 3. Using the value of Table 1 obtained through simulation for $W_5 = 5$ µm results in $M = 7.35$ (7).

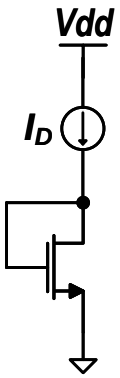

Fig. 2 Simplified schematic of the test bench to determine $\partial V_{gs}/\partial T$.

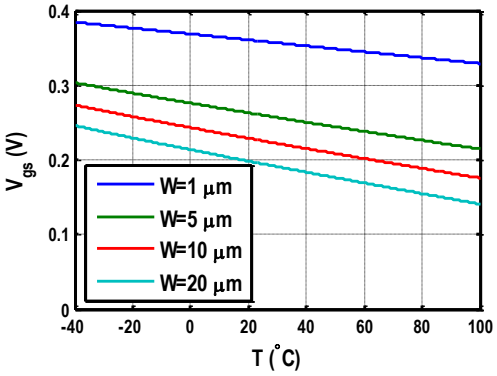

Fig. 3 Simulation results of the V_{gs} as a function of the Temperature for different W using the test bench of Fig. 2 with $I_D = 500$ nA and $L = 10$ µm.

Table 1. Simulation results of $\partial V_{gs}/\partial T$ of an NMOS transistor with $L = 10$ µm and $I_D = 500$ nA.

W(µm)	$\frac{\partial V_{gs}}{\partial T}$ (µV/°C)
1	-395.6
5	-634.5
10	-697.7
20	-750.4

The sizing of the resistors $R_{1,2,3}$ was performed using the same method used in [2]. Where the total resistance value was set according with the area constraints which resulted in a total resistance (R_{total}) value of 4 MΩ. Then, at room temperature ($T = 300$ K), $V_{gs}(W = 5\ \mu m) = 258$ mV, $V_T = 0.026$ V, $V_{REF} = 0.45$ V, $K = 4$ (for employing common centroid techniques), then

$$V_{REF} = \frac{R_3}{R_2}\left(V_{gs_5} + M\,V_T\right) \leftrightarrow 0.45 = \frac{R_3}{R_2}\,(0.258 + 7.35{\times}0.026) \tag{8}$$

$$M = \frac{R_2}{R_1} n\,\ln(K) \;\leftrightarrow 7.35 = \frac{R_2}{R_1}{\times}1.17{\times}\ln(4) \tag{9}$$

$$R_{total} = R_1 + R_2 + R_3 = 4{\times}10^6\ \Omega \tag{10}$$

Solving (8), (9), and (10) results in

$$R_1 = 397\ \text{K}\Omega$$
$$R_2 = 1.80\ \text{M}\Omega \tag{11}$$
$$R_3 = 1.80\ \text{M}\Omega$$

4 Simulation Results

In the theoretical analysis, it was assumed that both the current in M_5 and M_8 are equal. This is a rough approximation because the mirrored current of M_5 is divided between M_8 and R_2. Therefore I_{D_8} depends on I_{D_5} and R_2, which results in a transcendental equation without a closed-form solution. Hence, the theoretical resistance values were used as a starting point and the final values were optimized through simulation until a minimum $\partial V_{REF}/\partial T$ had been achieved. In these adjustments, it was verified that by keeping M_5 closer to the moderate inversion region (i.e., $V_{GS_5} \approx V_{th}$), the variation of V_{REF} over the temperature was greatly reduced than biasing M_5 in the weak inversion.

Table 2 shows the final values of the transistors widths and lengths, the resistors and capacitors values. Where the capacitance C_C is implemented by a MIM capacitor that can be placed on top of the bandgap resistors. Hence, its area was chosen to be equal to the total resistance area, resulting in a 20 pF capacitor

Table 2. Transistors, resistors, and capacitor final sizing values.

# Transistor	(W/L) (μm)
M_1	0.64/10
M_3, M_6, M_9	3/0.75
M_4, M_7	3/3
M_2, M_5	5/10
M_8	4×5/10
# Resistor	MΩ
R_1	0.260
R_2	2.455
R_3	1.281
# Capacitor	pF
C_c	20

Fig. 4 shows the simulation results of V_{REF} as a function of the temperature for $V_{DD} = 0.9$ V. The maximum and minimum value of V_{REF} are 451.69 mV and 450.16 mV, respectively. Resulting in a total variation of 1.54 mV and, a temperature coefficient ($TC = (\Delta V_{REF} \cdot 1{\times}10^6)/(V_{REF,27ºC}\ \Delta T)$) of 24 ppm/ºC. Fig. 5 shows the simulation results of V_{REF} when sweeping the supply voltage from 0 to 1.2 V at 27 ºC. The smallest V_{DD} voltage for the bandgap to provide a stable reference voltage is 0.6 V. Lastly, Fig. 6 shows the Power Supply Rejection Ratio performance for $V_{DD} = 0.9$ V at 27 ºC. The highest PSRR value of -40 dB occurs for frequencies bellow 20 KHz.

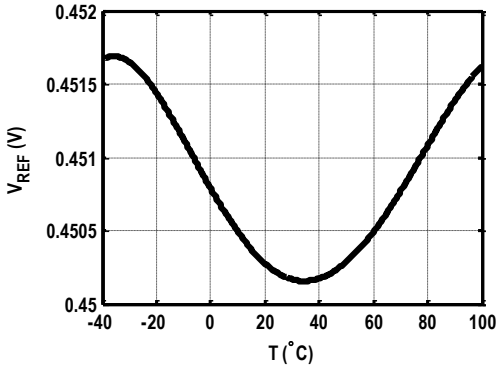

Fig. 4 Simulation results of V_{REF} as a function of the temperature for $V_{DD} = 0.9$ V.

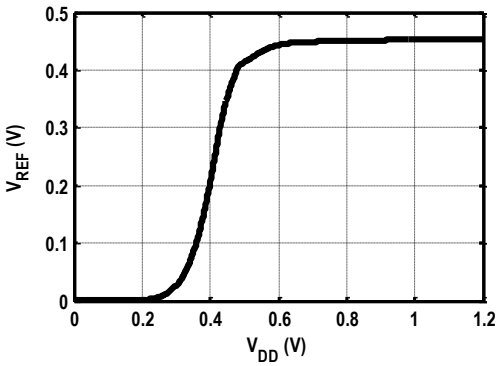

Fig. 5 Simulation results for V_{REF} as a function of V_{DD} at 27 ºC.

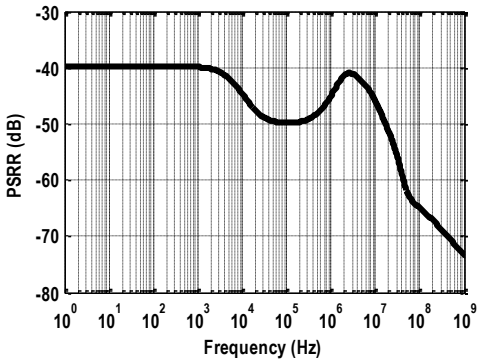

Fig. 6 Simulation results of the Power Supply Rejection Ratio (PSRR) of the bandgap circuit for $V_{DD} = 0.9$ V and $T = 27$°C.

5 Conclusion

This paper described the analysis of an all CMOS bandgap voltage reference circuit. This analysis showed that, in order to minimize the temperature variation of the reference voltage value, it is better to bias one of the diode connected transistors of the bandgap in the moderation region instead than in the weak inversion region. From this analysis a complete step-by-step design methodology was develop and described in this paper. This methodology is based on first obtaining an initial guess for the sizes of the devices and the using Spectre simulations to adjust the sizing and thus optimize the circuit in order to obtain the lowest possible of V_{REF} over temperature.

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